2.8 V to 5.5 V Input
5 A Synchronous Buck Regulator

DESCRIPTION

The SiP12108 is a high frequency current-mode constant on-time (CM-COT) synchronous buck regulator with integrated high-side and low-side power MOSFETs. Its power stage is capable of supplying 5 A continuous current at 4 MHz switching frequency. This regulator produces an adjustable output voltage down to 0.6 V from 2.8 V to 5.5 V input rail to accommodate a variety of applications, including computing, consumer electronics, telecom, and industrial.

SiP12108's CM-COT architecture delivers ultra-fast transient response with minimum output capacitance and tight ripple regulation at very light load. The part is stable with any capacitor type and no ESR network is required for loop stability. The device also incorporates a power saving scheme that significantly increases light load efficiency.

The SiP12108 integrates a full protection feature set, including output overvoltage protection (OVP), output under voltage protection (UVP) and thermal shutdown (OTP). The "A" version of the device, SiP12108A, does not have the UVP feature. They also incorporate UVLO for the input rail and an internal soft-start ramp.

The SiP12108 is available in lead (Pb)-free power enhanced 3 mm x 3 mm QFN-16 package.

FEATURES

Pb-free

RoHS COMPLIANT

HALOGEN FREE

- 2.8 V to 5.5 V input voltage
- Adjustable output voltage down to 0.6 V
- 5 A continuous output current
- Programmable switching frequency up to 4 MHz
- 95 % peak efficiency
- Stable with any capacitor. No external ESR network required.
- Ultrafast transient response
- Selectable power saving (PSM) mode or forced continuous mode
- ± 1 % accuracy of V_{OUT} setting
- Pulse-by-pulse current limit
- Scalable with SiP12107 - 3 A
- SiP12108 is fully protected with OTP, SCP, UVP, OVP
- SiP12108A is fully protected with OTP, SCP, OVP
- PGOOD Indicator
- PowerCAD Simulation software available at vishay.transim.com/login.aspx
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Point of load regulation for low-power processors, network processors, DSPs, FPGAs, and ASICs
- Low voltage, distributed power architectures with 3.3 V or 5 V rails
- Computing, broadband, networking, LAN/WAN, optical, test and measurement
- A/V, high density cards, storage, DSL, STB, DVR, DTV, Industrial PC

TYPICAL APPLICATION CIRCUIT

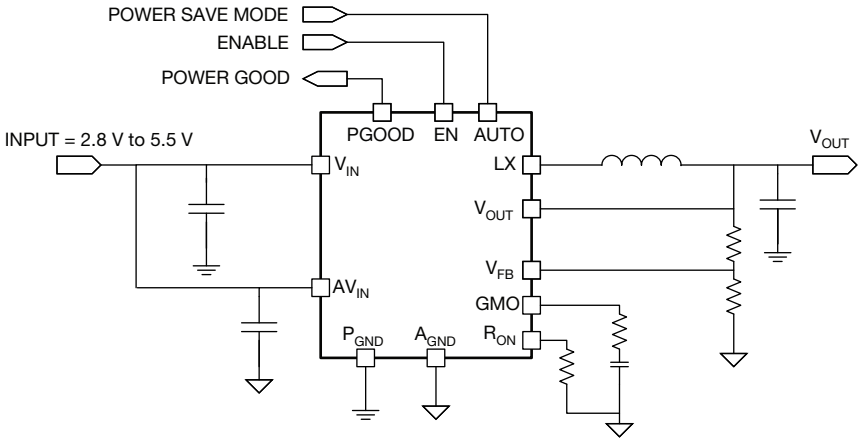


Fig. 1 - Typical Application Circuit for SiP12108

ABSOLUTE MAXIMUM RATINGS			
ELECTRICAL PARAMETER	**CONDITIONS**	**LIMIT**	**UNIT**
V_{IN}	Reference to P_{GND}	-0.3 to 6	V
AV_{IN}	Reference to A_{GND}	-0.3 to 6	
LX	Reference to P_{GND}	-0.3 to 6	
A_{GND} to P_{GND}		-0.3 to +0.3	
All Logic Inputs	Reference to A_{GND}	-0.3 to AV_{IN} + 0.3	
TEMPERATURE			
Max. Operating Junction Temperature		150	°C
Storage Temperature		-65 to 150	
POWER DISSIPATION			
Junction to Ambient Thermal Impedance (R_{thJA})		36.3	°C/W
Maximum Power Dissipation	Ambient temperature = 25 °C	3.4	W
	Ambient temperature = 100 °C	1.3	
ESD PROTECTION			
	HBM	4	kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE				
ELECTRICAL PARAMETER	**MINIMUM**	**TYPICAL**	**MAXIMUM**	**UNIT**
V_{IN}	2.8	-	5.5	V
AV_{IN}	2.8	-	5.5	
LX	-1	-	5.5	
V_{OUT}	0.6	-	0.85 x V_{IN}	
Ambient Temperature	-40 to 85			°C

ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITION UNLESS OTHERWISE SPECIFIED V_{IN} = AV_{IN} = 3.3 V, T_A = -40 °C to 85 °C	LIMITS			UNIT
			MIN.	TYP.	MAX.	
POWER SUPPLY						
Power Input Voltage Range	V_{IN}		2.8	-	5.5	V
Bias Input Voltage Range	AV_{IN}		2.8	-	5.5	
Input Current	I_{IN_NOLOAD}	Non- switching, I_O = 0 A, R_{on} = 100 kΩ, AUTO = Low	-	1200	-	µA
Shutdown Current	I_{IN_SHDN}	EN = 0 V	-	6	9.5	
AV_{IN} UVLO Threshold	AV_{IN_UVLO}	AV_{IN} rising	2.3	2.55	2.8	V
AV_{IN} UVLO Hysteresis	$AV_{IN\_UVLO\_HYS}$		-	300	-	mV
PWM CONTROLLER						
Feedback Reference	V_{FB}	T_A = 0 °C to +70 °C	0.594	0.600	0.606	V
		T_A = -40 °C to +85 °C	0.591	0.600	0.609	
V_{FB} Input Bias Current	I_{FB}		-	2	200	nA
Transconductance	g_m		-	1	-	mS
GMO Source Current	I_{GMO_SOURCE}		-	50	-	µA
GMO Sink Current	I_{GMO_SINK}		-	50	-	
Switching Frequency Range	f_{SW}	Guaranted by design	0.2	-	4	MHz
Minimum On-Time	t_{ON_MIN}	Guaranted by design	-	50	-	ns
Minimum Off-Time	t_{OFF_MIN}	V_{OUT} = 1.2 V, R_{ON} = 100 kΩ	-	125	-	
Soft Start Time	t_{SS}		-	1.5	-	ms
INTEGRATED MOSFETS						
High-Side On Resistance	R_{ON_HS}	V_{IN} = AV_{IN} = 5 V	-	35	51	mΩ
Low-Side On Resistance	R_{ON_LS}		-	23	35	
FAULT PROTECTIONS						
Over Current Limit	I_{OCP}	Inductor valley current	-	7.5	-	A
Output OVP Threshold	V_{FB_OVP}	V_{FB} with respect to 0.6 V reference	-	21	-	%
Output UVP Threshold	V_{FB_UVP}		-	-25	-	
Over Temperature Protection		Rising temperature	-	160	-	°C
		Hysteresis	-	30	-	
POWER GOOD						
Power Good Output Threshold	$V_{FB\_RISING\_VTH\_OV}$	V_{FB} rising above 0.6 V reference	-	21	-	%
	$V_{FB\_FALLING\_VTH\_UV}$	V_{FB} falling below 0.6 V reference	-	-12.5	-	
Power Good On Resistance	R_{ON_PGOOD}		-	30	60	Ω
Power Good Delay Time	t_{DLY_PGOOD}		-	4	-	µs
ENABLE THRESHOLD						
Logic High Level	V_{EN_H}		1.5	-	-	V
Logic Low Level	V_{EN_L}		-	-	0.4	

FUNCTIONAL BLOCK DIAGRAM

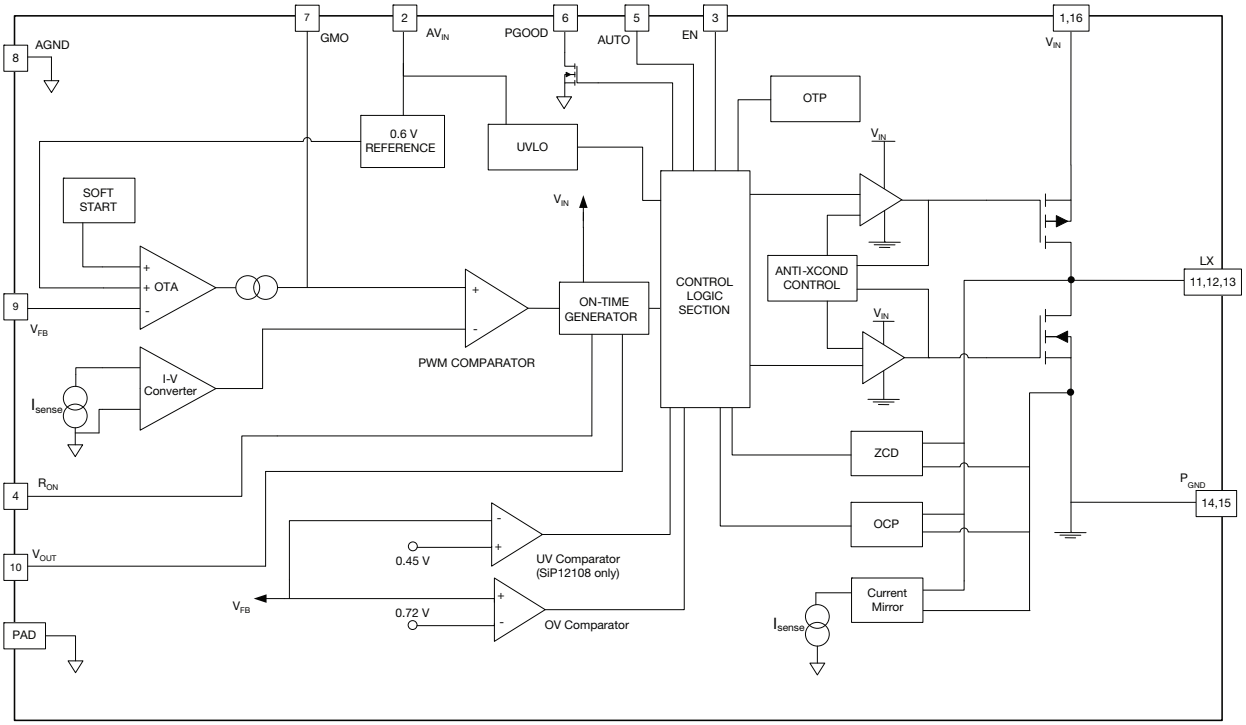
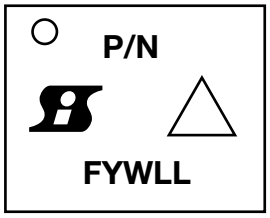


Fig. 2 - SiP12108 Functional Block Diagram

ORDERING INFORMATION		
PART NUMBER	**PACKAGE**	**MARKING (LINE 2: P/N)**
SiP12108DMP-T1GE4	QFN16 3x3	2108
SiP12108ADMP-T1GE4(1)	QFN16 3x3	108A
SiP12108DB	N/A	
SiP12108ADB(1)		

Note

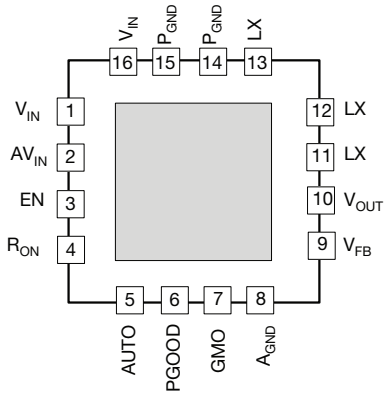
(1) Output undervoltage protection (UVP) disabled



Format:

Line 1: Dot
Line 2: P/N
Line 3: Siliconix Logo + ESD Symbol
Line 4: Factory Code + Year Code + Work Week Code + LOT Code

PIN CONFIGURATION



QFN16 3x3

Fig. 3 - SiP12108 Pin Configuration (Top View)

PIN CONFIGURATION		
PIN NUMBER	**NAME**	**FUNCTION**
1, 16	V_{IN}	Input supply voltage for power MOS. V_{IN} = 2.8 V to 5.5 V
2	AV_{IN}	Input supply voltage for internal circuitry. AV_{IN} = 2.8 V to 5.5 V
3	EN	Enable pin. Pull enable above 1.5 V to enable the part and below 0.4 V to disable. Do not float this pin.
4	R_{ON}	An external resistor between R_{ON} and GND sets the switching on time.
5	AUTO	Sets switching mode. Connect AUTO to AV_{IN} for forced continuous mode and AUTO to GND for power save mode. Do not float.
6	PGOOD	Power good output. Open drain.
7	GMO	Connect to an external RC network for loop compensation and droop function
8	A_{GND}	Analog ground
9	V_{FB}	Feedback voltage. 0.6 V (typ.). Use a resistor divider between V_{OUT} and A_{GND} to set the output voltage.
10	V_{OUT}	V_{OUT}, output voltage sense connection
11, 12, 13	LX	Switching output, inductor connection point
14, 15	P_{GND}	Power ground
EP		Exposed paddle (bottom). Connect to a good PCB thermal ground plane.

ELECTRICAL CHARACTERISTICS (V_{IN} = 3.3 V, L = 1 µH, C = 3 x 22 µF, f_{SW} = 1.2 MHz unless noted otherwise)

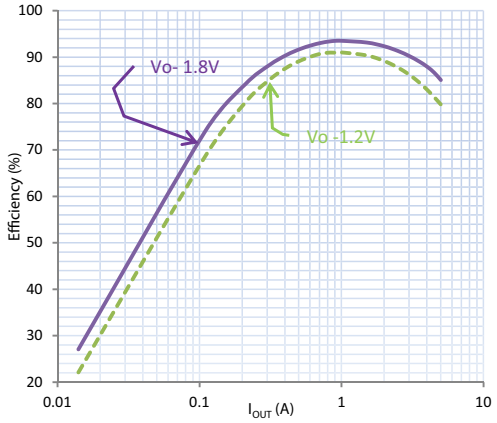


Fig. 4 - Efficiency - PWM Mode

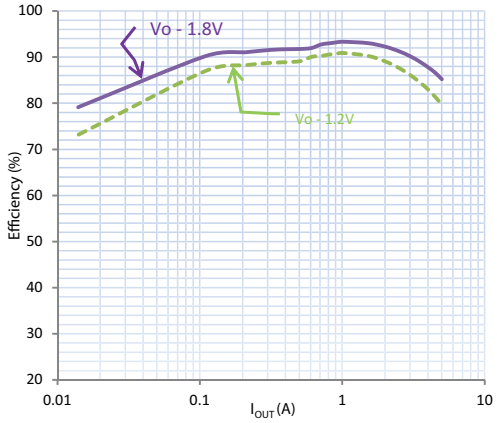


Fig. 7 - Efficiency - PSM Mode

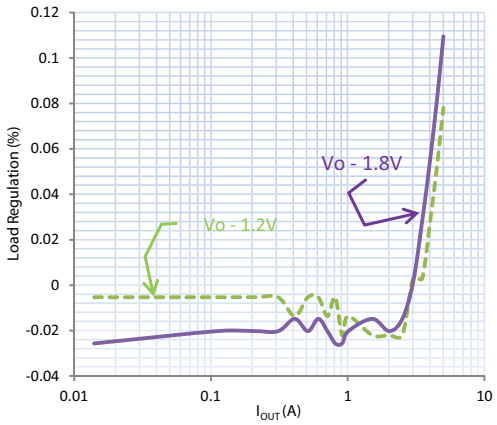


Fig. 5 - Load Regulation - PWM Mode

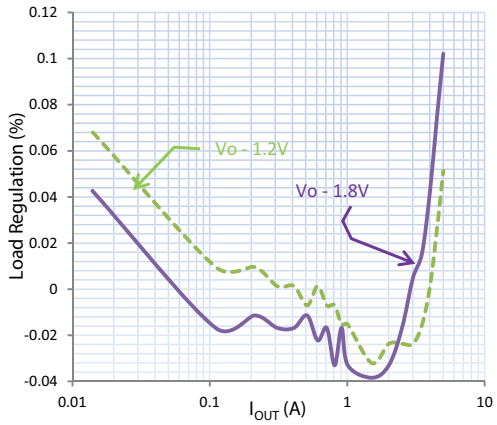


Fig. 8 - Load Regulation - PSM Mode

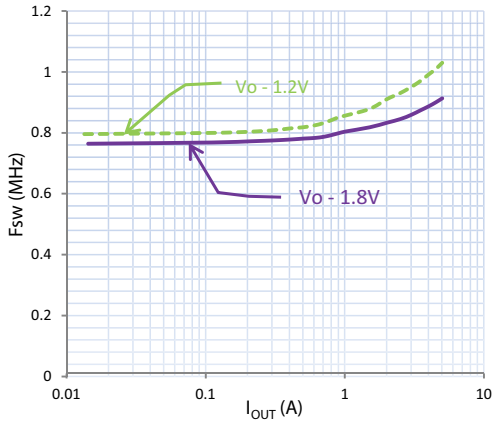


Fig. 6 - F_{SW} Variation - PWM Mode

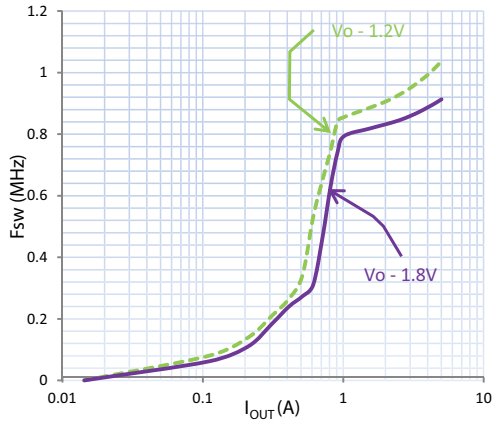


Fig. 9 - F_{SW} Variation - PSM Mode

ELECTRICAL CHARACTERISTICS (V_{IN} = 3.3 V, L = 1 µH, C = 3 x 22 µF, f_{SW} = 1.2 MHz unless noted otherwise)

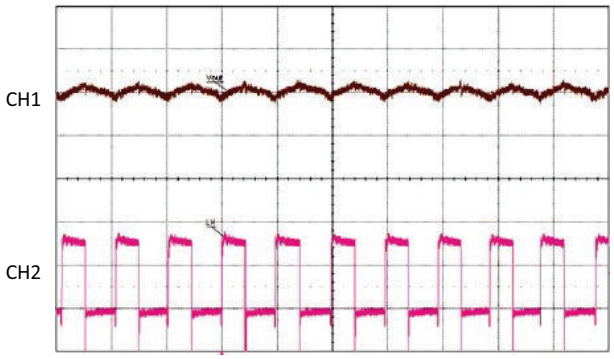


Fig. 10 - PWM Mode- Steady - State Ripple and LX, 5 A Load
CH1 = V_{OUT} , 20 mV/div, CH2 = LX, 2 V/div, Time = 1 µs/div

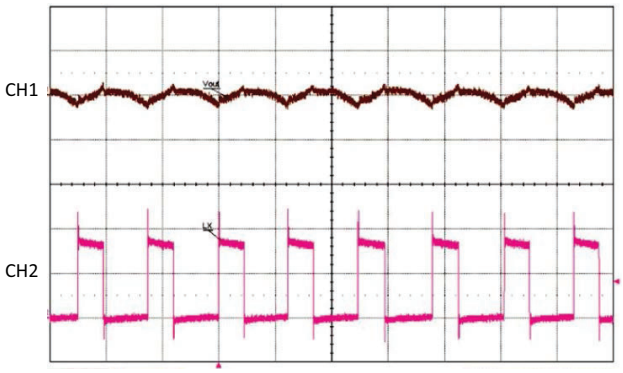


Fig. 13 - PWM Mode- Steady - State Ripple and LX, 0 A Load
CH1 = V_{OUT} , 20 mV/div, CH2 = LX, 2 V/div, Time = 1 µs/div

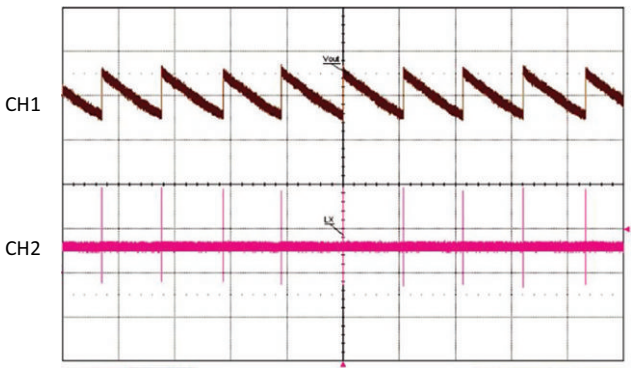


Fig. 11 - PSM Mode- Steady - State Ripple and LX, 0 A Load
CH1 = V_{OUT} , 20 mV/div, CH2 = LX, 2 V/div, Time = 10 ms/div

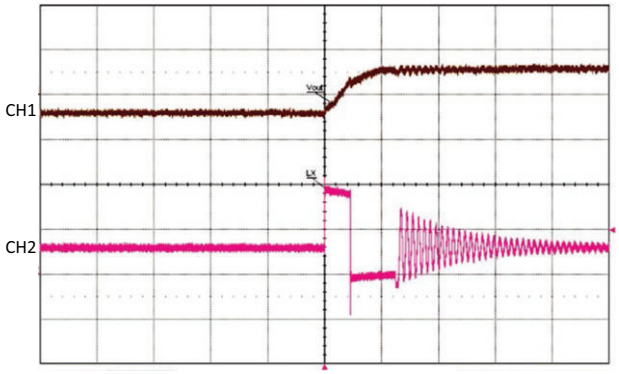


Fig. 14 - PSM Mode- Steady - State Ripple and LX, 0 A Load
CH1 = V_{OUT} , 20 mV/div, CH2 = LX, 2 V/div, Time = 1 µs/div

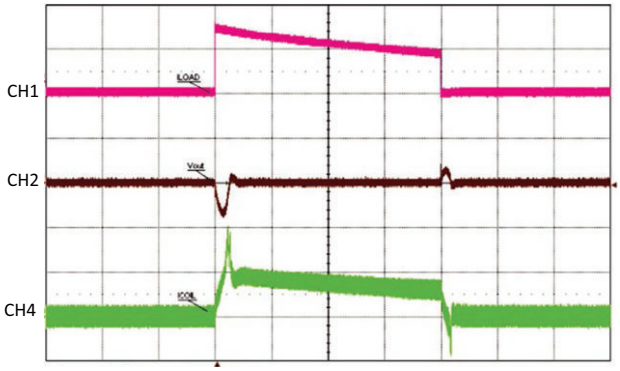


Fig. 12 - Load Step 0 A to 5 A to 0 A
CH1 = I_{load}, CH2 = V_{OUT}, 500 mV/div,
CH4 = I_{coil}, 5 A/div, Time = 100 µs/div

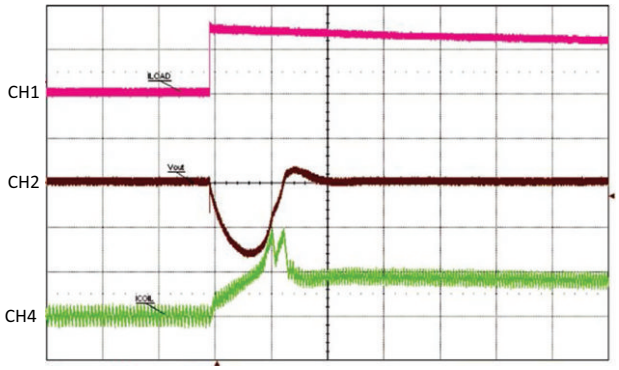


Fig. 15 - Load Step 0 A to 5 A, Rising Edge
CH1 = I_{load}, CH2 = V_{OUT}, 200 mV/div,
CH4 = I_{coil}, 5 A/div, Time = 20 µs/div

ELECTRICAL CHARACTERISTICS (V_{IN} = 3.3 V, L = 1 µH, C = 3 x 22 µF, f_{SW} = 1.2 MHz unless noted otherwise)

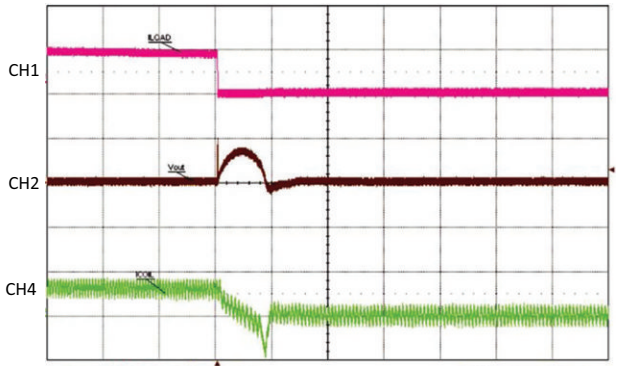


Fig. 16 - Load Step 0 A to 5 A, Falling Edge
CH1 = I_{load}, CH2 = V_{OUT}, 200 mV/div,
CH4 = I_{coil}, 5 A/div, Time = 20 µs/div

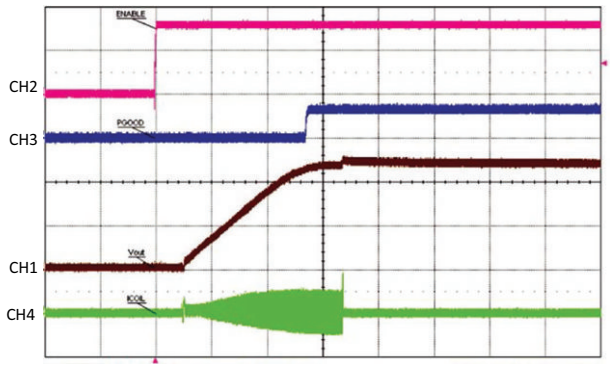


Fig. 19 - Turn-On Time PSM Mode, 0 A Load
CH1 = V_{OUT} , 500 mV/div, CH2 = EN, 2 V/div, CH3 = PGOOD,
5 V/div, CH4 = I_{coil}, 2 A/div, Time = 500 µs/div

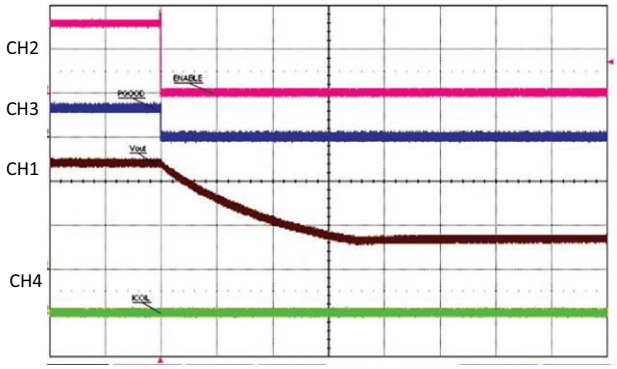


Fig. 17 - Turn-Off Time PSM Mode, 0 A Load
CH1 = V_{OUT} , 500 mV/div, CH2 = EN, 2 V/div, CH3 = PGOOD,
5 V/div, CH4 = I_{coil}, 2 A/div, Time = 500 µs/div

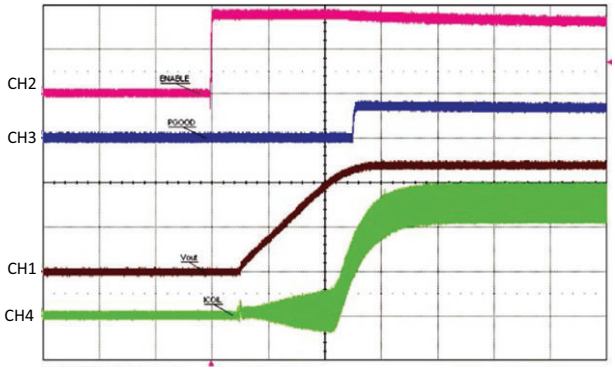


Fig. 20 - Turn-On Time PWM Mode, 5 A Load
CH1 = V_{OUT} , 500 mV/div, CH2 = EN, 2 V/div, CH3 = PGOOD,
5 V/div, CH4 = I_{coil}, 2 A/div, Time = 500 µs/div

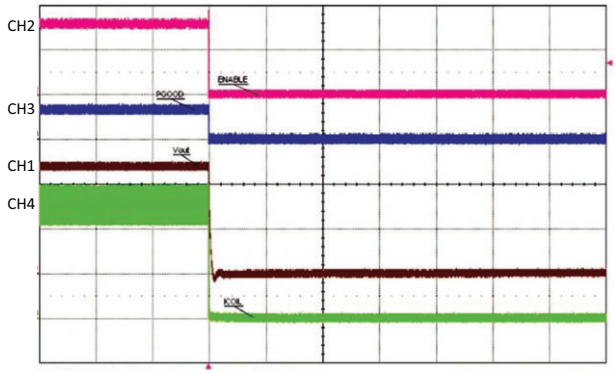


Fig. 18 - Turn-Off Time PWM Mode, 5 A Load
CH1 = V_{OUT} , 500 mV/div, CH2 = EN, 2 V/div, CH3 = PGOOD,
5 V/div, CH4 = I_{coil}, 2 A/div, Time = 500 µs/div

OPERATIONAL DESCRIPTION

Device Overview

SiP12108 is a high-efficiency monolithic synchronous buck regulator capable of delivering up to 5 A continuous current. The device has programmable switching frequency up to 4 MHz. The control scheme is based on current-mode constant-on-time architecture, which delivers fast transient response and minimizes external components. Thanks to the internal current ramp information, no high-ESR output bulk or virtual ESR network is required for the loop stability. This device also incorporates a power saving feature by enabling diode emulation mode and frequency foldback as load decreases.

SiP12108 has a full set of protection and monitoring features:

- Over current protection in pulse-by-pulse mode
- Output over voltage protection
- Output under voltage protection with device latch
- Over temperature protection with hysteresis
- Dedicated enable pin for easy power sequencing
- Power Good open drain output

This device is available in QFN16 3x3 package to deliver high power density and minimize PCB area.

Power Stage

SiP12108 integrated synchronous MOSFETs . The MOSFETs are optimized to achieve 95 % efficiency at 2 MHz switching frequency.

The power input voltage (V_{IN}) can go up to 5.5 V and as low as 2.8 V for power conversion. The logic bias voltage (AV_{IN}) ranges from 2.8 V to 5.5 V.

PWM Control Mechanism

SiP12108 employs a state-of-the-art current-mode COT control mechanism. During steady-state operation, output voltage is compared with internal reference (0.6 V typ.) and the amplified error signal (V_{COMP}) is generated on the COMP pin. In the meantime, inductor valley current is sensed, and its slope (I_{sense}) is converted into a voltage signal ($V_{current}$) to be compared with V_{COMP}. Once $V_{current}$ is lower than V_{COMP}, a single shot on-time is generated for a fixed time programmed by the external R_{ON}. Figure 4 illustrates the basic block diagram for CM-COT architecture and figure 5 demonstrates the basic operational principle:

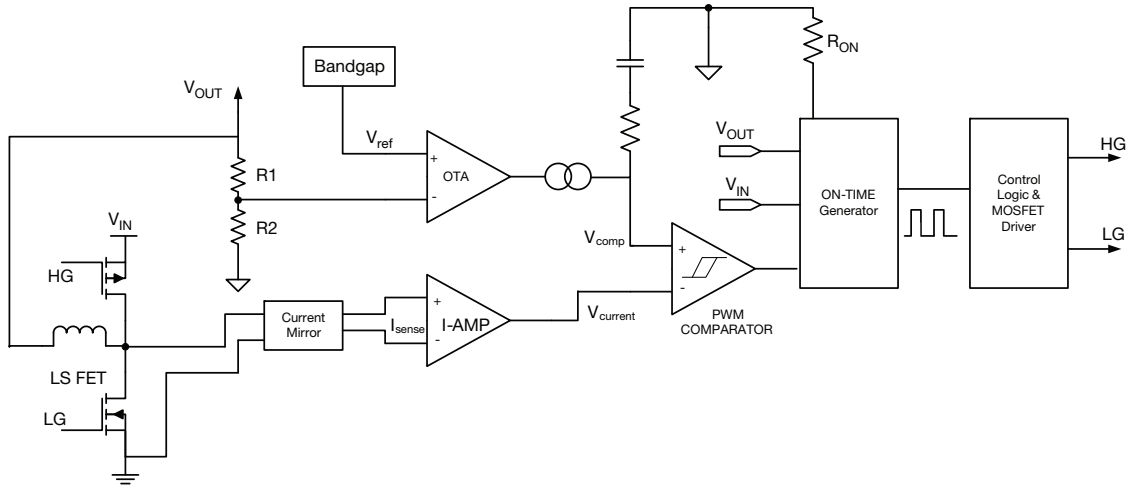


Fig. 21 - CM-COT Block Diagram

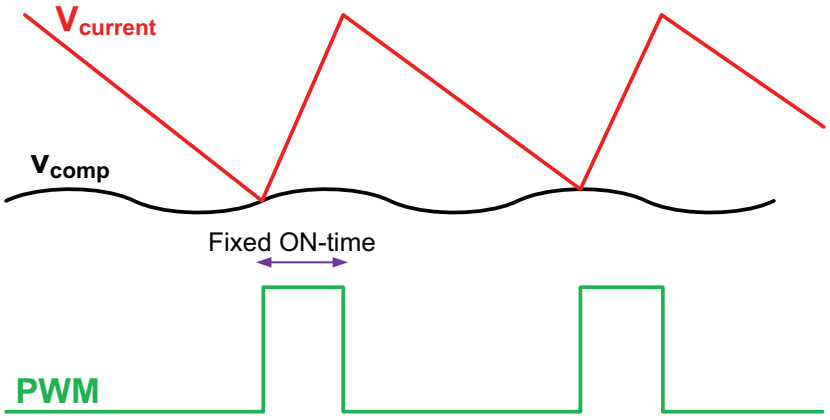


Fig. 22 - CM-COT Operational Principle

The following equation illustrates the relationship between on-time, V_{IN}, V_{OUT} and R_{ON} value:

$$T_{ON} = R_{ON} \times K \times \frac{V_{OUT}}{V_{IN}}, \text{ where } K = 10.45 \times 10^{-12} \text{ a constant set internally}$$

Once on-time is set, the pseudo constant frequency is then determined by the following equation:

$$f_{sw} = \frac{D}{T_{ON}} = \frac{\frac{V_{OUT}}{V_{IN}}}{\frac{V_{OUT}}{V_{IN}} \times R_{ON} \times K} = \frac{1}{R_{ON} \times K}$$

Loop Stability and Compensator Design

Due to the nature of current mode control, a simple RC network (type II compensator) is required between COMP and A_{GND} for loop stability and transient response purposes. The general concept of this loop design is to introduce a single zero through the compensator to determine the crossover frequency of overall close loop system.

The overall loop can be broken down into following segments.

Output feedback divider transfer function H_{fb}:

$$H_{fb} = \frac{R_{fb2}}{R_{fb1} \times R_{fb2}}$$

Voltage compensator transfer function G_{COMP} (s):

$$G_{COMP}(s) = \frac{R_O \times (1 + sC_{COMP}R_{COMP})}{(1 + sR_OC_{COMP})} gm$$

Modulator transfer function H_{mod} (s):

$$H_{mod}(s) = \frac{1}{AV_1 \times R_{DS(on)}} \times \frac{R_{load} \times (1 + sC_OR_{ESR})}{(1 + sC_OR_{load})}$$

The complete loop transfer function is given by:

$$H_{mod}(s) = \frac{R_{fb2}}{R_{fb1} \times R_{fb2}} \times \frac{R_O \times (1 + sC_{COMP}R_{COMP})}{(1 + sR_OC_{COMP})} gm \times \frac{1}{AV_1 \times R_{DS(on)}} \times \frac{R_{load} \times (1 + sC_OR_{ESR})}{(1 + sC_OR_{load})}$$

When:

C_{COMP} = Compensation capacitor
R_{COMP} = Compensation resistor
gm = Error amplifier transconductance
R_{load} = Load resistance
C_O = Output capacitor
$R_{DS(on)}$ = LS switch resistance
R_{fb1} = Feedback resistor connect to LX
R_{fb2} = Feedback resistor connect to ground
R_O = Output impedance of error amplifier = 20 MΩ
AV_1 = Voltage to current gain = 3

Power Save Mode using AUTO Pin

To further improve efficiency at light loads, SiP12108 provides a set of innovative implementations to eliminate LS recirculating current and switching losses. The internal Zero Crossing Detector (ZCD) monitors LX node voltage to determine when inductor current starts to flow negatively. In power saving mode (PSM), as soon as inductor valley current crosses zero, the device first deploys diode emulation mode by turning off LS FET. If load further decreases, switching frequency is further reduced proportional to load condition to save switching losses. The switching frequency is set by the controller to maintain regulation. At zero load this frequency can go as low as hundreds of Hz.

Whenever fixed frequency PWM operation is required over the entire load span, the power saving mode feature can be disabled by connecting AUTO pin to V_{IN} or AV_{IN}.

OUTPUT MONITORING AND PROTECTION FEATURES

Output Over-Current Protection (OCP)

SiP12108 has pulse-by-pulse over-current limit control. The inductor valley current is monitored during LS FET turn-on period through $R_{DS(on)}$ sensing. After a pre-defined time, the valley current is compared with internal threshold (7.5 A typ.) to determine the threshold for OCP. If monitored current is higher than threshold, HS turn-on pulse is skipped and LS FET is kept on until the valley current returns below OCP limit.

In the severe over-current condition, pulse-by-pulse current limit eventually triggers output under-voltage protection (UVP), which latches the device off to prevent catastrophic thermal-related failure. UVP is described in the next section.

OCP is enabled immediately after AV_{IN} passes UVLO level.

Figure 6 illustrates the OCP operation.

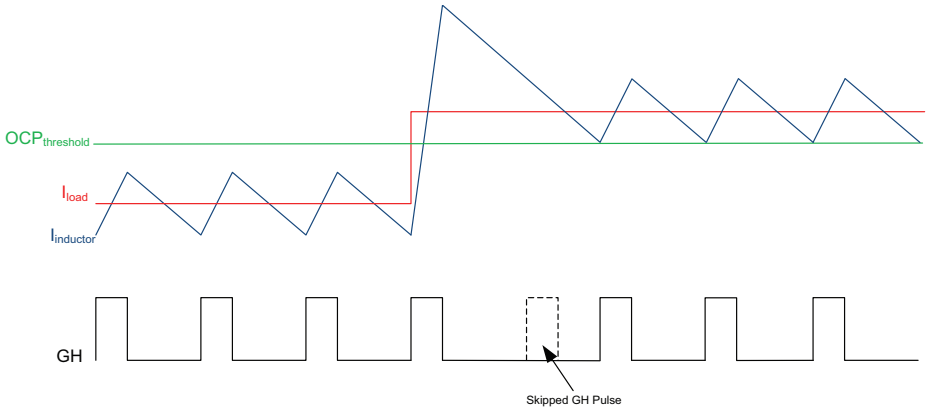


Fig. 23 - Over-Current Protection Illustration

Output Under-Voltage Protection (UVP)

UVP is implemented by monitoring output through V_{FB} pin. Once the voltage level at V_{FB} is below 0.45 V for more than 20 µs, then UVP event is recognized and both HS and LS MOSFETs are turned off. UVP latches the device off until either AV_{IN} or EN is recycled.

UVP is only active after the completion of soft-start sequence. This function only exists on SiP12108. On the “A” version of the device, SiP12108A, this feature is disabled.

Output Over-Voltage Protection (OVP)

For OVP implementation, output is monitored through V_{FB} pin. After soft-start, if the voltage level at V_{FB} is above 21 % (typ.), OVP is triggered with HS FET turning off and LS FET turning on immediately to discharge the output. Normal operation is resumed once V_{FB} drops back to 0.6 V.

OVP is active immediately after AV_{IN} passes UVLO level.

Over-Temperature Protection (OTP)

SiP12108 has internal thermal monitor block that turns off both HS and LS FETs when junction temperature is above 160 °C (typ.). A hysteresis of 30 °C is implemented, so when junction temperature drops below 130 °C, the device restarts by initiating the soft-start sequence again.

Soft Startup

SiP12108 deploys an internally regulated soft-start sequence to realize a monotonic startup ramp without any output overshoot. Once AV_{IN} is above UVLO level (2.55 V typ.). Both the reference and V_{OUT} will ramp up slowly to regulation in 1 ms (typ.) with the reference going from 0 V to 0.6 V and V_{OUT} rising monotonically to the programmed output voltage.

During soft-start period, OCP is activated. OVP and short-circuit protection are not active until soft-start is complete.

Pre-bias Startup

In case of pre-bias startup, output is monitored through V_{FB} pin. If the sensed voltage on V_{FB} is higher than the internal reference ramp value, control logic prevents HS and LS FET from switching to avoid negative output voltage spike and excessive current sinking through LS FET.

Power Good (PGOOD)

SiP12108's Power Good is an open-drain output. Pull PGOOD pin high up to 5 V through a 10K resistor to use this signal. Power Good window is shown in the below diagram. If voltage level on V_{FB} pin is out of this window, PGOOD signal is de-asserted by pulling down to GND.

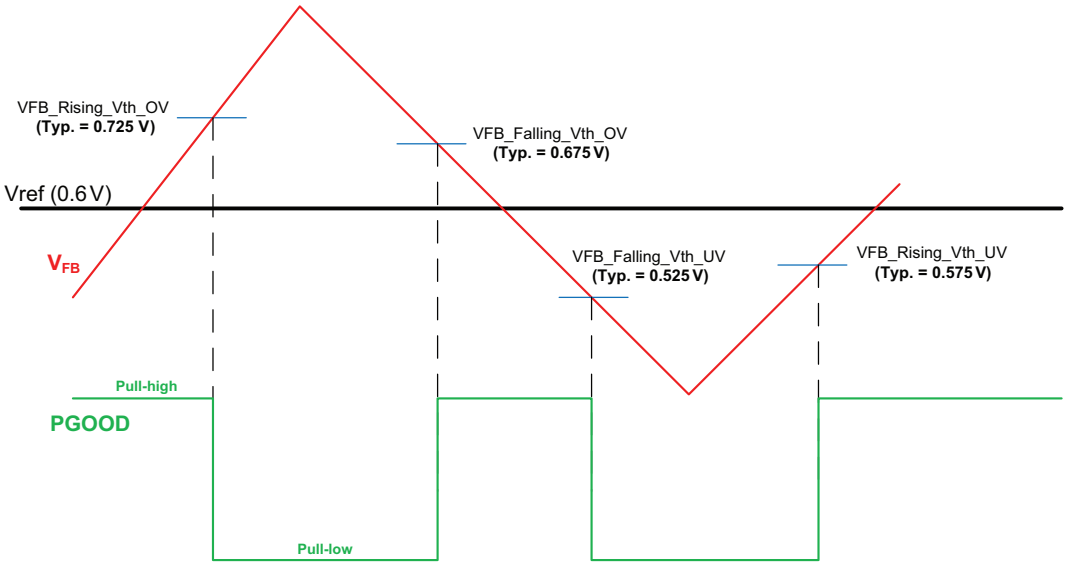


Fig. 24 - PGOOD Window and Timing Diagram

DESIGN PROCEDURE

The design process of the SiP12108 is quite straight forward. Only few passive components such as output capacitors, inductor and R_{on} resistor need to be selected.

The following paragraph describes the selection procedure for these peripheral components for a given operating conditions.

In the next example the following definitions apply:

$V_{INmax.}$: the highest specified input voltage

$V_{INmin.}$: the minimum effective input voltage subject to voltage drops due to connectors, fuses, switches, and PCB traces

There are two values of load current to evaluate - continuous load current and peak load current.

Continuous load current relates to thermal stress considerations which drive the selection of the inductor and input capacitors.

Peak load current determines instantaneous component stresses and filtering requirements such as inductor saturation, output capacitors, and design of the current limit circuit.

The following specifications are used in this design:

- V_{IN} = 3.3 V ± 10 %
- V_{OUT} = 1.2 V ± 1 %
- F_{SW} = 1 MHz
- Load = 5 A maximum

Setting the Output Voltage

The output voltage is set by using a resistor divider on the feedback (V_{FB}) pin. The V_{FB} pin is the negative input of the internal error amplifier.

When in regulation the V_{FB} voltage is 0.6 V. The output voltage V_O is set based on the following formula.

$V_O = V_{FB} (1 + R1/R2)$

where R1 and R2 are shown in figure 21.

Setting Switching Frequency

Selection of the switching frequency requires making a trade-off between the size and cost of the external filter components (inductor and output capacitor) and the power conversion efficiency. The desired switching frequency, 1 MHz was chosen based on optimizing efficiency while maintaining a small footprint and minimizing component cost.

In order to set the design for 1 MHz switching frequency, (R_{ON}) resistor which determines the on-time (indirectly setting the frequency) needs to be calculated using the following equation.

$$R_{ON} = \frac{1}{F_{SW} \times K} = \frac{1}{1 \times 10^{6} \times 10.45 \times 10^{-12}} \cong 105\ k\Omega$$

INDUCTOR SELECTION

In order to determine the inductance, the ripple current must first be defined. Cost, PCB size, output ripple, and efficiency are all used in the selection process. Low inductor values result in smaller size and allow faster transient performance but create higher ripple current which can reduce efficiency. Higher inductor values will reduce the ripple current while compromising the efficiency (higher DCR) and transient response.

The ripple current will also set the boundary for power-save operation. The switcher will typically enter power-save mode when the load current decreases to 1/2 of the ripple current. For example, if ripple current is 1 A then power-save operation will typically start at loads approaching 0.5 A. Alternatively, if ripple current is set at 40 % of maximum load current, then power-save will start for loads less than ~ 20 % of maximum current.

Inductor selection for the SiP12108 should be designed where the ripple current is ~ 50 % in all situations with V_{IN} 3.6 V and less.

For example 3.3 V_{IN} to 1.2 V_{OUT} at 1 MHz.
dI = V/L x dt = ((3.3 - 1.2)/0.33) x 0.36 = 2.3 A, %dI = 2.3/5 = 46 %.

For higher V_{IN} > 3.6 V ripple current should be set to less then 40 %.

For 5 V_{IN} to 1.2 V_{OUT} at 1 MHz dI = ((5 - 1.2)/0.68) x 0.36) = 2 A, %dI = 2/5 = 40 %.

Output Capacitance Calculation

The output capacitance is usually chosen to meet transient requirements. A worst-case load release, from maximum load to no load at the exact moment when inductor current is at the peak, determines the required capacitance. If the load release is instantaneous (load changes from maximum to zero in < $1/F_{SW}$ µs), the output capacitor must absorb all the inductor's stored energy. This will approximately cause a peak voltage on the capacitor according to the following equation.

$$C_{OUTmin.} = \frac{L \times \left(I_{OUT} + \frac{1}{2} \times I_{RIPPLEmax.}\right)^2}{(V_{peak})^2 - (V_{OUT})^2}$$

Assuming a peak voltage V_{PEAK} of 1.3 V (100 mV rise upon load release), and a 5 A load release, the required capacitance is shown by the next equation.

$$C_{OUTmin.} = \frac{1\ \mu H \times (5\ A + 0.5 \times (0.81\ A))^2}{(1.3\ V)^2 - (1.2\ V)^2} = 116.8\ \mu F$$

If the load release is relatively slow, the output capacitance can be reduced. Using MLCC ceramic capacitors we will use 5 x 22 µF or 110 µF as the total output capacitance.

STABILITY CONSIDERATIONS

Using the output capacitance as a starting point for compensation values. Then, taking Bode plots and transient response measurements we can fine tune the compensation values.

Setting the crossover frequency to 1/5 of the switching frequency:
$F_0 = F_{sw}/5 = 1\ MHz/5 = 200\ kHz$
Setting the compensation zero at 1/5 to 1/10 the crossover frequency for the phase boost:

$$F_Z = \frac{1}{2\pi \times R_C \times C_C} = \frac{F_0}{5}$$

Setting C_C = 0.47 nF and solve for R_C

$$R_C = \frac{5}{2\pi \times C_C \times F_0} = \frac{5}{2\pi \times 0.47\ nF \times 200K} = 8.469K$$

SWITCHING FREQUENCY VARIATIONS

The switching frequency variation in COT can be mainly attributed to the increase in conduction losses as the load increases. The on time is "ideally constant" so the controller must account for losses by reducing the off time which increases the overall duty cycle. Hence the F_{SW} will tend to increase with load.

In power save mode (PSM) the IC will run in pulse skip mode at light loads. As the load increases the F_{SW} will increase until it reaches the nominal set F_{SW}. This transition occurs approximately when the load reaches to 20 % of the full load current.

DESIGN CONSIDERATION

For V_{OUT} higher then UVLO (2.55 V typ) and/or very slow V_{IN} slew rates. The IC may have difficulty in starting-up because V_{IN} level is limiting how fast V_{OUT} can rise. In these situations a divider for EN pin threshold (~1.15 V) derived from V_{IN} can be used. Allowing a higher V_{IN} level before switching begins and a smooth start-up. For example R_{top} = 60K and R_{bot} = 25K when V_{IN}=4 V, EN level will be 1.18 V.

THERMAL DESIGN

The 16 pin package includes a thermal pad for much better thermal performance when incorporated in the PCB footprint. As shown in the PCB layout at the end of this document. There are four vias evenly placed on the pad that help transfer the heat to other layers. Tying the paddle to the bottom layer through vias will provide the best thermal performance.

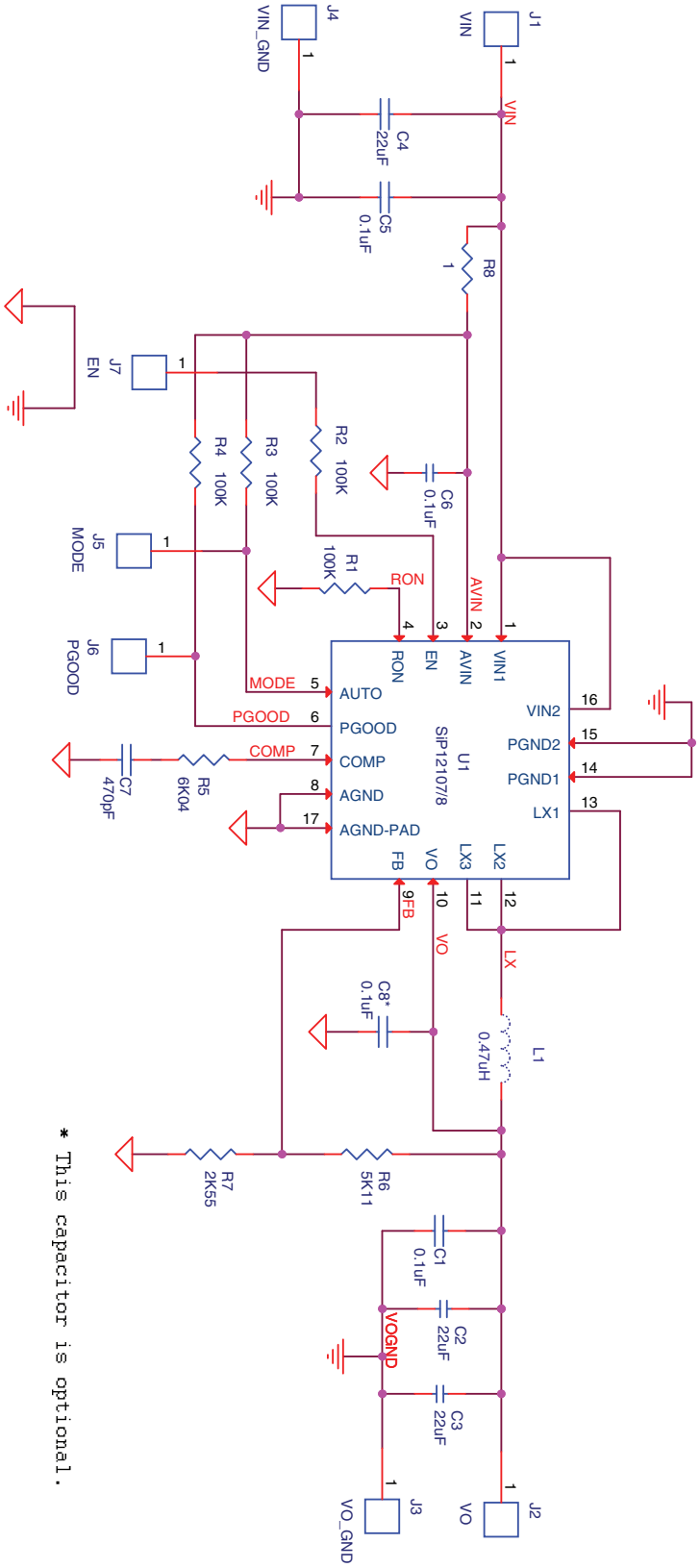


Fig. 25 - Reference Board Schematic

BILL OF MATERIALS

ITEM	QTY.	REFERENCE	VALUE	VOLTAGE	PCB FOOTPRINT	PART NUMBER	MANUFACTURER
1	2	C1, C5	0.1 µF	50 V	C0402-TDK	VJ0402Y104MXQCW1BC	Vishay
2	2	C2, C3, C4	22 µF	10 V	C0805-TDK	LMK212BJ226MG-T	Murata
4	1	C6	0.1 µF	10 V	C0603-TDK	GRM188R71C104KA01D	Murata
5	1	C7	470 pF	50 V	C0402-TDK	VJ0402A471JXACW1BC	TDK
6	1	C8 (1)	DNP	-	C0603-TDK	-	-
7	1	J1	VIN	-	TP30	5002K-ND	Keystone
8	1	J2	VO	-	TP30	5002K-ND	Keystone
9	1	J3	VO_GND	-	TP30	5002K-ND	Keystone
10	1	J4	VIN_GND	-	TP30	5002K-ND	Keystone
11	1	J5	MODE	-	TP30	5002K-ND	Keystone
12	1	J6	PGOOD	-	TP30	5002K-ND	Keystone
13	1	J7	EN	-	TP30	5002K-ND	Keystone
14	1	L1	0.47 µH	-	IHLP1616	IHLP1616BZERR47M11	Vishay
15	4	R1, R2, R3, R4	100K	50 V	R0402-Vishay	CRCW0402100KFKED	Vishay
16	1	R5	6K04	50 V	R0402-Vishay	TNPW04026K04BETD	Vishay
17	1	R6	5K11	50 V	R0402-Vishay	CRCW04025K11FKED	Vishay
18	1	R7	2K55	50 V	R0402-Vishay	TNPW04022K55BETD	Vishay
19	1	R8	1	50 V	R0402-Vishay	RC0402FR-071RL	Yageo
20	1	U1	SiP12107, SiP12108	-	MLP33-16	SiP1210x	Vishay

PCB LAYOUT OF REFERENCE BOARD

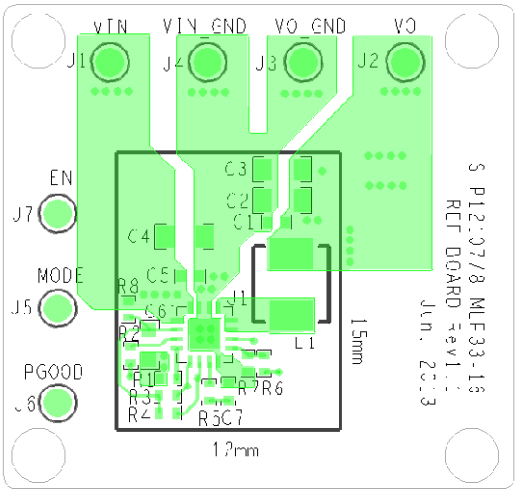


Fig. 26 - Top Layer

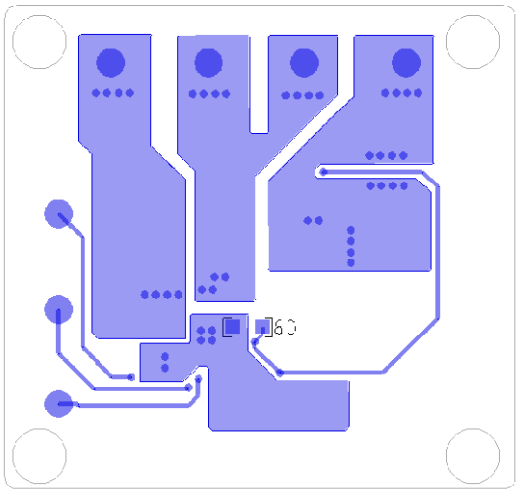
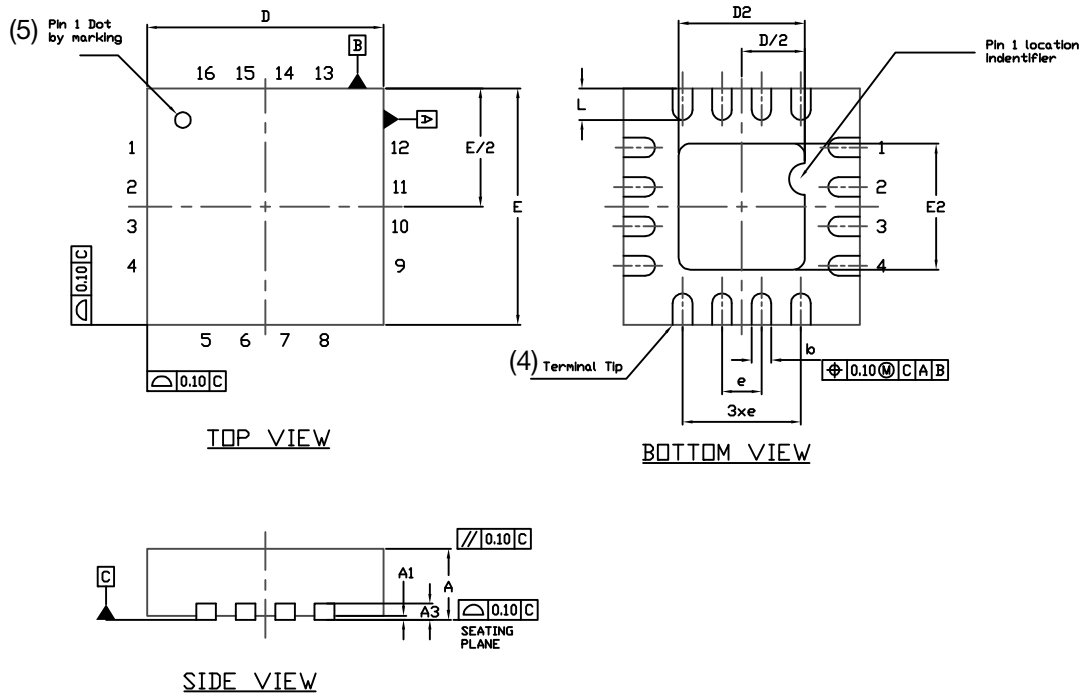


Fig. 27 - Bottom Layer

MLP33-16L CASE OUTLINE



DIMENSION	MILLIMETERS (1)			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.75	0.85	0.95	0.029	0.033	0.037
A1	0	-	0.05	0	-	0.002
A3		0.20 REF			0.001 REF	
b	0.18	0.25	0.30	0.007	0.010	0.012
D		3.00 BSC			0.118 BSC	
D2	1.5	1.6	1.7	0.059	0.063	0.067
e		0.50 BSC			0.020 BSC	
E		3.00 BSC			0.118 BSC	
E2	1.5	1.6	1.7	0.059	0.063	0.067
L	0.3	0.4	0.5	0.012	0.016	0.020
N (3)		16			16	
Nd (3)		4			4	
Ne (3)		4			4	

Notes

(1) Use millimeters as the primary measurement.
(2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.
(3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.
(4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
(5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.
(6) Package warpage max. 0.05 mm.

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