

# BLS9G3135L-400; BLS9G3135LS-400

LDMOS S-band radar power transistor

Rev. 1 — 6 April 2017

AMPLEON

Product data sheet

## 1. Product profile

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### 1.1 General description

400 W LDMOS power transistor for S-band radar applications in the frequency range from 3.1 GHz to 3.5 GHz.

**Table 1. Typical performance**

*Typical RF performance at  $T_{case} = 25\text{ °C}$ ;  $t_p = 300\text{ }\mu\text{s}$ ;  $\delta = 10\%$ ;  $I_{Dq} = 400\text{ mA}$ ; in a class-AB demo circuit.*

Test signal	f (GHz)	V <sub>DS</sub> (V)	P <sub>L</sub> (W)	G <sub>p</sub> (dB)	$\eta_D$ (%)
pulsed RF	3.1 to 3.5	32	425	12	43

### 1.2 Features and benefits

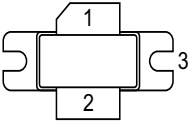
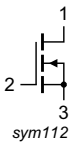
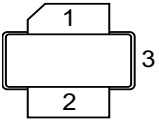
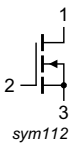
- High efficiency
- Excellent ruggedness
- Designed for S-band operation
- Excellent thermal stability
- Easy power control
- Integrated dual sided ESD protection enables excellent off-state isolation
- High flexibility with respect to pulse formats
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- S-band radar applications in the frequency range 3.1 GHz to 3.5 GHz

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>BLS9G3135L-400 (SOT502A)</b>			
1	drain		 sym112
2	gate		
3	source <sup>[1]</sup>		
<b>BLS9G3135LS-400 (SOT502B)</b>			
1	drain		 sym112
2	gate		
3	source <sup>[1]</sup>		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLS9G3135L-400	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A
BLS9G3135LS-400	-	earless flanged ceramic package; 2 leads	SOT502B

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
$V_{DS}$	drain-source voltage	-	65	V
$V_{GS}$	gate-source voltage	-6	+11	V
$T_{stg}$	storage temperature	-65	+150	°C
$T_j$	junction temperature <sup>[1]</sup>	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the online MTF calculator.

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-mb)}$	transient thermal impedance from junction to mounting base	$T_{case} = 85\text{ °C}; P_L = 400\text{ W}$		
		$t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.11	K/W
		$t_p = 200\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.13	K/W
		$t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.15	K/W
		$t_p = 500\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.17	K/W
		$t_p = 1\text{ ms}; \delta = 10\text{ }\%$	0.18	K/W
		$t_p = 100\text{ }\mu\text{s}; \delta = 20\text{ }\%$	0.15	K/W

## 6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 4.5\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 450\text{ mA}$	1.5	2	3.1	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	4	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	85	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	400	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 450\text{ mA}$	-	4.2	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 15.75\text{ A}$	-	0.026	-	$\Omega$

Table 7. RF characteristics

Test signal: pulsed RF;  $t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$ ; RF performance at  $V_{DS} = 32\text{ V}; I_{Dq} = 400\text{ mA}; T_{case} = 25\text{ °C}$ ; unless otherwise specified, in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_L = 425\text{ W}$	10	11	-	dB
$\eta_D$	drain efficiency	$P_L = 425\text{ W}$	40	43	-	%
$RL_{in}$	input return loss	$P_L = 425\text{ W}$	-	-6	-	dB
$P_{droop(pulse)}$	pulse droop power	$P_L = 425\text{ W}$	-	0.15	0.50	dB
$t_r$	rise time	$P_L = 425\text{ W}$	-	6	50	ns
$t_f$	fall time	$P_L = 425\text{ W}$	-	6	50	ns
$P_{L(2dB)}$	output power at 2 dB gain compression		400	-	-	W

**7. Test information**

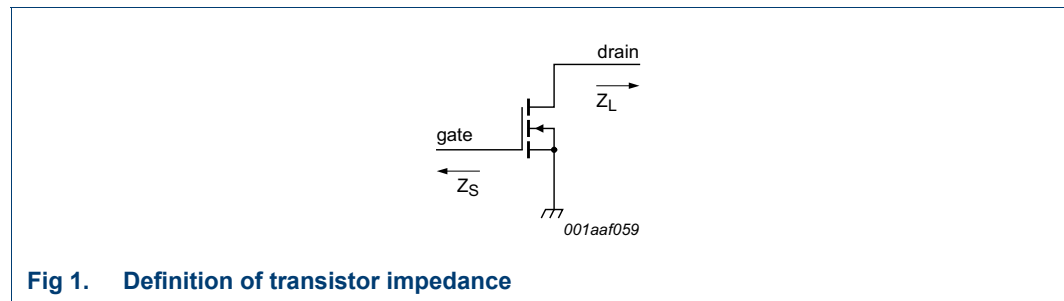
**7.1 Ruggedness in class-AB operation**

The BLS9G3135L-400 and BLS9G3135LS-400 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS} = 32\text{ V}$ ;  $I_{DQ} = 400\text{ mA}$ ;  $P_L = 400\text{ W}$ ;  $t_p = 300\text{ }\mu\text{s}$ ;  $\delta = 10\text{ }\%$ .

**7.2 Impedance information**

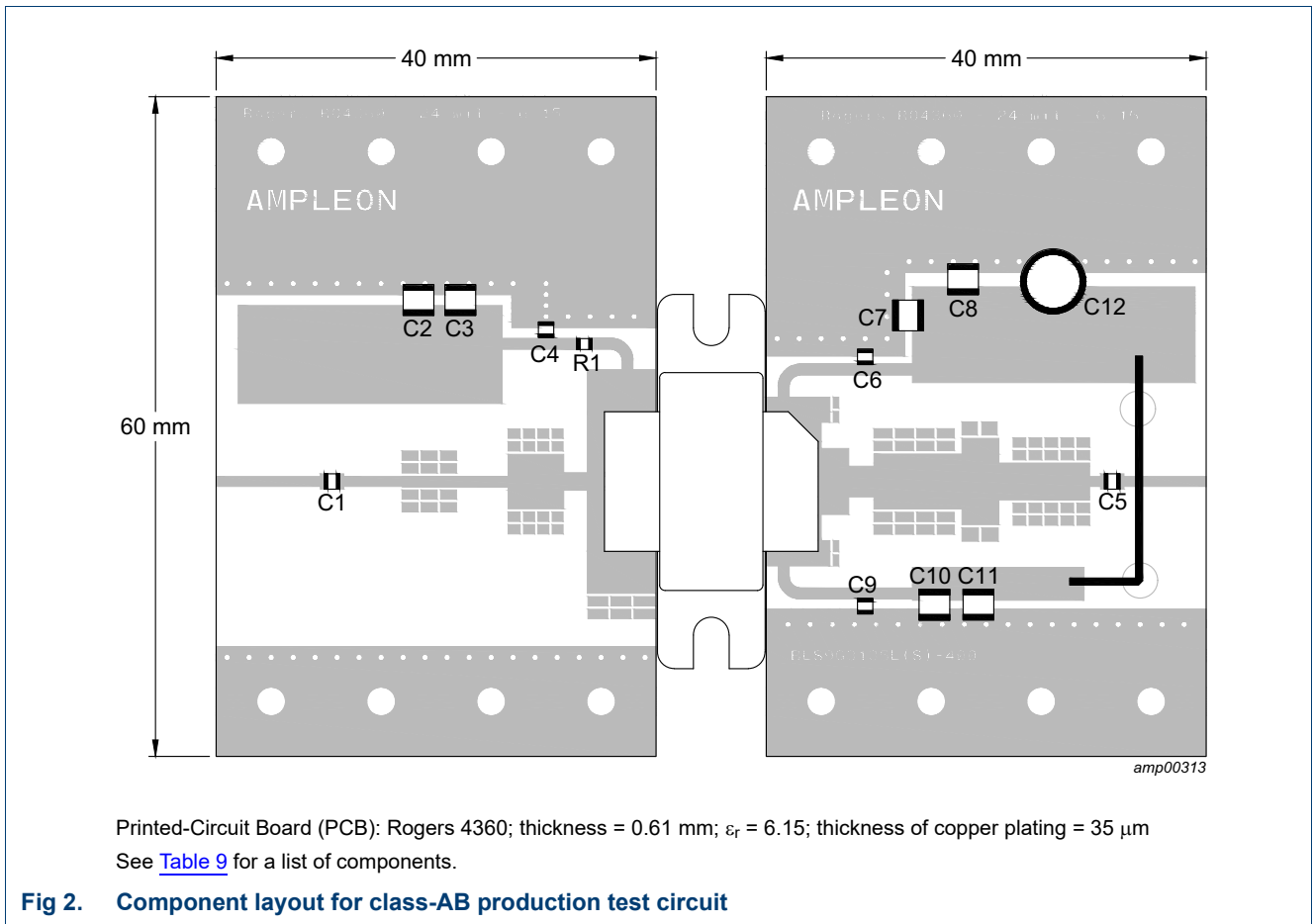
**Table 8. Typical impedance**

<b>f</b> <b>(GHz)</b>	<b>Z<sub>S</sub></b> <b>(<math>\Omega</math>)</b>	<b>Z<sub>L</sub></b> <b>(<math>\Omega</math>)</b>
3.1	4.122 – j8.679	1.206 – j4.231
3.2	6.215 – j3.927	1.593 – j4.396
3.3	4.334 – j3.313	1.885 – j4.262
3.4	2.085 – j2.187	2.473 – j3.915
3.5	1.976 – j2.700	2.313 – j3.180



**Fig 1. Definition of transistor impedance**

7.3 Test circuit information

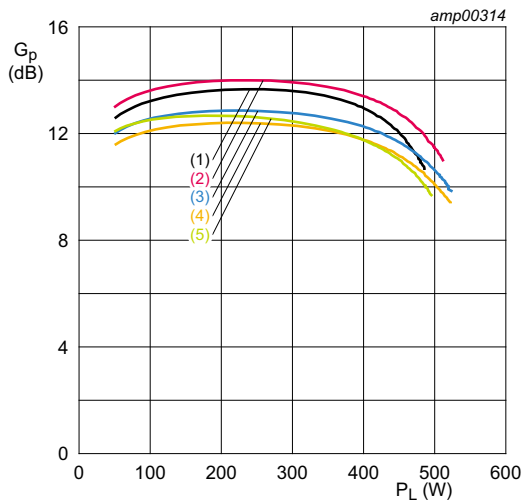


**Table 9. List of components**

For test circuit see [Figure 2](#).

Component	Description	Value	Remarks
C1, C4	multilayer ceramic chip capacitor	10 pF	ATC100A
C2	multilayer ceramic chip capacitor	4.7 $\mu\text{F}$	
C3, C8, C10	multilayer ceramic chip capacitor	1 nF	ATC100B
C5, C6, C9	multilayer ceramic chip capacitor	10 pF	ATC800A
C7, C11	multilayer ceramic chip capacitor	10 $\mu\text{F}$ , 50 V	Murata: GRM55DR61H106KA88L
C12	electrolytic capacitor	220 $\mu\text{F}$ , 63 V	
R1	resistor	5 $\Omega$	SMD 0603

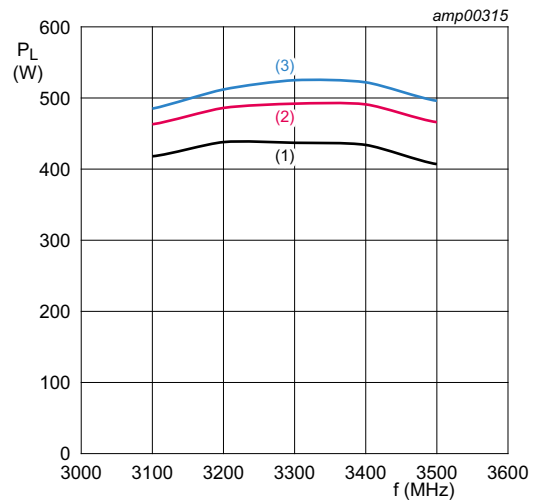
7.4 Graphical data



$V_{DS} = 32\text{ V}; I_{Dq} = 400\text{ mA}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ \%}$ .

- (1)  $f = 3100\text{ MHz}$
- (2)  $f = 3200\text{ MHz}$
- (3)  $f = 3300\text{ MHz}$
- (4)  $f = 3400\text{ MHz}$
- (5)  $f = 3500\text{ MHz}$

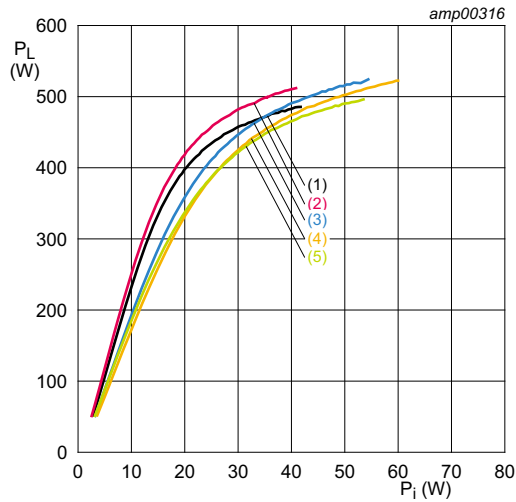
Fig 3. Power gain as a function of output power; typical values



$V_{DS} = 32\text{ V}; I_{Dq} = 400\text{ mA}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ \%}$ .

- (1)  $P_{1dB}$
- (2)  $P_{2dB}$
- (3)  $P_{3dB}$

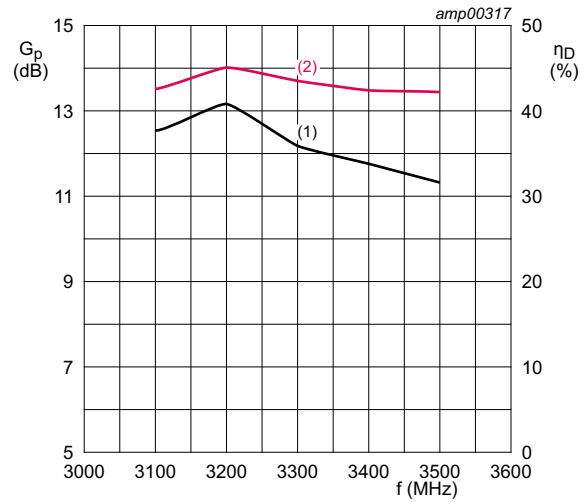
Fig 4. Output power as a function of frequency; typical values



$V_{DS} = 32\text{ V}; I_{Dq} = 400\text{ mA}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$ .

- (1)  $f = 3100\text{ MHz}$
- (2)  $f = 3200\text{ MHz}$
- (3)  $f = 3300\text{ MHz}$
- (4)  $f = 3400\text{ MHz}$
- (5)  $f = 3500\text{ MHz}$

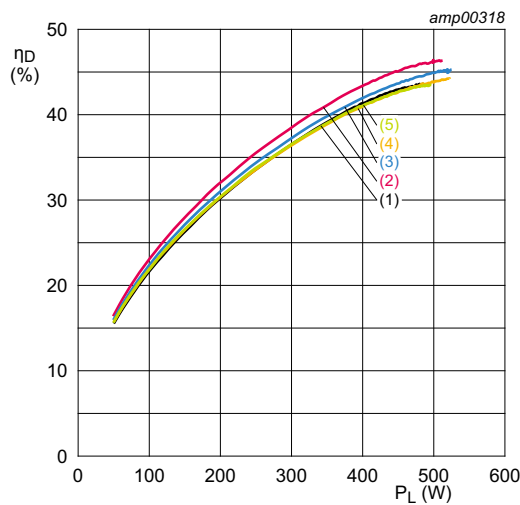
**Fig 5. Output power as a function of input power; typical values**



$V_{DS} = 32\text{ V}; I_{Dq} = 400\text{ mA}; P_L = 425\text{ W}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$ .

- (1)  $G_p$
- (2)  $\eta_D$

**Fig 6. Power gain and drain efficiency as function of frequency; typical values**



$V_{DS} = 32\text{ V}; I_{Dq} = 400\text{ mA}; t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$ .

- (1)  $f = 3100\text{ MHz}$
- (2)  $f = 3200\text{ MHz}$
- (3)  $f = 3300\text{ MHz}$
- (4)  $f = 3400\text{ MHz}$
- (5)  $f = 3500\text{ MHz}$

**Fig 7. Drain efficiency as a function of output power; typical values**

8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads

SOT502A

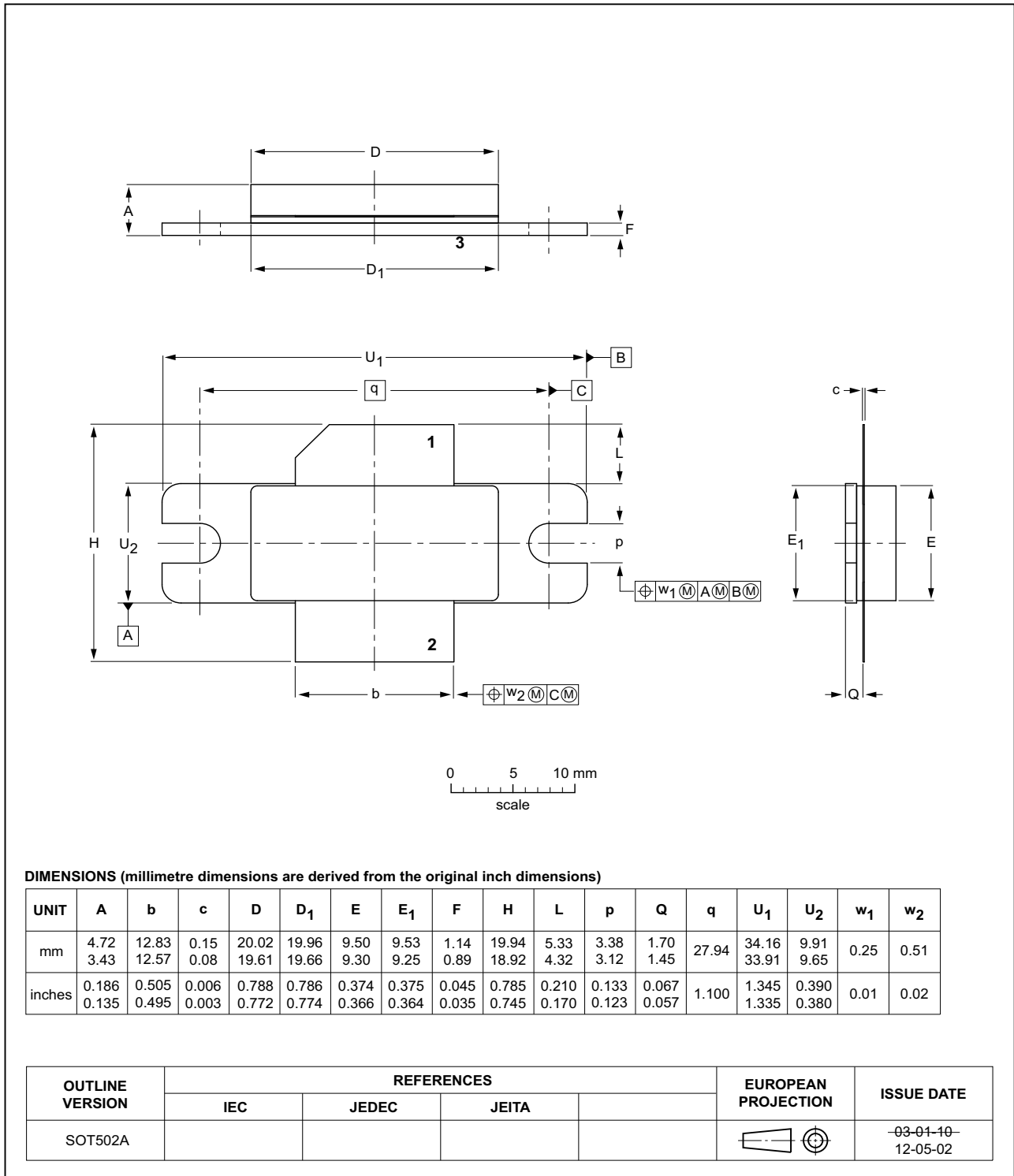


Fig 8. Package outline SOT502A



Earless flanged ceramic package; 2 leads

SOT502B

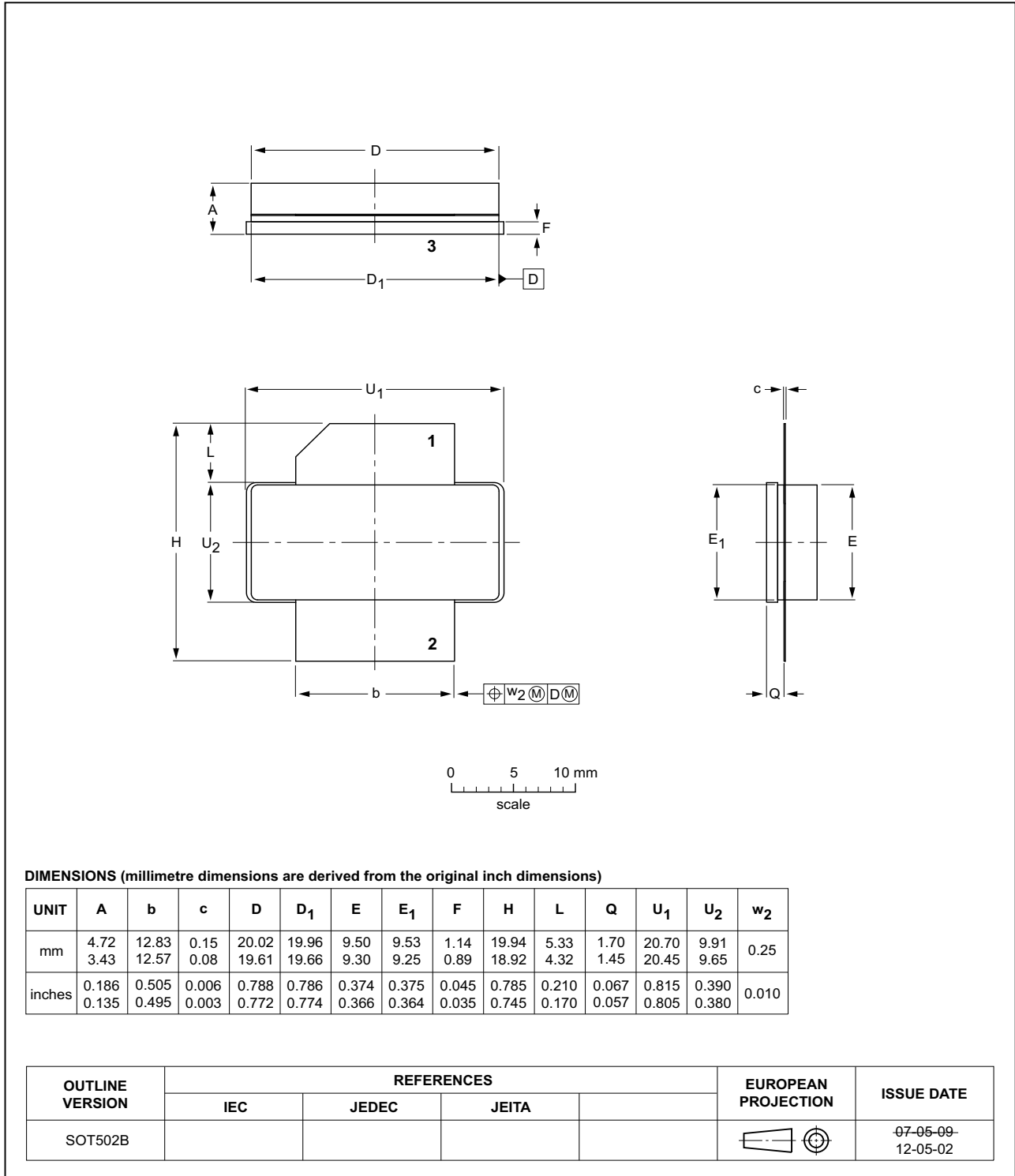


Fig 9. Package outline SOT502B

## 9. Handling information

**CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

**Table 10. ESD sensitivity**

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A <a href="#">[1]</a>
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 <a href="#">[2]</a>

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

## 10. Abbreviations

**Table 11. Abbreviations**

Acronym	Description
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
S-band	Short wave Band
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

## 11. Revision history

**Table 12. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLS9G3135L-400_LS-400 v.1	20170406	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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