

#### Single String Linear constant current LED Controller with Integrated DC/DC Boost Controller

##### Features

- Integrated Boost Controller
- Drives external N-Ch MOSFETS
- Over-Temperature Fault Detection
- 8-bit DAC for peak current control
- PWM Input for Dimming Duty Cycle
- Linear current control for ripple-free LED current regulation
- 8-bit Efficiency Optimizer Minimizes Power Use
- $\pm 3\%$  Current Accuracy
- I<sup>2</sup>C Serial Interface (use Optional)
- 32 Bytes Free RAM, 32 Bytes Free EEPROM
- 24-Pin QFN Package
- -40°C To +105°C Operating Temperature Range

##### Typical Applications

- General and Architectural Lamps
- Down Lights and Recessed Lights
- PAR Lamps
- DC Input LED lamps

# 1. Introduction

The MSL2010 LED string driver features a constant off-time Boost Controller and provides very accurate, no ripple, linear controlled string current. The Atmel patent-pending Efficiency Optimizer (EO) controls the switch-mode converter output, optimizing the output voltage to achieve maximum power efficiency. Both the switching and linear controllers drive external MOSFETs to provide flexibility over a wide range of power levels (LED currents and voltages) and extremely low LED ripple current.

The MSL2010 operates from a 9.5V to 15V power supply. The Boost controller voltage regulation loop uses a constant off-time control algorithm to achieve stable control with good transient behavior. For flexibility of design, off-time is set with an external resistor. External loop compensation offers additional flexibility for the Boost Controller.

An I<sup>2</sup>C interface provides access to the control registers, and to 32 bytes of RAM. Integrated non-volatile EEPROM memory, also accessed through the I<sup>2</sup>C serial interface, allows configuration at final test in the case that the factory default settings must be modified.

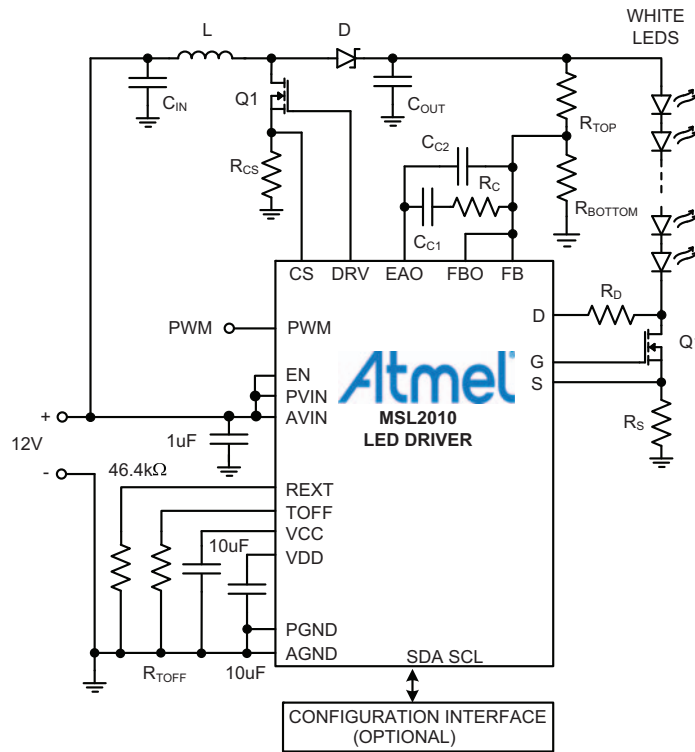
The MSL2010 is available in the space-saving 24-pin 4x4mm QFN package and operates over the extended -40°C to 105°C operating range.

# 2. Ordering Information

| Ordering code | Description                                 | Package <sup>(1)</sup> |
|---------------|---|------------------------|
| MSL2010       | One String LED Driver with DC-DC Controller | 4 x 4mm 24-pin QFN     |

Note: 1. Lead-Free, Halogen-Free, RoHS Compliant Package

# 3. Application Circuit



## 4. Absolute Maximum Ratings

| Voltage with respect to AGND              |  |                   |
|---|--|-------------------|
| AVIN, PVIN, EN                            |  | -0.3V to +16.5V   |
| VCC, PWM, FLTB, SDA, SCL, TOFF, REXT, FBO |  | -0.3V to +5.5V    |
| VDD                                       |  | -0.3V to +2.75V   |
| CS, S                                     |  | -0.3V to VDD+0.3V |
| D   |  | -0.3V to +22V     |
| G, DRV                                    |  | -0.3V to VIN+0.3V |
| PGND, AGND                                |  | -0.3V to +0.3V    |

| Current (into pin)             |  |             |
|--------------------------------|--|-------------|
| AVIN, PVIN, DRV, G (average)   |  | 100mA       |
| PVIN (peak, $\leq 1\%$ duty)   |  | 1A          |
| DRV, G (peak, $\leq 1\%$ duty) |  | $\pm 1$ A   |
| PGND (peak, $\leq 1\%$ duty)   |  | -1A         |
| AGND, PGND (average)           |  | -100mA      |
| All other pins                 |  | $\pm 10$ mA |

| Continuous Power Dissipation at 70°C                      |  |        |
|---|--|--------|
| 24-Pin 4mm x 4mm VQFN (derate 21.8mW/°C above TA = +70°C) |  | 1200mW |

|                                     |  |                 |
|-------------------------------------|--|-----------------|
| Ambient Operating Temperature Range |  | -40°C to +105°C |
| Junction Temperature                |  | +125°C          |
| Storage Temperature Range           |  | -65°C to +125°C |
| Lead Soldering Temperature, 10s     |  | +300°C          |

## 5. Electrical Characteristics

AVIN = PVIN = 12V,  $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ , Typical Operating Circuit, unless otherwise noted.  
Typical values at  $T_A = +25^{\circ}\text{C}$ .

Table 5-1. DC electrical characteristics

| Parameter  | Conditions   | Min.                | Typ. | Max.                | Unit                    |
|--|--|---------------------|------|---------------------|-------------------------|
| AVIN, PVIN Operating Supply Voltage                        |  | 9.5                 | 12   | 15                  | V                       |
| AVIN Operating Supply Current                              | LEDs on at PWM = 100%, serial interface idle                             |                     | 10   |                     | mA                      |
| AVIN Disable Supply Current                                | $V_{EN} = 0$ , all digital inputs = 0                                    |                     |      | 5                   | $\mu\text{A}$           |
| VCC Regulation Voltage                                     | $I_{VCC} = 10\text{mA}_{\text{peak}}^{(1)}$                              | 4.5                 | 5    | 5.5                 | V                       |
| VDD Regulation Voltage                                     | $I_{VDD} = 10\text{mA}_{\text{peak}}^{(1)}$                              | 2.25                | 2.5  | 2.75                | V                       |
| PWM, SCL, SDA Input High Voltage                           |  | $0.7 \cdot V_{VDD}$ |      |                     | V                       |
| PWM, SCL, SDA Input Low Voltage                            |  |                     |      | $0.3 \cdot V_{VDD}$ | V                       |
| EN Input High Voltage                                      |  | 2                   |      |                     | V                       |
| EN Input Low Voltage                                       |  |                     |      | 0.5                 | V                       |
| EN Input Hysteresis  |  |                     | 100  |                     | mV                      |
| SDA, FLTB Output Low Voltage                               | Sinking 6mA  |                     |      | 0.3                 | V                       |
| SCL, SDA, PWM, FLTB leakage current                        |  | -5                  |      | 5                   | $\mu\text{A}$           |
| S Current Sense Regulation Voltage                         | MREF = 0x64  | 194                 | 200  | 206                 | mV                      |
| S Current Sense Regulation Voltage Accuracy                | Main string at 100% duty cycle, $T_A = 25^{\circ}\text{C}$ , MREF = 0x64 | -3                  |      | +3                  | %                       |
| S Current Sense Regulation Voltage Temperature Coefficient |  |                     | -220 |                     | ppm/ $^{\circ}\text{C}$ |
| G Maximum Output Voltage                                   |  | $AVIN - 3.5$        |      | $AVIN - 2.0$        | V                       |
| D Regulation Threshold                                     | EOCTRL = 0xE5  | 0.9                 | 1    | 1.1                 | V                       |
| CS Current Sense Regulation Voltage                        | CAREF = 0x64   |                     | 200  |                     | mV                      |
| EA Unity Gain Bandwidth                                    |  |                     | 7    |                     | MHz                     |
| EA Open Loop Gain  |  |                     | 100  |                     | dB                      |
| DRV Impedance  | $V_{DRV} = 12\text{V}$ , $I_{DRV} = 20\text{mA}$                         |                     | 5.6  | 9                   | $\Omega$                |
|  | $V_{DRV} = 0\text{V}$ , $I_{DRV} = -20\text{mA}$                         |                     | 5.6  | 9                   | $\Omega$                |
| FBO Full Scale Current                                     |  | 170                 | 255  | 340                 | $\mu\text{A}$           |
| FBO LSB Current  |  |                     | 1.0  |                     | $\mu\text{A}$           |
| Thermal Shutdown Temperature                               | Temperature rising   |                     | 133  |                     | $^{\circ}\text{C}$      |
| Thermal Shutdown Hysteresis                                |  |                     | 15   |                     | $^{\circ}\text{C}$      |

Note: 1. Additional decoupling may be required when pulling current from VCC and/or VDD in noisy environments

**Table 5-2. AC electrical characteristics**

| Parameter                 | Conditions               | Min. | Typ. | Max.   | Unit    |
|---------------------------|--------------------------|------|------|--------|---------|
| DRV $t_{OFF}$ timing      | $R_{TOFF} = 46.5k\Omega$ |      | 0.5  |        | $\mu s$ |
| PWM Input Frequency       | (1)                      | 60   |      | 10,000 | Hz      |
| PWM Duty Cycle            |                          | 1    |      | 100    | %       |
| PWM Duty Cycle Resolution |                          |      | 0.4  |        | %       |

Note: 1. 2 $\mu s$  minimum on time, 0% duty cycle is supported. PWM between 0% and 1% not guaranteed

**Table 5-3. I<sup>2</sup>C switching characteristics**

| Parameter                                | Symbol        | Conditions | Min. | Typ. | Max.  | Unit    |
|--|---------------|------------|------|------|-------|---------|
| SCL Clock Frequency                      |               | (1)        | 0.05 |      | 1,000 | kHz     |
| STOP to START Condition Bus Free Time    | $t_{BUF}$     |            | 0.5  |      |       | $\mu s$ |
| Repeated START condition Hold Time       | $t_{HD:STA}$  |            | 0.26 |      |       | $\mu s$ |
| Repeated START condition Setup Time      | $t_{SU:STA}$  |            | 0.26 |      |       | $\mu s$ |
| STOP Condition Setup Time                | $t_{SU:STOP}$ |            | 0.26 |      |       | $\mu s$ |
| SDA Data Hold Time                       | $t_{HD:DAT}$  |            | 5    |      |       | ns      |
| SDA Data Valid Acknowledge Time          |               | (2)        | 0.05 |      | 0.55  | $\mu s$ |
| SDA Data Valid Time                      |               | (3)        | 0.05 |      | 0.55  | $\mu s$ |
| SDA Data Set-Up Time                     | $t_{SU:DAT}$  |            | 100  |      |       | ns      |
| SCL Clock Low Period                     | $t_{LOW}$     |            | 0.5  |      |       | $\mu s$ |
| SCL Clock High Period                    | $t_{HIGH}$    |            | 0.26 |      |       | $\mu s$ |
| SDA, SCL Fall Time                       | $t_F$         | (4), (5)   |      |      | 120   | ns      |
| SDA, SCL Rise Time                       | $t_R$         |            |      |      | 120   | ns      |
| SDA, SCL Input Suppression Filter Period |               | (6)        |      | 50   |       | ns      |
| Bus Timeout                              | $t_{TIMEOUT}$ | (1)        |      | 25   |       | ms      |

- Notes:
1. Minimum SCL clock frequency is limited by the bus timeout feature, which resets the serial bus interface when either SDA or SCL is held low for  $t_{TIMEOUT}$ .
  2. SDA Data Valid Acknowledge Time is SCL LOW to SDA (out) LOW acknowledge time.
  3. SDA Data Valid Time is minimum SDA output data-valid time following SCL LOW transition.
  4. A master device must internally provide an SDA hold time of at least 300ns to ensure an SCL low state.
  5. The maximum SDA and SCL rise times is 300ns. The maximum SDA fall time is 250ns. This allows series protection resistors to be connected between SDA and SCL inputs and the SDA/SCL bus lines without exceeding the maximum allowable rise time.
  6. Includes input filters on SDA and SCL that suppress noise less than 50ns.

## 6. Typical Operating Characteristics

Figure 6-1. Istr (String Current) rising.

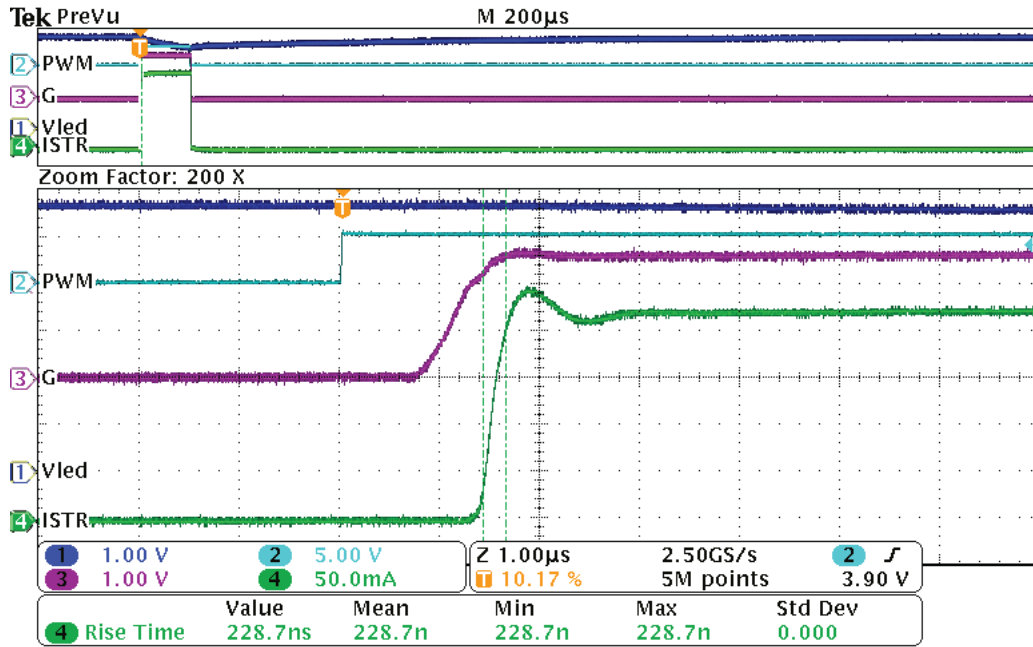


Figure 6-2. Istr (String Current) falling.

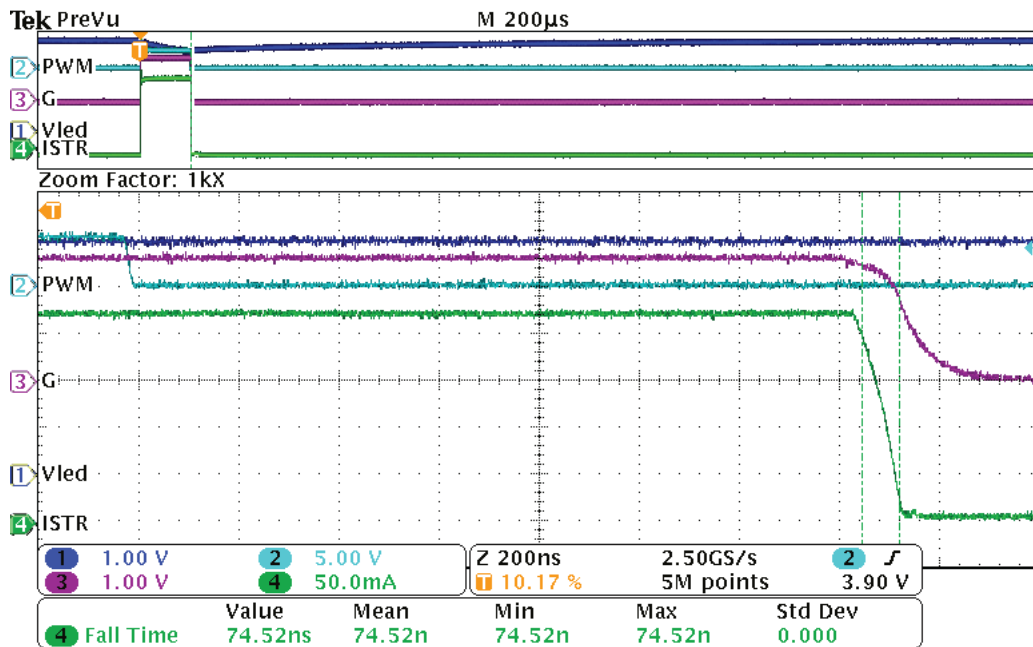


Figure 6-3. Start-up behavior, PWM = 10% duty cycle (Test conditions).

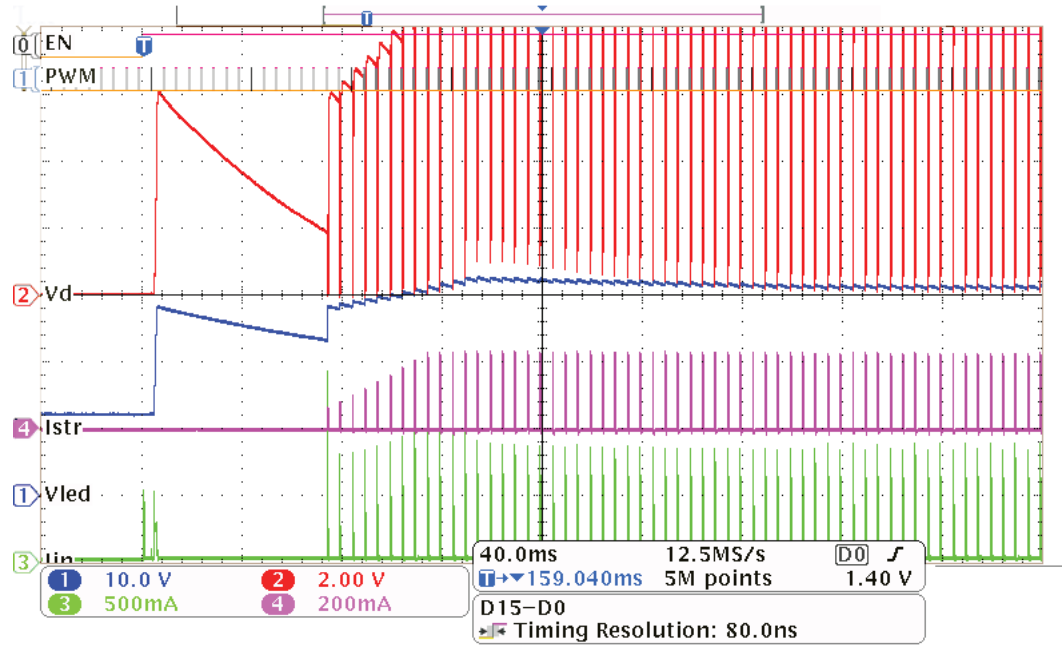


Figure 6-4. Start-up behavior, PWM = 10% (Zoom) duty cycle (Test conditions).

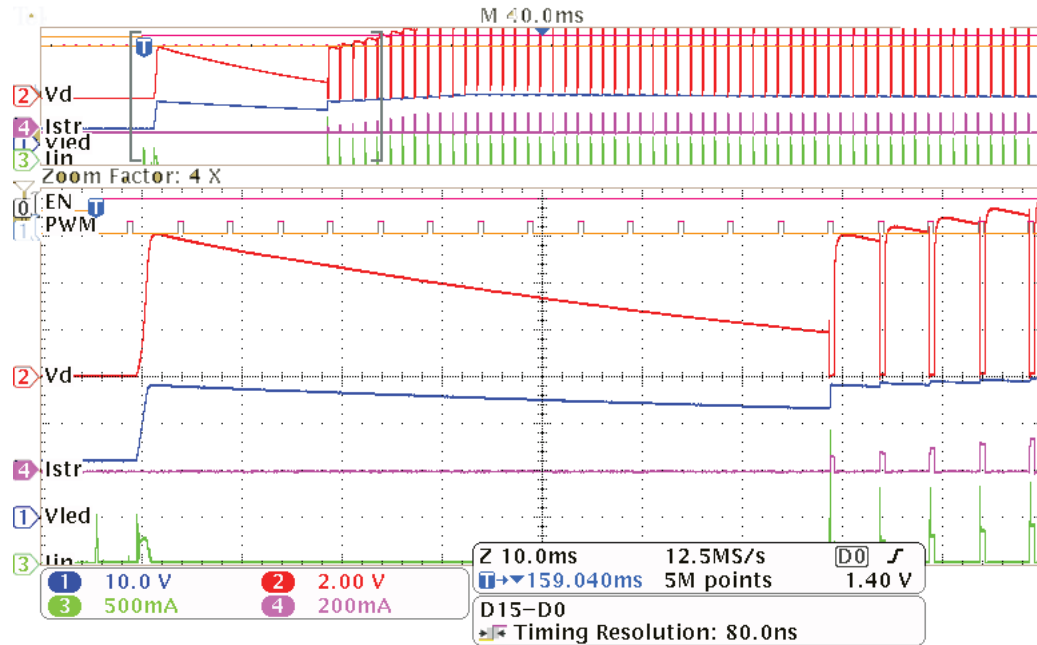


Figure 6-5. Start-up behavior, PWM = 90% duty cycle (Test conditions).

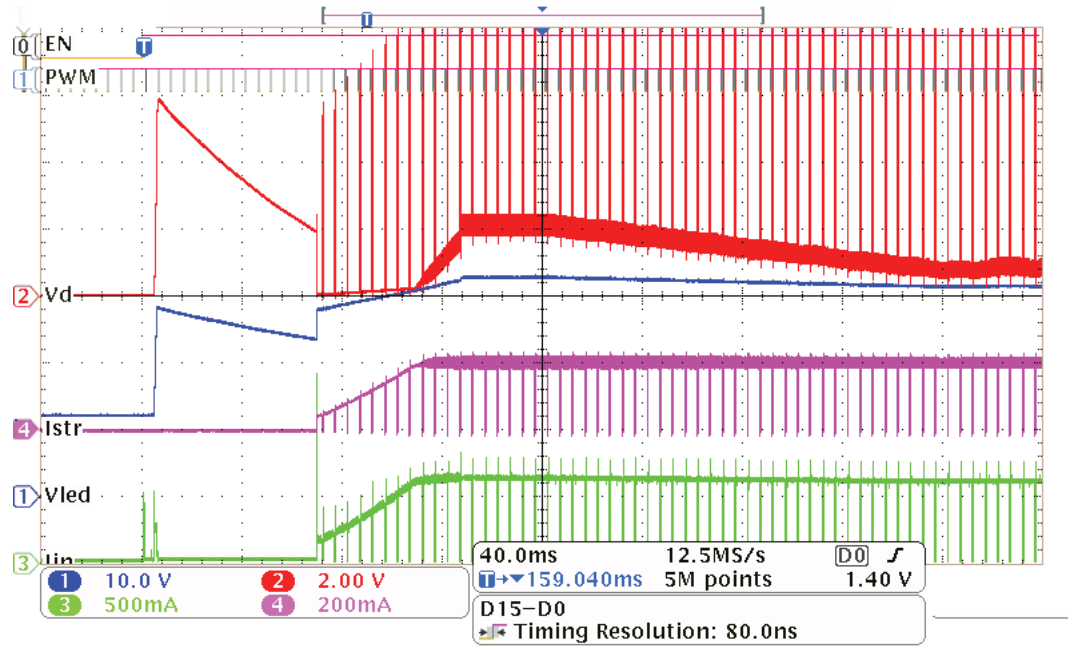


Figure 6-6. Start-up behavior,, PWM = 90%(zoom) duty cycle (Test conditions).

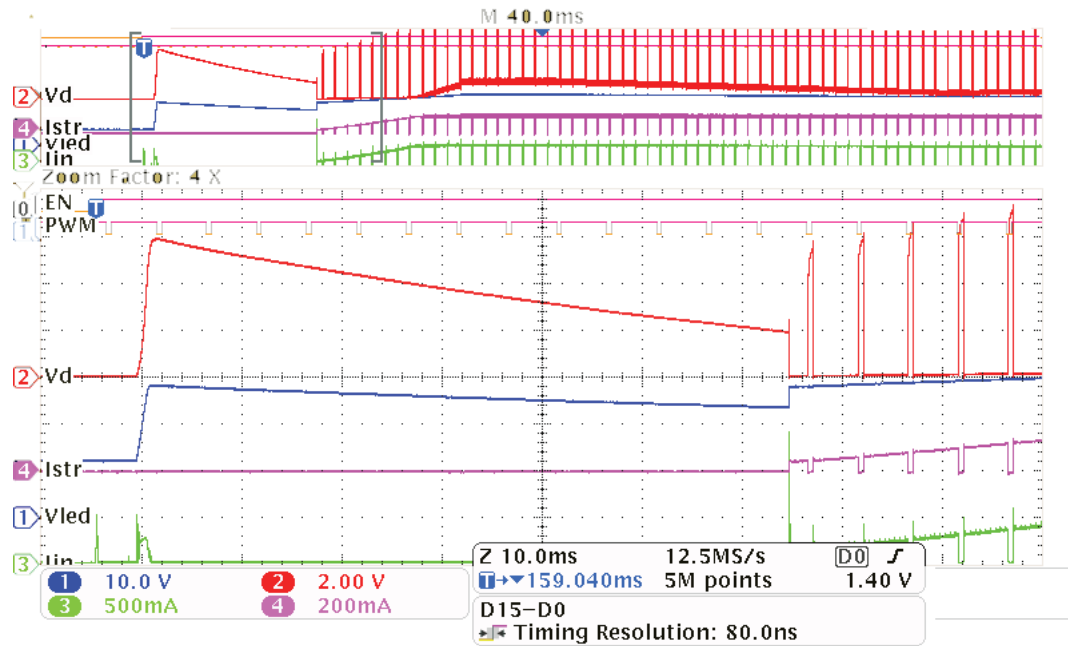




Figure 6-7. Operating current vs. input voltage

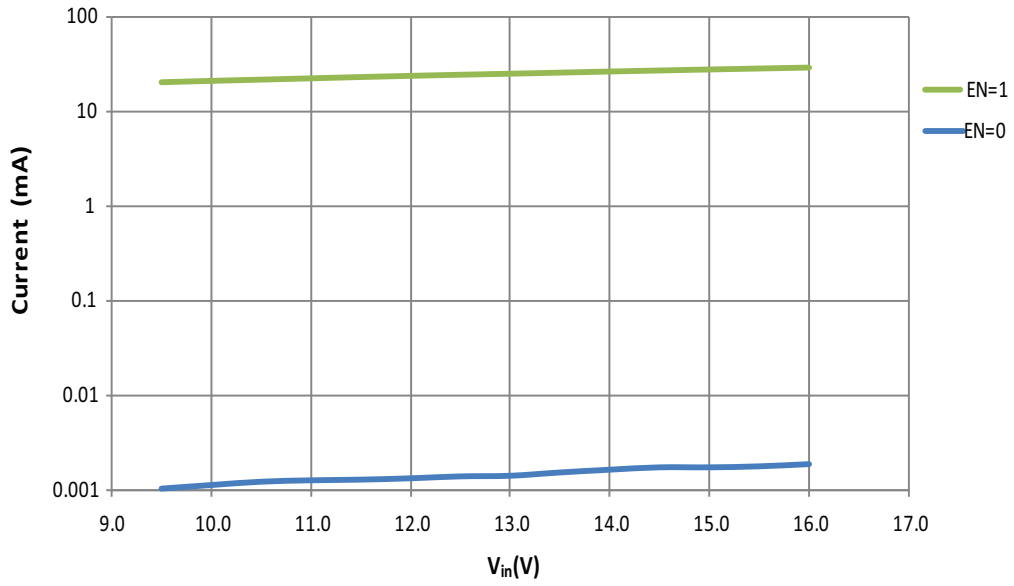


Figure 6-8. V<sub>CC</sub> and V<sub>DD</sub> regulation

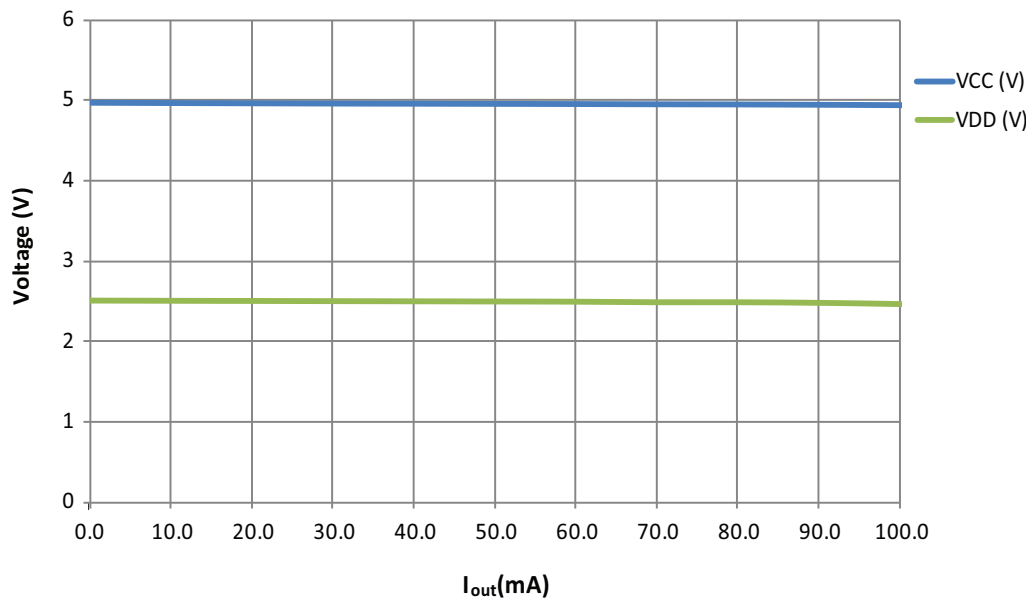
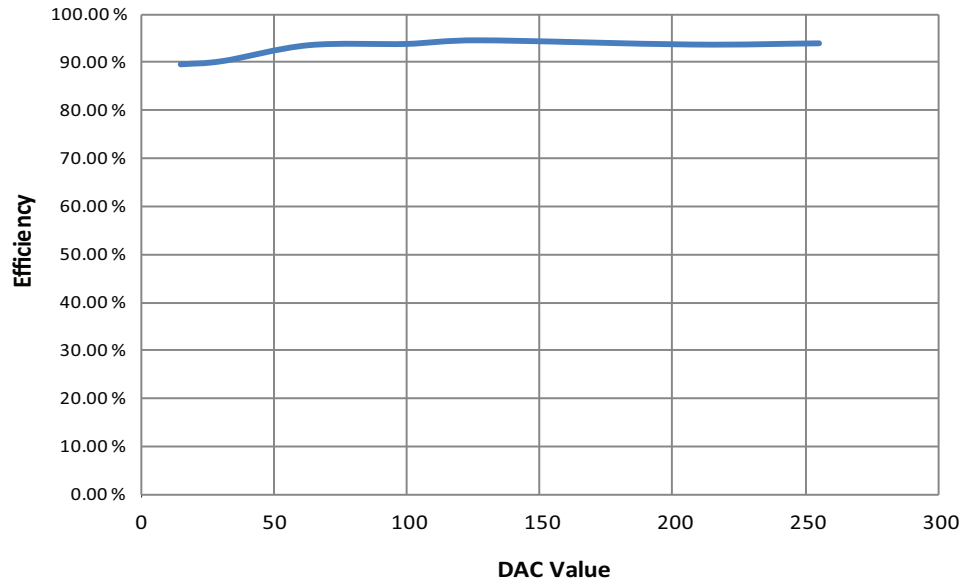
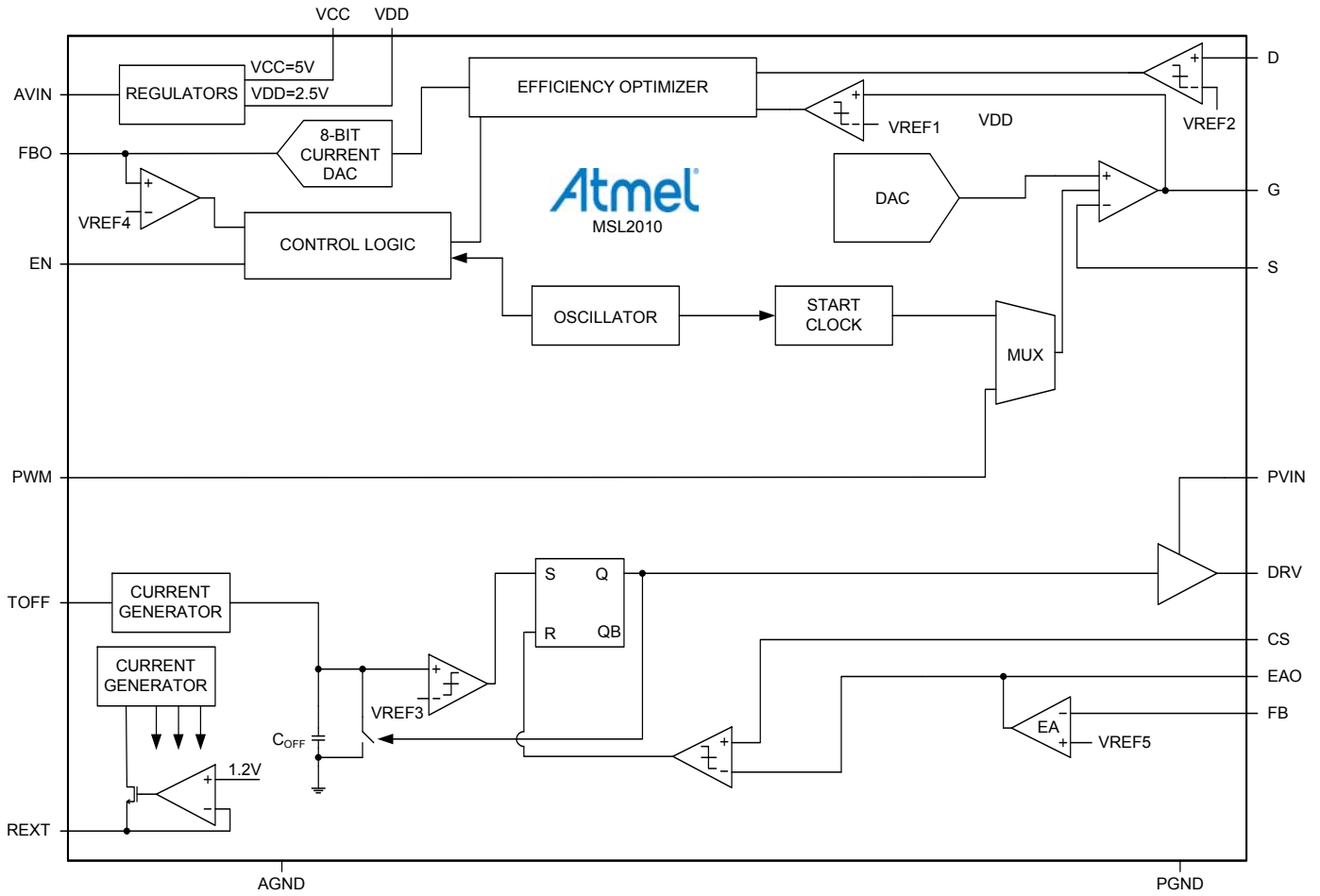


Figure 6-9. Efficiency vs DAC value



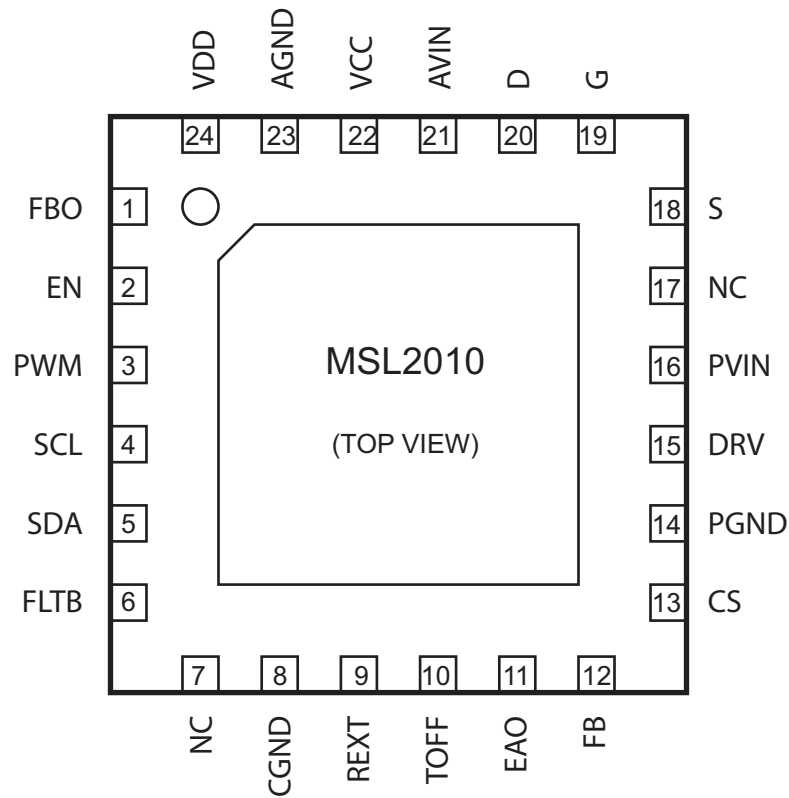
## 7. Block Diagram

Figure 7-1. MSL2010 block diagram



## 8. Pinout and Pin Description

### 8.1 Pinout MSL2010



### 8.2 Pin Descriptions

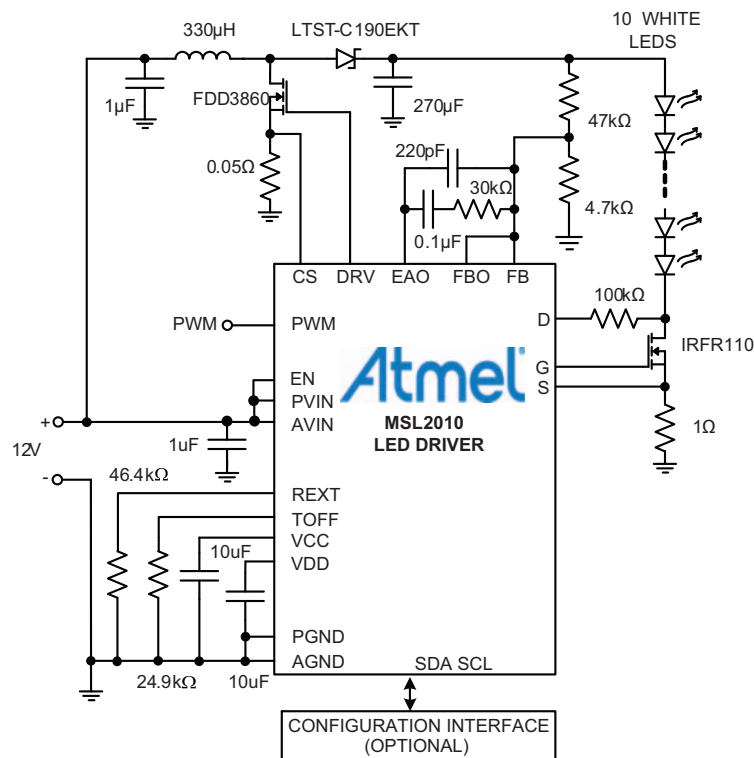
| Name        | Pin   | Description  |
|-------------|-------|--|
| <b>FBO</b>  | 1     | <b>Feedback Output</b><br>Feedback output from Efficiency Optimizer. Connect FBO to the LED power supply regulation feedback node to control $V_{LED}$ . When unused connect FBO to VCC.                           |
| <b>EN</b>   | 2     | <b>Enable Input (Active High)</b><br>Drive EN high to turn on the MSL2010, drive EN low to turn it off. For automatic start-up connect EN to AVIN.   |
| <b>PWM</b>  | 3     | <b>PWM Dimming Input</b><br>Drive PWM with a pulse-width modulated signal to control LED brightness. See <a href="#">“PWM and LED Brightness” on page 17</a> for details.  |
| <b>SCL</b>  | 4     | <b>Serial Clock Input</b><br>SCL is the I <sup>2</sup> C serial interface clock input. See <a href="#">“I<sup>2</sup>C Serial Interface” on page 21</a> details.   |
| <b>SDA</b>  | 5     | <b>Serial Data Input/Output</b><br>SDA is the I <sup>2</sup> C serial interface data I/O. See <a href="#">“I<sup>2</sup>C Serial Interface” on page 21</a> details.  |
| <b>FLTB</b> | 6     | <b>Fault Output</b><br>Open Collector FLTB pulls low when an overtemperature is detected (die temperature $\geq 147^{\circ}\text{C}$ ). FLTB releases when the die temperature falls below $127^{\circ}\text{C}$ . |
| <b>NC</b>   | 7, 17 | <b>No Internal Connection</b>  |

| Name | Pin | Description   |
|------|-----|---|
| CGND | 8   | <b>Connect to Ground</b><br>Connect CGND to AGND  |
| REXT | 9   | <b>External Resistor</b><br>Connect a 46.4k $\Omega$ , 1% resistor from REXT to AGND.   |
| TOFF | 10  | <b>Off-Time Set Input</b><br>A resistor from TOFF to AGND controls the constant off time for the Boost converter, where $R_{TOFF} = t_{OFF} * (90.9 \times 10^9)$ , with $t_{OFF}$ in seconds and $R_{TOFF}$ in Ohms. For example, an off time of 4.4 $\mu$ s results in a resistor value of 402k $\Omega$ (to the nearest 1% value). |
| EAO  | 11  | Error Amp Out<br>Output of the switch-mode error amplifier. Connect the compensation network between EAO and FB.  |
| FB   | 12  | <b>Feedback Input for Boost Regulator</b><br>Connect FB to the middle node of the Boost regulator voltage setting resistor divider. Also, connect FBO to FB to allow the MSL2010 to optimize $V_{LED}$ .  |
| CS   | 13  | <b>Current Sense Input for the Boost Converter</b><br>Connect CS to the external current sense resistor of the Boost regulator. The current sense threshold is 200mV. For more information see the section "Boost Reference Voltage register (CSREF, 0x21)" on page 20.   |
| PGND | 14  | Power Ground<br>PGND is the ground connection for the FET gate drivers. Connect PGND to AGND close to the MSL2010.  |
| DRV  | 15  | <b>Gate Drive for Boost Regulator MOSFET</b><br>Connect DRV to the gate of the Boost regulator power MOSFET.  |
| PVIN | 16  | <b>Power Voltage Input</b><br>PVIN powers DRV, the Boost regulator FET gate driver. Connect PVIN to a power supply of 10V to 15V. Bypass PVIN to PGND with a 1.0 $\mu$ F or greater capacitor.  |
| S    | 18  | <b>Source Sense Input for LED String Drive MOSFET</b><br>Connect S to the source of the LED string drive external MOSFET, and to the current sense resistor for the LED string. The current sense threshold is 200mV. For more information see the section "LED String Reference Voltage register (SREF, 0x20)" on page 20.           |
| G    | 19  | <b>Gate Output for LED String MOSFET</b><br>Connect G to the gate of the LED string drive external MOSFET. Minimum on-time is 2 $\mu$ s.  |
| D    | 20  | <b>Drain Output for LED String MOSFET</b><br>Connect D to the drain of the LED string drive external MOSFET.  |
| AVIN | 21  | <b>Analog Voltage Input (12V)</b><br>AVIN is the power input to the MSL2010. Bypass AVIN to AGND with a 1.0 $\mu$ F or greater capacitor placed close to AVIN.  |
| VCC  | 22  | 5V Internal Voltage<br>Connect 10 $\mu$ F bypass capacitor from VCC to AGND.  |
| AGND | 23  | Analog Ground<br>Connect AGND to system ground.   |
| VDD  | 24  | <b>2.5V Internal Voltage</b><br>Connect 10 $\mu$ F bypass capacitor from VDD to AGND.   |
| EP   | EP  | <b>Exposed Pad</b><br>EP is the main thermal path for heat to escape the die. Connect EP to a large copper plane connected to PGND and AGND.  |

## 9. Typical Application Circuit

MSL2010 Boost Switcher and Linear Driver, Driving 10 White LEDs.

Figure 9-1. Typical application circuit



## 10. Detailed Description

The MSL2010 drives one LED string, and includes a Boost Regulator Controller to generate  $V_{LED}$ , the string voltage, from a low voltage input. An Efficiency Optimizer (EO) algorithm regulates  $V_{LED}$  to the minimum required to keep the LEDs in current regulation, minimizing power loss across the external string drive MOSFET. A PWM input accepts 1% to 100% duty cycle signal of 60Hz to 10kHz. The LED PWM output dimming duty cycle and frequency equal the PWM input duty cycle and frequency, with a 2μs minimum on time. LEDs are driven by a linear driver.

## 11. Fault Conditions

Over Temperature Protection shuts down the device when the die temperature is above 133°C. The device turns back on when the die temperature falls below 118°C, as if EN is taken from low to high.

## 12. Applications Information

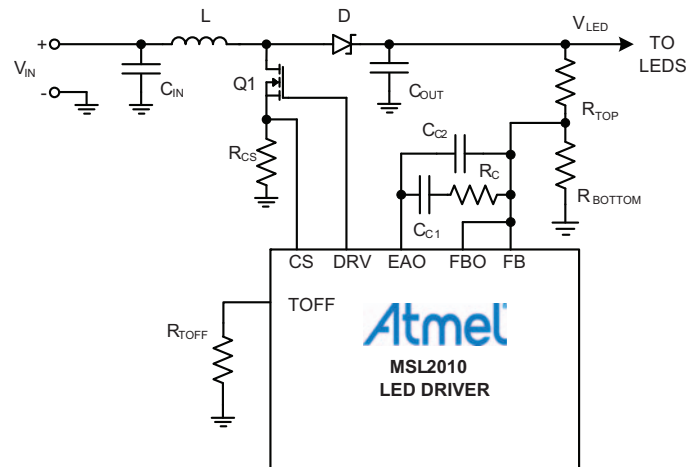
### 12.1 Turn-On Sequence

When EN is taken high, the MSL2010 waits for 6ms, then optimizes  $V_{LED}$ , the LED string voltage, which typically takes about 250ms, then begins to drive the LEDs based on the PWM input.

## 12.2 The Boost Regulator

MSL2010 includes a Constant Off-Time DC/DC Boost Controller to generate  $V_{LED}$ , the voltage for the LED string. The Boost components are shown in [Figure 12-1 on page 15](#), and include a voltage setting resistor divider, a MOSFET, a Schottky diode, a resistor to set the Off-Time, an Inductor, a current sense resistor, a Drain resistor, a few capacitors and a compensation network. The following sections discuss selecting these components.

**Figure 12-1. Boost Regulator Components**



### 12.2.1 Setting the Boost Output Voltage, $V_{LED}$

A resistor divider sets the nominal Boost output voltage,  $V_{LED}$ . Select the two feedback resistors by first determining the minimum output voltage using:

$$V_{OUT(MIN)} \leq (V_{fMIN}) * (N) + 0.2 \text{ V,}$$

where  $V_{fMIN}$  is the minimum LED forward voltage at the expected LED current, N is the number of LEDs in the string, and 0.2V is the minimum overhead required for the current sense resistor and the FET. Then determine the maximum output voltage using:

$$V_{OUT(MAX)} = (V_{fMAX}) * (N) + 1.2 \text{ V,}$$

where  $V_{fMAX}$  is the maximum LED forward voltage at the expected LED current, N is the number of LEDs in the string, and 1.2V is the maximum overhead required for the current sense resistor and the FET.

Determine the value for the upper voltage setting resistor using:

$$R_{TOP} = \frac{V_{OUT(MAX)} - V_{OUT(MIN)}}{340 \times 10^{-6}} \Omega,$$

where 340 $\mu$ A is the guaranteed maximum FBO current from the [“Electrical Characteristics” on page 4](#). Determine the lower resistor using:

$$R_{BOTTOM} = R_{TOP} * \frac{2.5}{V_{OUT(MIN)} - 2.5} \Omega,$$

where 2.5V is  $V_{FB}$ , the feedback regulation voltage of the FB input. The Efficiency Optimizer (EO) output, FBO, connects to FB and pulls current from the node to force the converter's output voltage up to the proper level to keep the LEDs in current regulation with the minimum power loss.

### 12.2.2 The Boost MOSFET and Schottky Diode

Output DRV drives the gate of an external N-Channel MOSFET at up to  $V_{PVIN} - 1.5V$ . Select a MOSFET with a maximum drain-source voltage of at least 1V above  $V_{OUT(MAX)}$  (from above), a low gate charge and low  $R_{DS(ON)}$ . Use a Schottky diode with a maximum reverse voltage of at least  $V_{OUT(MAX)}$ .

### 12.2.3 The Off-Time Resistor, $R_{TOFF}$

The Boost driver uses a constant off-time algorithm. The MOSFET turns off when  $V_{CS} = 0.2V$  ([Figure 12-1 on page 15](#)). Control off-time with external resistor  $R_{TOFF}$  using:

$$R_{TOFF} = t_{OFF} * (90.9 \times 10^9) \Omega,$$

where  $t_{OFF}$  is in seconds. For example, an off-time of 4.4 $\mu$ s results in a resistor value of 402k $\Omega$  (to the nearest 1% value).

### 12.2.4 Setting the Inductor Current with $R_{CS}$

The Boost inductor peak current regulates by way of the voltage at CS, the Boost MOSFET source resistor connection. Connect the current sense resistor  $R_{CS}$  from the MOSFET source to ground. The default feedback voltage for CS is 0.2V. Choose the current sense resistor using:

$$R_{CS} = \frac{0.2}{I_L} \Omega,$$

where  $I_L$  is the inductor peak current. For example, for 350mA  $I_L$ , use  $R_{CS}$  of 0.56 Ohms. The 0.2V in this equation is set in the Current Sense Reference Voltage (CSREF) register 0x21. The default value for CSREF is 0x64, which sets the feedback voltage to 0.2V. For information about CSREF see "[Boost Reference Voltage register \(CSREF, 0x21\)](#)" on [page 20](#).

### 12.2.5 Sizing The Inductor, L

Current increases through the inductor until the voltage at CS reaches 0.2V. The MOSFET then turns off for the off-time programmed by  $R_{TOFF}$  (above). Estimate the inductor value using:

$$L = \frac{v(t)}{\left(\frac{di(t)}{dt}\right)} H,$$

where  $v(t)$  = the acceptable ripple voltage of  $V_{LED}$ ,  $di(t)$  = acceptable peak to peak inductor ripple current, and  $dt$  = the off-time set by  $R_{TOFF}$ .

For example:

With an inductor ripple voltage of 0.5% of  $V_{OUT(MAX)}$  (from above),  $v(t) = 35.2 * (0.005) = 176mV$ .

With an average load current of 350mA and an inductor ripple current of 4%,  $di(t) = 0.35 * 0.04 = 0.014A$ .

And, with a  $t_{OFF}$  of 4.4 $\mu$ s, then:

$$L = \left(\frac{0.176}{\frac{0.014}{4.4 \times 10^{-6}}}\right) = 55 \mu H.$$



Assure that the inductor saturation current rating is greater than  $I_L$ , the peak inductor current from the  $R_{CS}$  equation above.

### 12.2.6 The Drain Resistor, $R_D$

The drain resistor,  $R_D$  in [Figure 12-1 on page 15](#), connects the MSL2010 to the Drain of the LED string external MOSFET. Use a  $100k\Omega$  for  $R_D$ .

### 12.2.7 The Input and Output Capacitors

The input and output capacitors carry the high frequency current of the Boost regulator switching. The input capacitor prevents this high frequency current from travelling back to the input voltage source, reducing conducted and radiated noise. The output capacitor prevents high frequency current to the load, in this case the LEDs, and also prevents conducted and radiated noise. The output capacitors also have a large effect on the Boost regulator loop stability and transient response, and so are critical to optimal Boost regulator operation. Use capacitors that keep their rated values at their expected operating voltages. The [“Typical Application Circuit” on page 14](#) shows recommended values for these capacitors.

### 12.2.8 The Compensation Network

The compensation components,  $R_C$ ,  $C_{C1}$  and  $C_{C2}$  in [Figure 12-1 on page 15](#), effectively dampen the oscillation-producing high frequency response of the Boost regulator error amplifier. The [“Typical Application Circuit” on page 14](#) shows recommended values for these capacitors.

## 12.3 The LED string

### 12.3.1 Selecting the LED String MOSFET

The LED string MOSFET sinks the LED current to ground through current sense resistor  $R_S$ . Output G drives the gate of the MOSFET with at up to at least  $V_{AVIN} - 1.5V$ . Select a FET with a maximum drain-source voltage of at least  $V_{OUT(MAX)}$  (from above), and a low  $R_{DS(ON)}$ .

### 12.3.2 Setting LED String On-Current with $R_S$

The LED string on-current regulates by monitoring the voltage at S, the MOSFET source resistor connection. Connect the current sense resistor  $R_S$  from the MOSFET source to ground. The default feedback voltage for S is 0.2V. Choose the string current sense resistor  $R_S$  using:

$$R_S = \frac{0.2}{I_{LED}} \Omega,$$

where  $I_{LED}$  is the LED string regulation current. The LED String Reference Voltage (SREF), register 0x20, sets the 0.2V feedback voltage, at 2mV per LSB. For more information about SREF see the [“LED String Reference Voltage register \(SREF, 0x20\)” on page 20](#).

### 12.3.3 PWM and LED Brightness

MSL2010 uses the input signal at PWM to directly control the duty cycle (brightness) and frequency of the LED string driver output G. The PWM input accepts a signal of 60Hz to 10kHz, 1% to 100% duty cycle; output G operates with a minimum on time of  $2\mu s$ .

## 13. Control Registers

Table 13-1. MSL2010 Register Map (Do not change unspecified registers or bits).

| Address and Register name            | Function | Default value   | Bit functions                   |                        |    |    |              |             |    |
|--------------------------------------|----------|---|---------------------------------|------------------------|----|----|--------------|-------------|----|
|                                      |          |   | D7                              | D6                     | D5 | D4 | D3           | D2          | D1 |
| <b>Control and Monitor Registers</b> |          |   |                                 |                        |    |    |              |             |    |
| 0x00 through 0x1F                    | RAM      | 0xXX  | Free RAM                        |                        |    |    |              |             |    |
| 0x20                                 | SREF     | LED String MOSFET Source Feedback Reference Voltage<br>0x64 | $S_{REF} = 2\text{mV per LSB}$  |                        |    |    |              |             |    |
| 0x21                                 | CSREF    | Boost Current Sense Reference Feedback Voltage<br>0x64      | $CS_{REF} = 2\text{mV per LSB}$ |                        |    |    |              |             |    |
| 0x40                                 | EOCTRL   | Efficiency Optimizer<br>0xE5                                | Reserved[4:0]                   |                        |    |    | DThresh[3:0] |             |    |
| 0x60                                 | E2ADDR   | EEPROM Address<br>0x00                                      | –                               | EEPROM Address Pointer |    |    |              |             |    |
| 0x61                                 | E2CTRL   | EEPROM Control<br>0x00                                      | –                               | –                      | –  | –  | –            | RWCTRL[2:0] |    |
| <b>Unused and Reserved Registers</b> |          |   |                                 |                        |    |    |              |             |    |

### 13.1 EEPROM and Power-Up Defaults

An on-chip EEPROM holds all the default register values (Table 13-1 on page 18). At power-up the data in the EEPROM automatically copy directly to control registers 0x00 thru 0x51, setting up the device for operation.

Any changes made to registers 0x00 thru 0x51 after power-up are not reflected in the EEPROM and are lost when power is removed from the device, or when the enable input EN is forced low. If a different power-up condition is desired program the values into the EEPROM via the serial interface as explained in the next section, or contact the factory to inquire about ordering a customized power-up setting.

### 13.2 EEPROM Address and Control/Status Registers

The EEPROM can be visualized as an image of the control registers from 0x00 thru 0x69. Change an EEPROM register value by writing the new value into the associated control register, and then instructing the device to program that value into the EEPROM. Two control registers facilitate this process, the EEPROM address register E2ADDR (0x60), and the EEPROM control register E2CTRL (0x61). Into E2ADDR write the location of the data that is to be programmed into the EEPROM, and write 0x03 to E2CTRL to command the device to program that data into the EEPROM. Programming the EEPROM takes a finite amount of time; after sending a command to E2CTRL wait 5ms, then end the write cycle by writing 0x00 to E2CTRL.

**Example:** Change the string current feedback voltage MREF to 100mV.

**Commands:** To register 0x20 (MREF) write 0x32 (the new value for MREF). To register 0x60 (E2ADDR) write 0x20 (the address of the MREF register). To register 0x61 (E2CTRL) write 0x03 (the command to copy the value to EEPROM). Wait 5ms. To register 0x61 (E2CTRL) write 0x00, to turn off EEPROM access.

**Result:** The value 0x32, located in the MREF register, is programmed into the EEPROM and becomes the new power-up default value for MREF.

**Summary:**

0x20 32

0x60 20

0x61 03

Wait 5ms

0x61 00

E2CTRL provides additional functions beyond simply programming a register's value into the EEPROM. Data may be transferred in either direction, from the registers to the EEPROM, or from the EEPROM to the registers. Register data may be transferred into or out of the EEPROM in groups of eight, a page at a time. The page address boundaries are predefined, and E2ADDR must be loaded with the address of the first byte of the page that is to be copied. Page addresses begin at 0x00 and increment by eight, with the second page beginning at 0x08, the third at 0x10, etc. To program a full page of data into the EEPROM, write the address of the page's first byte to E2ADDR, and write 0x04 to E2CTRL. Wait 5ms, and then end the write cycle by writing 0x00 to E2CTRL. When finished accessing the EEPROM always write 0x00 to E2CTRL to block inadvertent EEPROM read/writes. [Table 13-2 on page 19](#) details the functions available through E2CTRL.

**Table 13-2. EEPROM Address Register (E2ADDR, 0x60), defaults highlighted.**

| Register                    | Address | Register data |             |          |          |          |          |          |          |  |
|-----------------------------|---------|---------------|-------------|----------|----------|----------|----------|----------|----------|--|
|                             |         | D7            | D6          | D5       | D4       | D3       | D2       | D1       | D0       |  |
| E2ADDR                      | 0x60    | -             | E2ADDR[6:0] |          |          |          |          |          |          |  |
| <b>DEFAULT</b>              |         | <b>0</b>      | <b>0</b>    | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> |  |
| EEPROM Minimum Address 0x00 |         | -             | 0           | 0        | 0        | 0        | 0        | 0        | 0        |  |
| EEPROM Maximum Address 0x51 |         | -             | 1           | 0        | 1        | 0        | 0        | 0        | 1        |  |

**Table 13-3. EEPROM Status Register (E2CTRL, 0x61), defaults highlighted.**

| Register                            | Address | Register data |          |          |          |          |             |          |          |
|-------------------------------------|---------|---------------|----------|----------|----------|----------|-------------|----------|----------|
|                                     |         | D7            | D6       | D5       | D4       | D3       | D2          | D1       | D0       |
| E2CTRL                              | 0x61    | -             | -        | -        | -        | -        | RWCTRL[2:0] |          |          |
| <b>DEFAULT</b>                      |         | <b>0</b>      | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b>    | <b>0</b> | <b>0</b> |
| <b>EEPROM Read / Write Disabled</b> |         | x             | x        | x        | x        | x        | <b>0</b>    | <b>0</b> | <b>0</b> |
| Read 1 Byte from EEPROM             |         | x             | x        | x        | x        | x        | 0           | 0        | 1        |
| Read 8 Bytes from EEPROM            |         | x             | x        | x        | x        | x        | 0           | 1        | 0        |
| Write 1 Byte to EEPROM              |         | x             | x        | x        | x        | x        | 0           | 1        | 1        |
| Write 8 Bytes to EEPROM             |         | x             | x        | x        | x        | x        | 1           | 0        | 0        |
| Unused                              |         | x             | x        | x        | x        | x        | 1           | 0        | 1        |
|                                     |         | x             | x        | x        | x        | x        | 1           | 1        | x        |

## 14. Detailed Register Descriptions

The MSL2010 registers are summarized in “Control Registers” on page 18. Detailed register information follows.

### 14.1 RAM (0x00 through 0x1F)

32 Bytes of RAM accessible through the I<sup>2</sup>C serial interface. Copy data from RAM into EEPROM (see “EEPROM and Power-Up Defaults” on page 18) to have the data automatically load into the RAM at power up, and when EN is taken high.

Table 14-1. RAM (0x00 through 0x1F), defaults undetermined

| REGISTER DATA |         |    |    |    |    |    |    |    |    |
|---------------|---------|----|----|----|----|----|----|----|----|
| REGISTER NAME | ADDRESS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| DEFAULTS      |         | X  | X  | X  | X  | X  | X  | X  | X  |

### 14.2 LED String Reference Voltage register (SREF, 0x20)

Holds the DAC value that controls the reference voltage for the LED string MOSFET source feedback. The reference voltage equals decimal value of this register times 2mV. The default value for SREF is 0x64, which equates to  $V_{SREF} = 200\text{mV}$ .

Table 14-2. LED String Reference register (SREF, 0x20), defaults highlighted

| REGISTER DATA  |         |           |    |    |    |    |    |    |    |
|--|---------|-----------|----|----|----|----|----|----|----|
| REGISTER NAME  | ADDRESS | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| SREF   | 0x20    | SREF[7:0] |    |    |    |    |    |    |    |
| DEFAULT: $V_{SREF} = 0x64 = 100 * 2\text{mV} = 200\text{mV}$ |         | 0         | 1  | 1  | 0  | 0  | 1  | 0  | 0  |
| $V_{SREF} = 0 * 2\text{mV} = 0\text{V}$                      |         | 0         | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| $V_{SREF} = 255 * 2\text{mV} = 510\text{mV}$                 |         | 1         | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

### 14.3 Boost Reference Voltage register (CSREF, 0x21)

Holds the DAC value that controls the reference voltage for the Boost MOSFET source feedback. The reference voltage equals decimal value of this register times 2mV. The default value for CSREF is 0x64, which equates to  $V_{CSREF} = 200\text{mV}$ .

Table 14-3. Boost Reference Voltage register (CSREF, 0x21), defaults highlighted

| REGISTER DATA   |         |            |    |    |    |    |    |    |    |
|---|---------|------------|----|----|----|----|----|----|----|
| REGISTER NAME   | ADDRESS | D7         | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| CSREF   | 0x21    | CSREF[7:0] |    |    |    |    |    |    |    |
| DEFAULT: $V_{CSREF} = 0x64 = 100 * 2\text{mV} = 200\text{mV}$ |         | 0          | 1  | 1  | 0  | 0  | 1  | 0  | 0  |
| $V_{CSREF} = 0 * 2\text{mV} = 0\text{mV}$                     |         | 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| $V_{CSREF} = 255 * 2\text{mV} = 510\text{mV}$                 |         | 1          | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

## 14.4 Efficiency Optimizer Control Register (EOCTRL, 0x40)

DThresh sets the voltage feedback threshold for D, The LED string MOSFET drain connection.

D Threshold = ( $\langle DThresh \rangle * 150mV$ ) + 250mV. This is how the device monitors  $V_{LED}$  to control the magnitude of the EO current. The default value for DThresh is 1V.

**Table 14-4. Efficiency Optimizer Control Register (FBOCTRL, 0x40), default highlighted**

| Register   | Address/<br>Default | Register data |          |          |          |              |          |          |          |
|--|---------------------|---------------|----------|----------|----------|--------------|----------|----------|----------|
|  |                     | D7            | D6       | D5       | D4       | D3           | D2       | D1       | D0       |
| FBOCTRL  | 0x40                | Reserved[4:0] |          |          |          | DThresh[3:0] |          |          |          |
| <b>Defaults</b>  | <b>0xE5</b>         | <b>1</b>      | <b>1</b> | <b>1</b> | <b>0</b> | <b>0</b>     | <b>1</b> | <b>0</b> | <b>1</b> |
| D Threshold = $(0 * 150mV) + 250mV = 0.25V$                |                     | 1             | 1        | 1        | 0        | 0            | 0        | 0        | 0        |
| <b>D Threshold = <math>(5 * 150mV) + 250mV = 1V</math></b> |                     | <b>1</b>      | <b>1</b> | <b>1</b> | <b>0</b> | <b>0</b>     | <b>1</b> | <b>0</b> | <b>1</b> |
| D Threshold = $(15 * 150mV) + 250mV = 2.5V$                |                     | 1             | 1        | 1        | 0        | 1            | 1        | 1        | 1        |

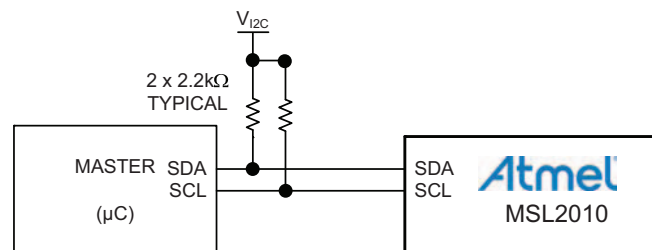
These registers control access to the EEPROM. See “EEPROM and Power-Up Defaults” on page 18 and “EEPROM Address and Control/Status Registers” on page 18 for information.

## 15. I<sup>2</sup>C Serial Interface

The MSL2010 operates as a slave that sends and receives data through an I<sup>2</sup>C/SMBus compatible 2-wire serial interface. The interface is not needed for operation, but is provided to allow control and monitoring of device functions. These functions include changing the string current reference feedback voltages, reading and adjusting the fault response behavior and status, and programming the EEPROM. The I<sup>2</sup>C/SMBus compatible interface is suitable for 100kHz, 400kHz and 1MHz communication. The interface uses data I/O SDA and clock input SCL to achieve bidirectional communication between master and slaves.

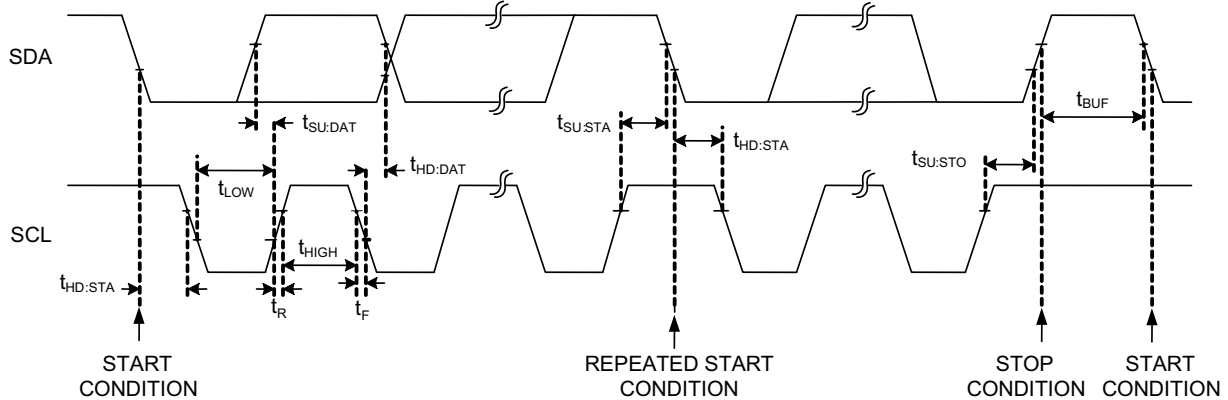
The master, typically a microcontroller, initiates all data transfers, and generates the clock that synchronizes the transfers. SDA operates as both an input and an open-drain output. SCL operates only as an input, and does not perform clock-stretching. Pull-up resistors are required on SDA, and SCL.

**Figure 15-1. I<sup>2</sup>C Interface Connections**



A transmission consists of a START condition sent by a master, a 7-bit slave address plus one R/W bit, an acknowledge bit, none or many data bytes each separated by an acknowledge bit, and a STOP condition (Figure 15-2, Figure 15-4 and Figure 15-5 on page 23).

Figure 15-2. I<sup>2</sup>C Serial Interface Timing Details



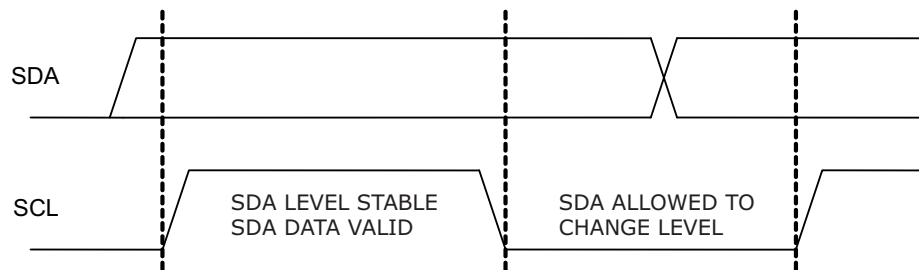
### 15.1 I<sup>2</sup>C Bus Timeout

The bus timeout feature allows the MSL2010 to reset the serial bus interface if a communication ceases before a STOP condition is sent. If SCL or SDA is low for more than 25ms (typical), then the MSL2010 terminates the transaction, releases SDA and waits for another START condition.

### 15.2 I<sup>2</sup>C Bit Transfer

One data bit is transferred during each clock pulse. SDA must remain stable while SCL is high.

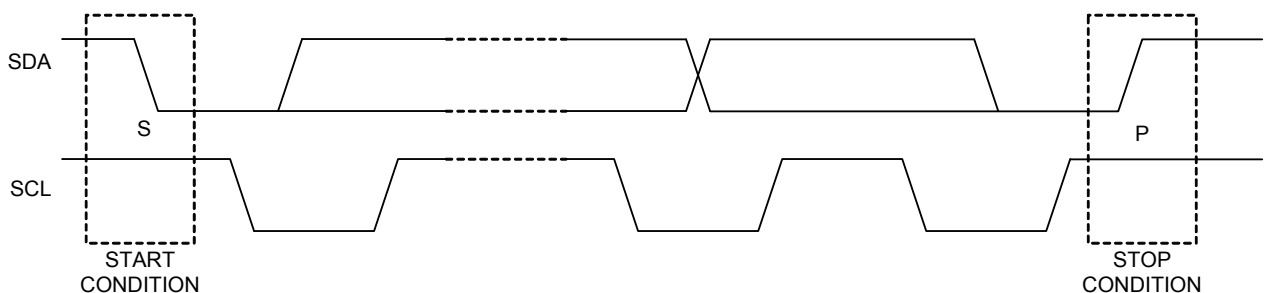
Figure 15-3. I<sup>2</sup>C Bit Transfer



### 15.3 I<sup>2</sup>C START and STOP Conditions

Both SCL and SDA remain high when the interface is free. The master signals a transmission with a START condition (S) by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition (P) by transitioning SDA from low to high while SCL is high. The bus is then free.

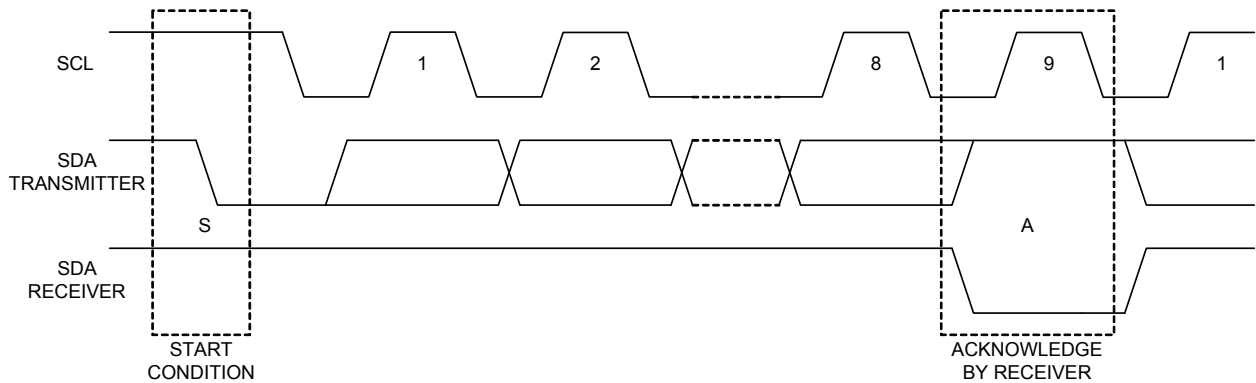
Figure 15-4. I<sup>2</sup>C START and STOP Conditions



## 15.4 I<sup>2</sup>C Acknowledge Bit

The acknowledge bit is a clocked 9th bit which the recipient uses to handshake receipt of each byte of data. The master generates the 9th clock pulse, and the recipient holds SDA low during the high period of the clock pulse. When the master is transmitting to the MSL2010, the MSL2010 pulls SDA low because the MSL2010 is the recipient. When the MSL2010 is transmitting to the master, the master pulls SDA low because the master is the recipient.

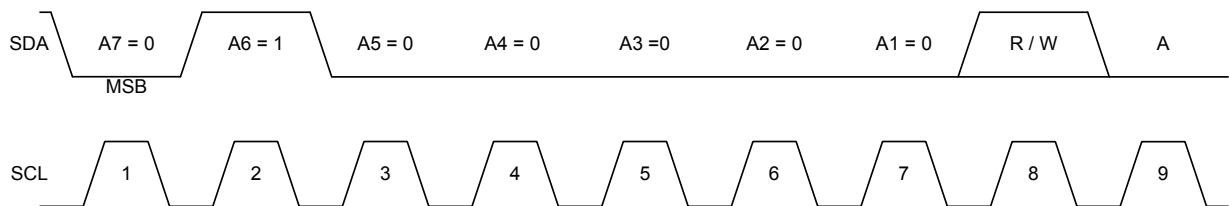
Figure 15-5. I<sup>2</sup>C Acknowledge



## 15.5 I<sup>2</sup>C Slave Address

The MSL2021 has a 7-bit long slave address, 0b0100000, followed by an eighth bit, the R/W bit. The R/W bit is low for a write to the MSL2010, high for a read from the MSL2010. All MSL2010 devices have the same slave address; when using multiple devices and communicating with them through their serial interfaces, make external provision to route the serial interface to the appropriate device. Note that development systems that use I<sup>2</sup>C often left-shift the address one position before they insert the R/W bit, and thus expect a base address setting of 0x20 instead of 0x40.

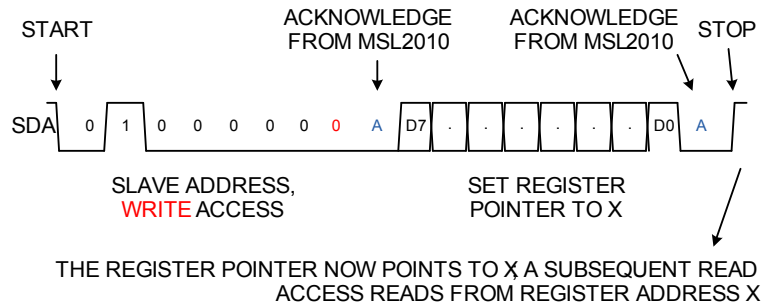
Figure 15-6. I<sup>2</sup>C Slave Address



## 15.6 I<sup>2</sup>C Message Format for Writing to the MSL2010

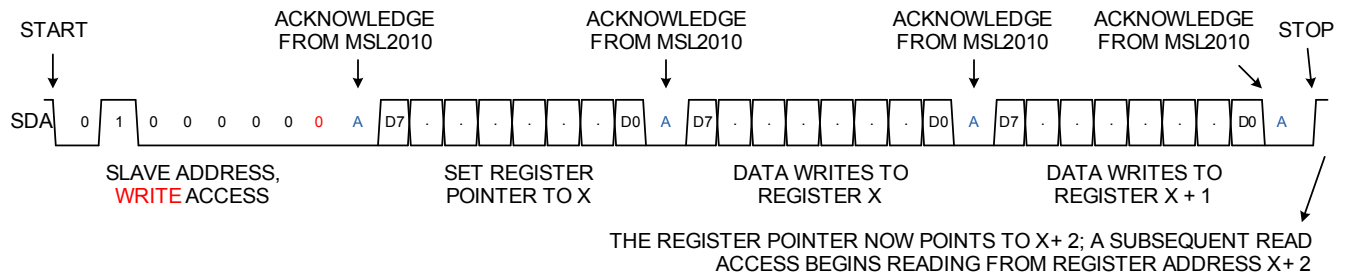
A write to the MSL2010 contains the MSL2010's slave address, the R/W bit cleared to 0, and at least 1 byte of information (Figure 15-7 on page 24). The first byte of information is the register address byte. The register address byte is stored as a register pointer, and determines which register the following byte is written into. If a STOP condition is detected after the register address byte is received, then the MSL2010 takes no further action beyond setting the register pointer.

**Figure 15-7. I<sup>2</sup>C Writing a Register Pointer**



When no STOP condition is detected, the byte transmitted after the register address byte is a data byte, and is placed into the register pointed to by the register address byte (Figure 15-8). To simplify writing to multiple consecutive registers, the register pointer auto-increments during each following acknowledge period. Further data bytes transmitted before a STOP condition fill subsequent registers.

**Figure 15-8. I<sup>2</sup>C Writing Two Data Bytes**

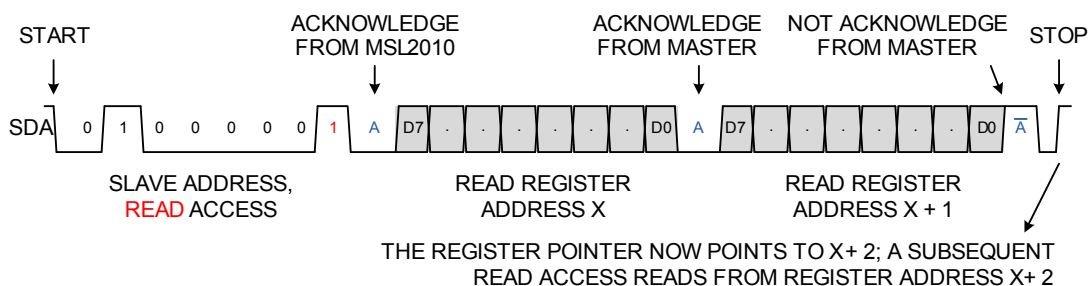


## 15.7 I<sup>2</sup>C Message Format for Reading from the MSL2010

Read the MSL2010 registers using one of two techniques.

The first technique begins the same way as a write, by setting the register address pointer as shown in Figure 15-7, including the STOP condition (note that even though the final objective is to read data, the R/W bit is first sent as a write because the address pointer byte is being written into the device). Follow the Figure 15-7 transaction by what shown in Figure 15-9, with a new START condition and the slave address, this time with the R/W bit set to 1 to indicate a read. Then, after the slave initiated acknowledge bit, clock out as many bytes as desired, separated by master initiated acknowledges. The pointer auto-increments during each master initiated acknowledge period. End the transmission with a not-acknowledge followed by a stop condition.

**Figure 15-9. I<sup>2</sup>C Reading Register Data with Preset Register Pointer**

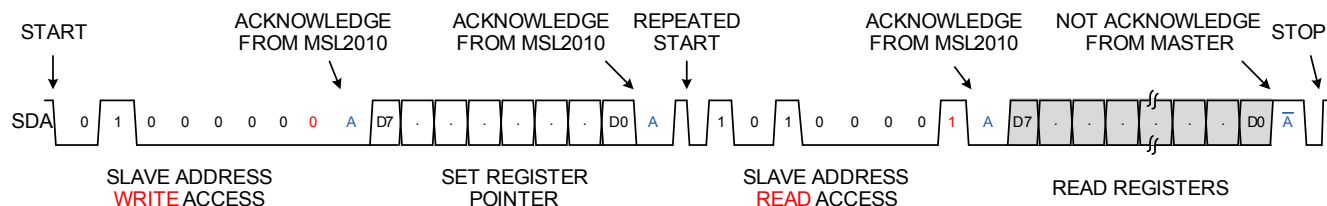


The second read technique is illustrated in Figure 15-10. Write to the MSL2010 to set the register pointer, send a repeated START condition after the second acknowledge bit, then send the slave address again with the R/W bit set to 1 to indicate a read. Then clock out the data bytes separated by master initiated acknowledge bits. The register pointer auto-increments during each master initiated acknowledge period. End the transmission with a not-acknowledge



followed by a stop condition. This technique is recommended for buses with multiple masters, because the read sequence is performed in one uninterrupted transaction.

**Figure 15-10. I<sup>2</sup>C Reading Register Data Using a Repeated START**

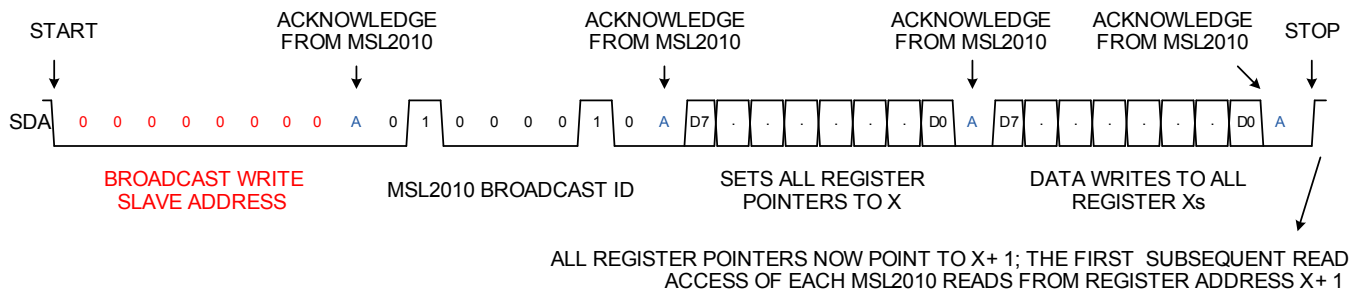


## 15.8 I<sup>2</sup>C Message Format for Broadcast Writing to Multiple devices

With a broadcast write to MSL2010, a master broadcasts the same register data to all MSL2010s on the bus. First send the broadcast write slave address of 0x00, followed by the MSL2010 broadcast device ID of 0x42. These two bytes are followed by the register address in the MSL2010's that the following data are to be written into, and finally the data byte(s) to be written into all devices.

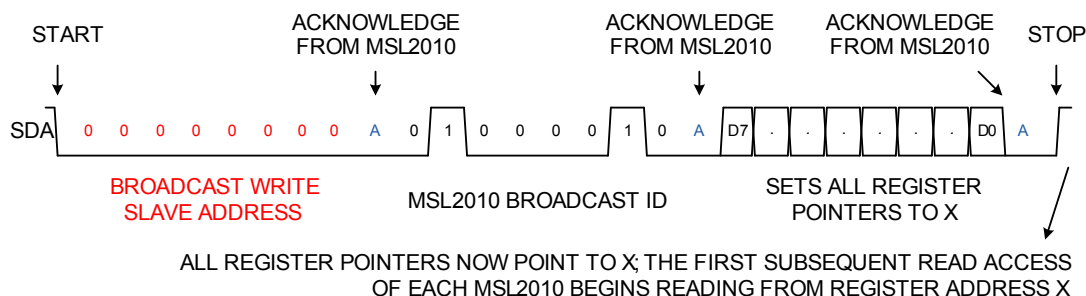
A broadcast write example is shown in [Figure 15-11](#). Here, the same register address in every MSL2010 is written to with identical data. If further data bytes are transmitted before the STOP condition, they are stored in subsequent internal registers of each MSL2010.

**Figure 15-11. I<sup>2</sup>C Broadcast Writing a Data Byte**

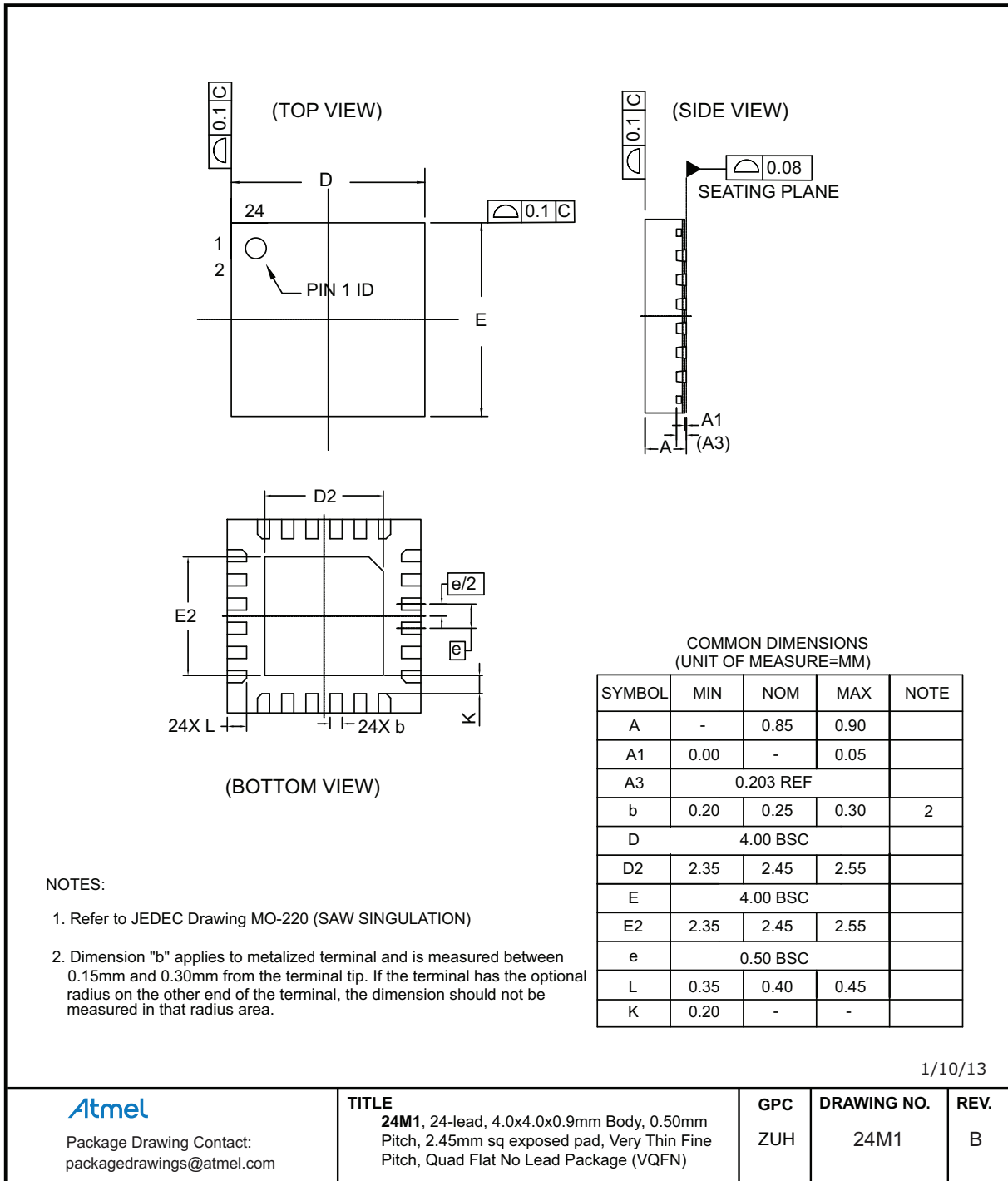


There is no broadcast read. However, a broadcast write may be used to set up the internal register pointers of all the MSL2010s in a system to speed up the subsequent individual reading of, for example, all the status registers. [Figure 15-12](#) illustrates a broadcast write that sets all the register pointers, and issues a STOP.

**Figure 15-12. I<sup>2</sup>C Broadcast Writing a Register Pointer**



## 16. Packaging Information



No representation or warranties are made concerning third-party patents with regard to the use of Atmel® products. The mixing of red LEDs with phosphor-converted LEDs may be protected by certain third-party patents, such as U.S. Patent No. 7,213,940 and related patents of Cree, Inc.

## 17. Datasheet Revision History

### 17.1 42072A – 05/2013

|    |                   |
|----|-------------------|
| 1. | Initial revision. |
|----|-------------------|

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