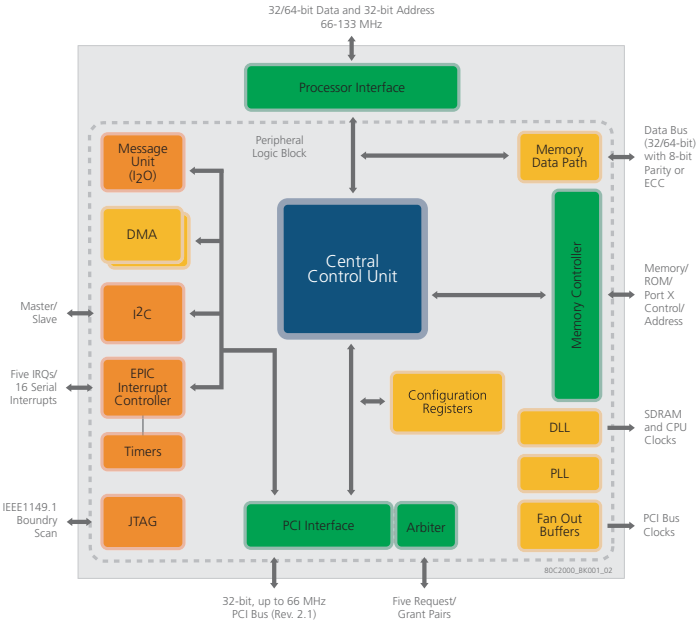
Tsi107™ Host Bridge for PowerPC® Product Brief

Device Overview

The IDT Tsi107 Host Bridge for PowerPC provides system interconnect between PowerPC processors, PCI peripherals, and local memory. PCI support allows system designers to design systems quickly using peripherals already developed for PCI and the other standard interfaces available in the personal computer hardware environment.

The Tsi107 provides many of the other necessities for embedded applications, including a high-performance memory controller and dual-processor support; two-channel flexible DMA controller; an interrupt controller; an I2O-ready message unit; an inter-integrated circuit controller (I2C); and low-skew clock drivers. The Tsi107 contains an Embedded Programmable Interrupt Controller (EPIC) featuring five hardware interrupts (IRQs), as well as 16 serial interrupts and four timers. The Tsi107 uses an advanced, 2.5V CMOS process technology, and is fully compatible with TTL devices.

Block Diagram



Multiprocessor and Local Bus Slave Support

The Tsi107 supports a programmable interface to microprocessors implementing the PowerPC architecture, operating at bus frequencies up to 133 MHz. The Tsi107 processor interface allows for a variety of system configurations by providing support for a second processor and a local bus slave.

Integrated Memory Controller

The memory interface controls processor and PCI interactions to main memory. It supports a variety of programmable DRAM (FPM, EDO), SDRAM, and ROM/Flash ROM configurations. These support timing at speeds of up to 133 MHz.

PCI Bus Support

The Tsi107 PCI interface is designed to connect the processor and memory buses to the PCI local bus without the need for “glue” logic. It runs at speeds up to 66 MHz. The Tsi107 acts as either a master or target on the PCI bus and contains a PCI bus arbitration unit which reduces the need for an equivalent external unit. This reduces the total system complexity and cost.

Features

Processor Interface

- Supports the Motorola MPC603e, MPC7xx, and MPC74xx processors
- Supports the IBM PowerPC 603e, and PowerPC 7xx processors
- Processor bus frequency up to 133 MHz
- 64/32-bit data bus, 32-bit address bus
- I/O voltage: 2.5V or 3.3V
- SMP support for a second processor
- Full memory coherency, integrated arbiter and slave peripheral support

Memory Interface

- High-bandwidth (32-bit/64-bit) data bus up to 133 MHz
- Programmable timing: supports either DRAM (FPM, EDO) or SDRAM
- Supports one to eight banks: 4, 16, 64, 128, and/or 256-bit DRAMs/SDRAMs
- 1 GB RAM space, 144 MB ROM space
- 8, 32, or 64-bit ROM/Flash ROM
- 8, 32, or 64-bit general-purpose I/O port: uses ROM controller interface with address strobe
- Supports parity, read-modify-write, or error-correcting code (ECC)

PCI Interface

- Compliant with PCI specification, (revision 2.1)
- 32-bit PCI interface — up to 66 MHz
- 5.0 V compatible
- Read and write buffers to improve PCI performance
- Selectable big or little-endian operation
- PCI interface acts as host or agent — allows multiple Tsi107s on one PCI bus

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- Arbiter supports up to five other PCI devices
- Two-channel integrated DMA controller
- Intelligent Input/Output (I2O) message controller
- Doorbell and messaging registers
- Inter-Integrated Circuit (I2C) Controller
- Embedded Programmable Interrupt Controller (EPIC)
- Integrated PCI bus and SDRAM clock generation

General

- Available in commercial temperature range (0 to 105°C junction temperature)
- IEEE 1149.1 compliant, JTAG boundary-scan interface
- Power management unit
- Inter-Integrated Circuit (I2C) Controller
- Embedded Programmable Interrupt Controller (EPIC)
- Integrated PCI bus and SDRAM clock generation
- Available in commercial temperature range (0 to 105°C junction temperature)
- IEEE 1149.1 compliant, JTAG boundary-scan interface
- Power management unit

Package

- 503-pin flip chip plastic ball grid array (FC-PBGA)
- Package outline: 33 mm x 33 mm, pitch 1.27 mm

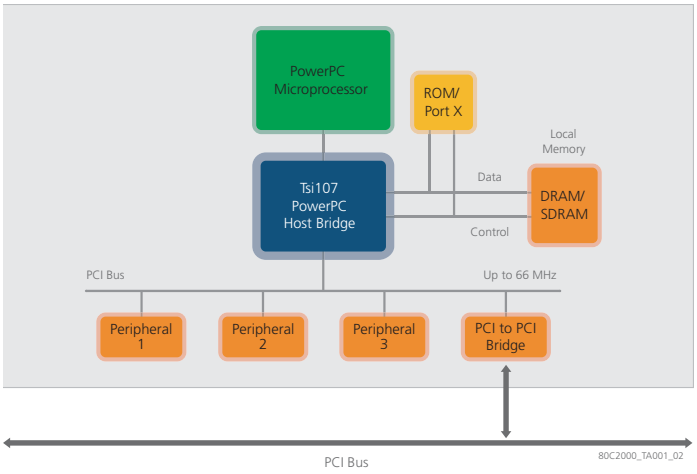
Benefits

- Proven PowerPC system interconnect solution
- Low latency, high performance memory controller
- Integrated clock drivers, PCI, and processor bus arbiters reduce system complexity and cost

Typical Applications

The Tsi107 can be used in either a system host configuration or as a peripheral device. For system applications where cost, space, and power consumption are critical parameters, the Tsi107 provides a complete solution without sacrificing performance. The Tsi107 is shown below as a host bridge.

Host Bridge Application



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