DATASHEET

Wide V_{IN} 300mA Synchronous Buck Regulator

ISL85413

The ISL85413 is a 300mA synchronous buck regulator with an input range of 3.5V to 40V. It provides an easy to use, high efficiency low BOM count solution for a variety of applications.

The ISL85413 integrates both high-side and low-side NMOS FETs and features a PFM mode for improved efficiency at light loads. This feature can be disabled if forced PWM mode is desired. The part switches at a default frequency of 700kHz. By integrating both NMOS devices and providing internal configuration, minimal external components are required, reducing BOM count and complexity of design.

With the wide V_{IN} range and reduced BOM, the part provides an easy to implement design solution for a variety of applications while giving superior performance. It will provide a very robust design for high voltage industrial applications as well as an efficient solution for battery powered applications.

The part is available in a small Pb-free 3mmx3mm TDFN plastic package with an operation junction temperature range of -40°C to +125°C.

Related Literature

- AN1929, “ISL85413EVAL1Z, ISL85412EVAL1Z Evaluation Boards”
- AN1931, “ISL85413DEMO1Z, ISL85412DEMO1Z Wide VIN Synchronous Buck Regulator - Short Form”

Features

- Wide input voltage range of 3.5V to 40V
- Synchronous operation for high efficiency
- No compensation required
- Integrated high-side and low-side NMOS devices
- Selectable PFM or forced PWM mode at light loads
- Internal switching frequency 700kHz
- Continuous output current up to 300mA
- Internal soft-start
- Minimal external components required
- Power-good and enable functions available

Applications

- Industrial control
- Medical devices
- Portable instrumentation
- Distributed power supplies
- Cloud infrastructure

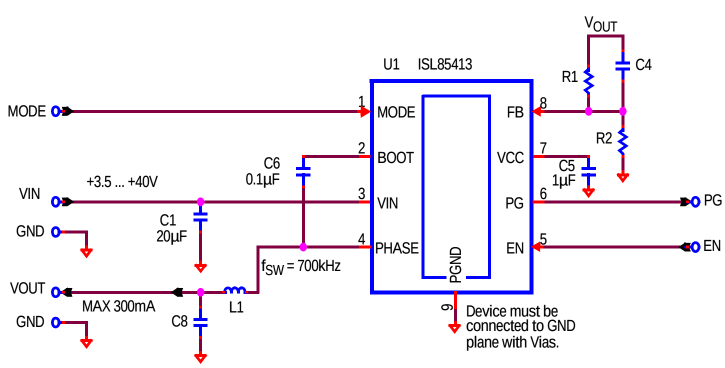

FIGURE 1. TYPICAL APPLICATION

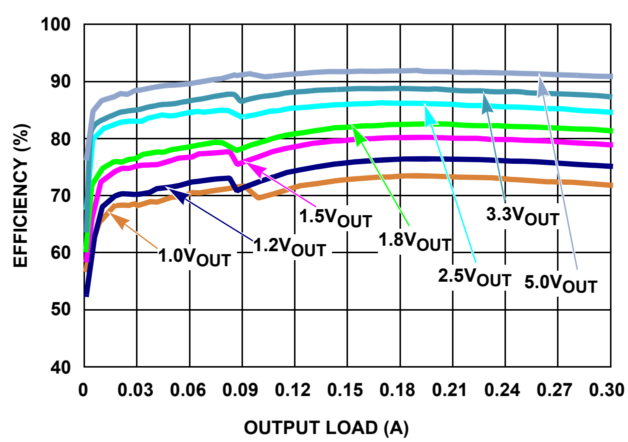

FIGURE 2. EFFICIENCY vs LOAD, PFM, V_{IN} = 12V

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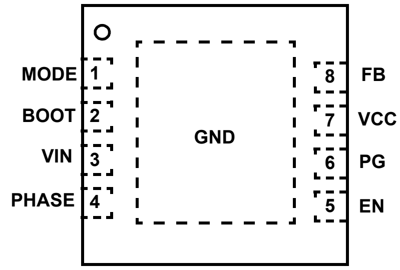
Pin Configuration

ISL85413
(8 LD 3x3 TDFN)
TOP VIEW



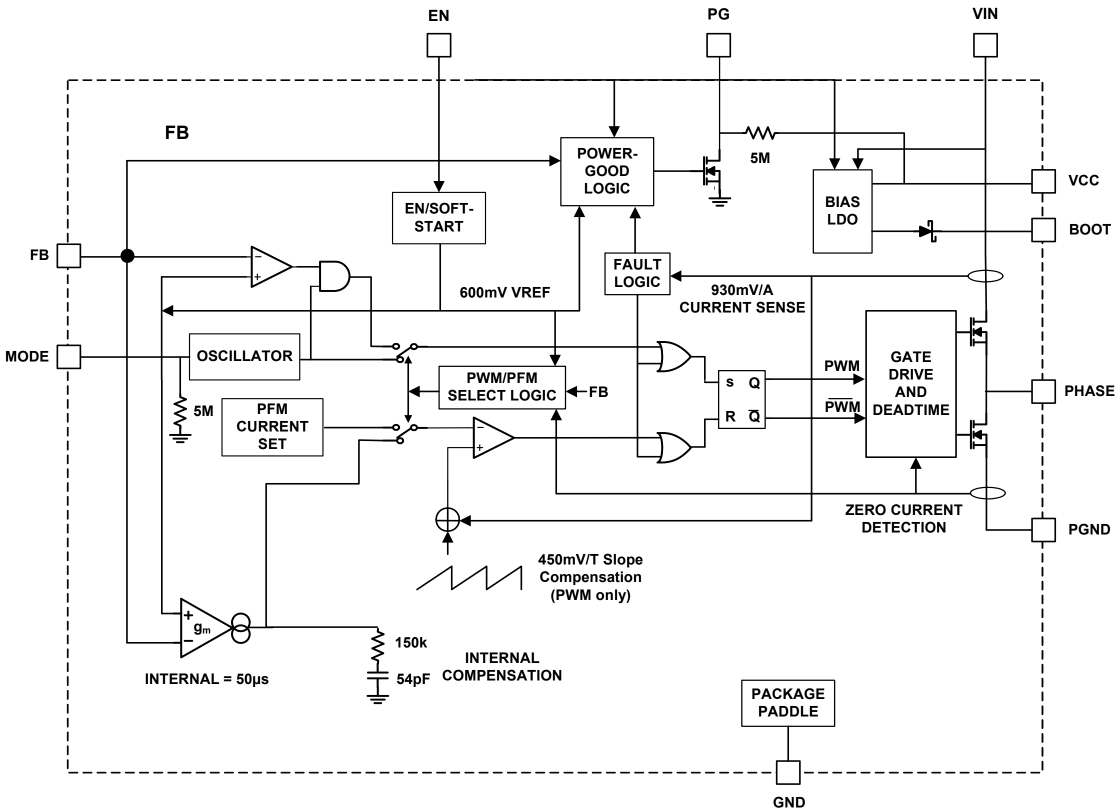
Pin Descriptions

PIN NUMBER	SYMBOL	PIN DESCRIPTION
1	MODE	Mode Selection pin. Connect to logic high or VCC for PWM mode. Connect to logic low or ground for PFM mode. Logic ground enables the IC to automatically choose PFM or PWM operation. There is an internal 5MΩ pull-down resistor to prevent an undefined logic state if MODE is left floating.
2	BOOT	Floating bootstrap supply pin for the power MOSFET gate driver. The bootstrap capacitor provides the necessary charge to turn on the internal N-Channel MOSFET. Connect an external 100nF capacitor from this pin to PHASE.
3	VIN	The input supply for the power stage of the regulator and the source for the internal linear bias regulator. Place a minimum of 10µF ceramic capacitance from VIN to GND and close to the IC for decoupling.
4	PHASE	Switch node output. It connects the switching FETs with the external output inductor.
5	EN	Regulator enable input. The regulator and bias LDO are held off when the pin is pulled to ground. When the voltage on this pin rises above 1V, the chip is enabled. Connect this pin to VIN for automatic start-up. Do not connect EN pin to VCC since the LDO is controlled by EN voltage.
6	PG	Open drain power-good output that is pulled to ground when the output voltage is below regulation limits or during the soft-start interval. There is an internal 5MΩ internal pull-up resistor.
7	VCC	Output of the internal 5V linear bias regulator. Decouple to PGND with a 1µF ceramic capacitor at the pin.
8	FB	Feedback pin for the regulator. FB is the inverting input to the voltage loop error amplifier. COMP is the output of the error amplifier. The output voltage is set by an external resistor divider connected to FB. In addition, the PWM regulator’s power-good and UVLO circuits use FB to monitor the regulator output voltage.
EPAD	GND	Signal ground connections. Connect to application board GND plane with at least 5 vias. All voltage levels are measured with respect to this pin. The EPAD MUST not float.

TABLE 1. EXTERNAL COMPONENT SELECTION (Refer To Figure 1)

V_{OUT} (V)	C_4 (pF)	C_8 (µF)	L_1 (µH)	R_1 (kΩ)	R_2 (kΩ)
1.0	100	2x22	10	90.9	137
1.2	100	2x22	10	90.9	90.9
1.5	100	2x22	16	90.9	60.4
1.8	100	2x22	16	90.9	45.3
2.5	100	22	22	90.9	28.7
3.3	100	22	33	90.9	20
5.0	100	22	47	90.9	12.4
12.0	100	22	100	90.9	4.75

Functional Block Diagram



Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL85413FRTZ	5413	-40 to +125	8 Ld TDFN	L8.3x3H
ISL85413EVAL1Z	Evaluation Board			
ISL85413DEMO1Z	Demonstration Board			

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL85413. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

VIN to GND. . . . . -0.3V to +43V
PHASE to GND. . . . . -0.3V to VIN + 0.3V (DC)
PHASE to GND. . . . . -2V to 44V (20ns)
EN to GND . . . . -0.3V to +43V
BOOT to PHASE. . . . . -0.3V to +5.5V
COMP, FS, PG, MODE, SS, VCC to GND. . . . . -0.3V to +5.9V
FB to GND . . . . -0.3V to +2.95V
Junction Temperature Range at 0A . . . . +150°C
ESD Rating
  Human Body Model (Tested per JESD22-A114) 2.5kV
  Charged Device Model (Tested per JESD22-C101E). 1kV
  Machine Model (Tested per JESD22-A115). 200V
Latch-up (Tested per JESD-78A; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
TDFN Package (Notes 4, 5)	47	4

Maximum Junction Temperature (Plastic Package) . . . .+150°C
Maximum Storage Temperature Range . . . . -65°C to +150°C
Operating Junction Temperature Range . . . . -40°C to +125°C
Pb-Free Reflow Profile . . . . see TB493

Recommended Operating Conditions

Temperature . . . . -40°C to +125°C
Supply Voltage . . . . +3.5V to +40V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379 for details.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

T_J = -40°C to +125°C, V_{IN} = 3.5V to 40V, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the junction temperature range, -40°C to +125°C**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
SUPPLY VOLTAGE						
V_{IN} Voltage Range	V_{IN}		**3.5**		**40**	V
V_{IN} Quiescent Supply Current	I_Q	V_{FB} = 0.7V, MODE = 0V		50		µA
V_{IN} Shutdown Supply Current	I_{SD}	EN = 0V, V_{IN} = 40V (Note 6)		1.8	**2.5**	µA
V_{CC} Voltage	V_{CC}	V_{IN} = 40V	**4.5**	5.1	**5.5**	V
		V_{IN} = 12V; I_{OUT} = 0A to 10mA	**4.35**	5	**5.45**	V
POWER-ON RESET						
V_{CC} POR Threshold		Rising Edge		3.3	**3.46**	V
		Falling Edge	**2.76**	3		V
OSCILLATOR						
Nominal Switching Frequency	f_{SW}		**600**	700	**784**	kHz
Minimum Off-Time	t_{OFF}	V_{IN} = 3.5V		130		ns
Minimum On-Time	t_{ON}	(Note 9)		90		ns
ERROR AMPLIFIER						
Error Amplifier Transconductance Gain	gm			50		µA/V
FB Leakage Current		V_{FB} = 0.6V		1	**100**	nA
Current Sense Amplifier Gain	R_T		**0.84**	0.93	**1.02**	V/A
FB Voltage		T_A = -40°C to +125°C	**0.589**	0.599	**0.606**	V

Electrical Specifications

T_J = -40°C to +125°C, V_{IN} = 3.5V to 40V, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the junction temperature range, -40°C to +125°C (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
POWER-GOOD						
Lower PG Threshold - VFB Rising				91	**94**	%
Lower PG Threshold - VFB Falling			**81.5**	85		%
Upper PG Threshold - VFB Rising				118	**121**	%
Upper PG Threshold - VFB Falling			**107**	111		%
PG Propagation Delay		Percentage of the soft-start time		10		%
PG Low Voltage		I_{SINK} = 3mA, EN = V_{CC}, V_{FB} = 0V		0.05	**0.3**	V
TRACKING AND SOFT-START						
Internal Soft-start Ramp Time		EN/SS = V_{CC}	**1.5**	2.3	**3.1**	ms
FAULT PROTECTION						
Thermal Shutdown Temperature	T_{SD}	Rising Threshold		150		°C
	T_{HYS}	Hysteresis		20		°C
Current Limit Blanking Time	t_{OCON}			17		Clock pulses
Overcurrent and Auto Restart Period	t_{OCOFF}			8		SS cycle
Positive Peak Current Limit	IPLIMIT	(Note 7)	**0.54**	0.6	**0.66**	A
PFM Peak Current Limit	I_{PK_PFM}		**0.17**	0.22	**0.27**	A
Zero Cross Threshold				5		mA
Negative Current Limit	INLIMIT	(Note 7)	**-0.33**	-0.30	**-0.27**	A
POWER MOSFET						
High-side	R_{HDS}	I_{PHASE} = 100mA, V_{CC} = 5V		900	**1300**	mΩ
Low-side	R_{LDS}	I_{PHASE} = 100mA, V_{CC} = 5V		500	**800**	mΩ
PHASE Leakage Current		EN = PHASE = 0V		50	**300**	nA
PHASE Rise Time	t_{RISE}	V_{IN} = 40V		10		ns
EN/MODE						
Mode Input Threshold		Rising Edge, Logic High		1.3	**1.45**	V
		Falling Edge, Logic Low	**0.4**	1.0		V
EN Threshold		Rising Edge, Logic High		1.2	**1.45**	V
		Falling Edge, Logic Low	**0.4**	0.9		V
EN Logic Input Leakage Current		EN = 0V/40V	**-0.5**		**0.5**	µA
MODE Logic Input Leakage Current		MODE = 0V		10	**100**	nA
MODE Pull-down Resistor				5	**6.15**	MΩ

NOTES:

6. Test Condition: V_{IN} = 40V, FB forced above regulation point (0.6V), no switching, and power MOSFET gate charging current not included.
7. Established by both current sense amplifier gain test and current sense amplifier output test at I_L = 0A.
8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
9. Minimum On-Time required to maintain loop stability.

Efficiency Curves f_{SW} = 700kHz, T_A = +25°C, C_{IN} = 20µF

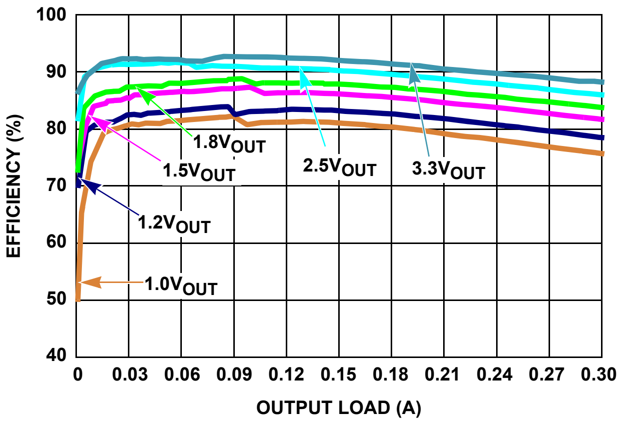


FIGURE 3. EFFICIENCY vs LOAD, PFM, V_{IN} = 5V

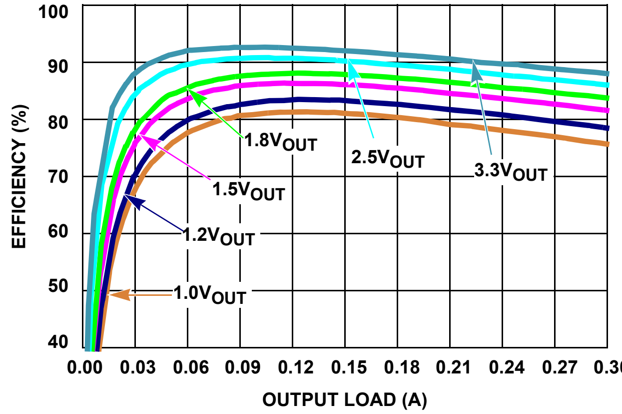


FIGURE 4. EFFICIENCY vs LOAD, PWM, V_{IN} = 5V

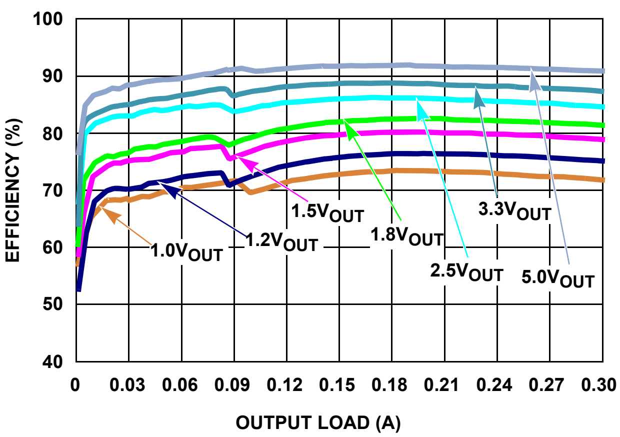


FIGURE 5. EFFICIENCY vs LOAD, PFM, V_{IN} = 12V

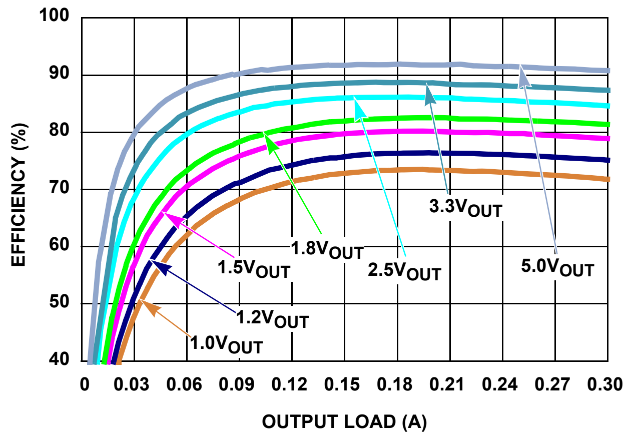


FIGURE 6. EFFICIENCY vs LOAD, PWM, V_{IN} = 12V

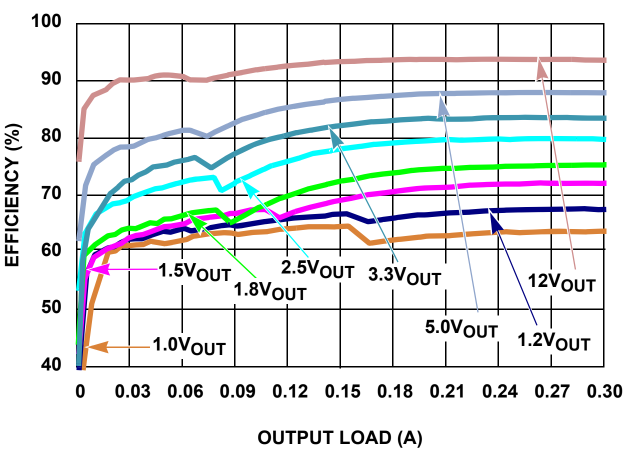


FIGURE 7. EFFICIENCY vs LOAD, PFM, V_{IN} = 24V

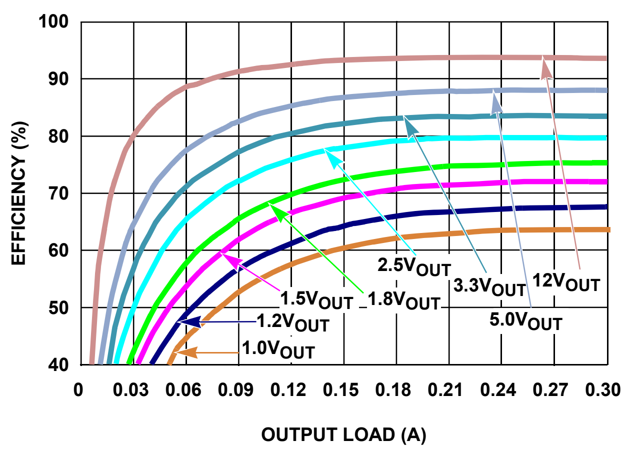


FIGURE 8. EFFICIENCY vs LOAD, PWM, V_{IN} = 24V

Efficiency Curves f_{SW} = 700kHz, T_A = +25°C, C_{IN} = 20µF (Continued)

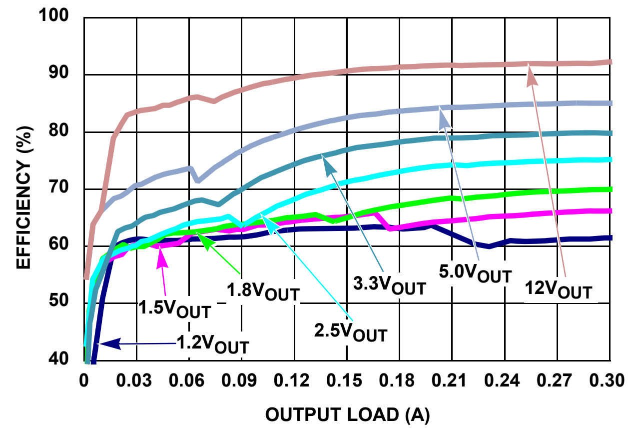


FIGURE 9. EFFICIENCY vs LOAD, PFM, V_{IN} = 36V

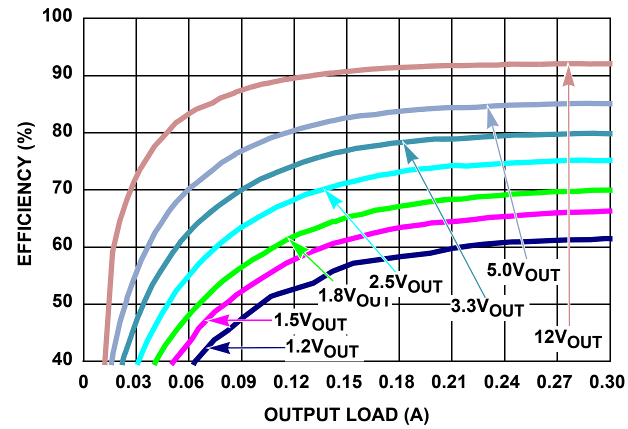


FIGURE 10. EFFICIENCY vs LOAD, PWM, V_{IN} = 36V

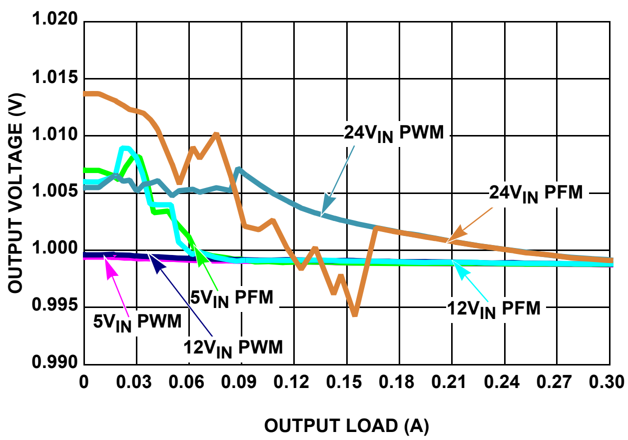


FIGURE 11. V_{OUT} REGULATION vs LOAD, V_{OUT} = 1V

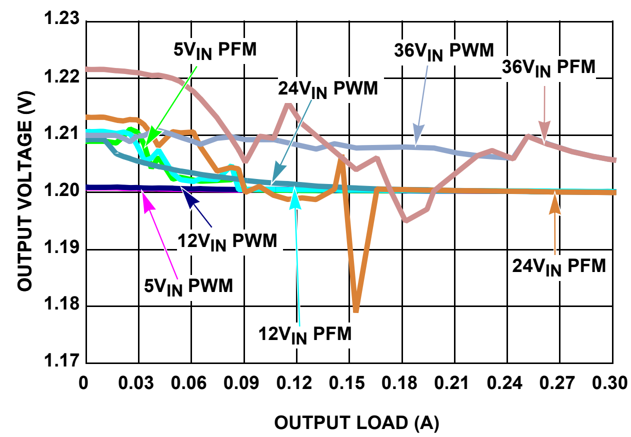


FIGURE 12. V_{OUT} REGULATION vs LOAD, V_{OUT} = 1.2V

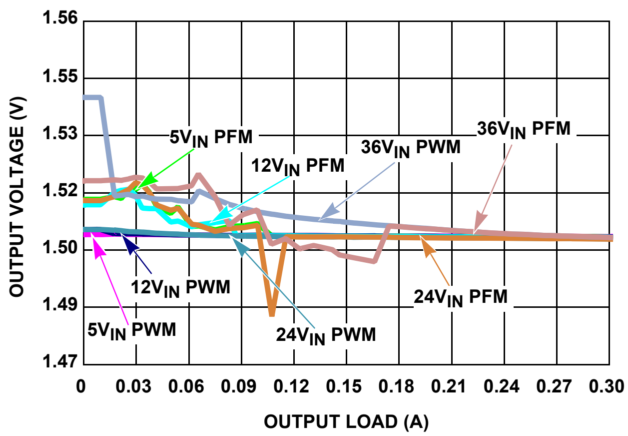


FIGURE 13. V_{OUT} REGULATION vs LOAD, PWM, V_{OUT} = 1.5V

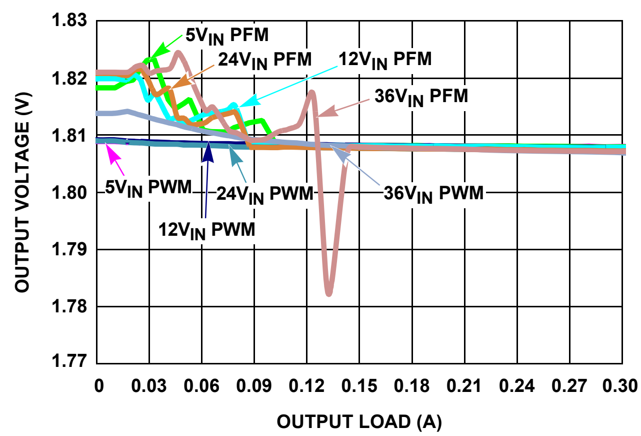


FIGURE 14. V_{OUT} REGULATION vs LOAD, V_{OUT} = 1.8V

Efficiency Curves f_{SW} = 700kHz, T_A = +25°C, C_{IN} = 20µF (Continued)

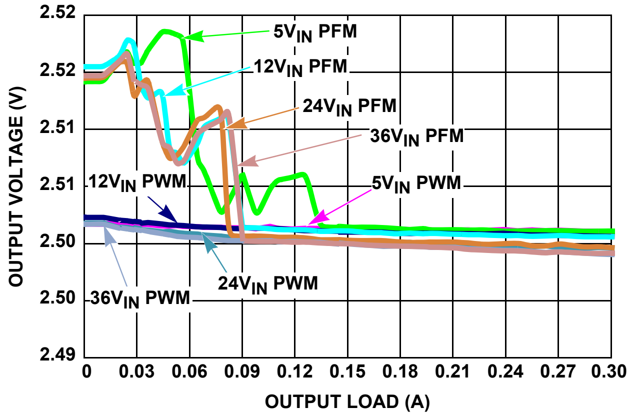


FIGURE 15. V_{OUT} REGULATION vs LOAD, V_{OUT} = 2.5V

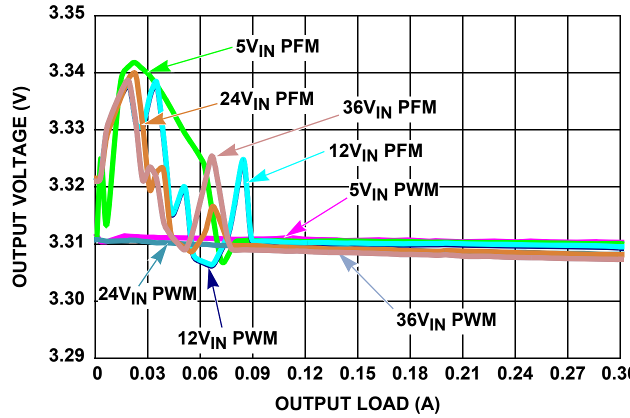


FIGURE 16. V_{OUT} REGULATION vs LOAD, V_{OUT} = 3.3V

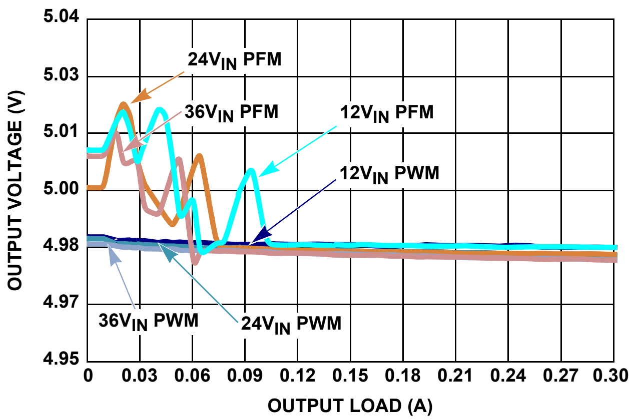


FIGURE 17. V_{OUT} REGULATION vs LOAD, V_{OUT} = 5V

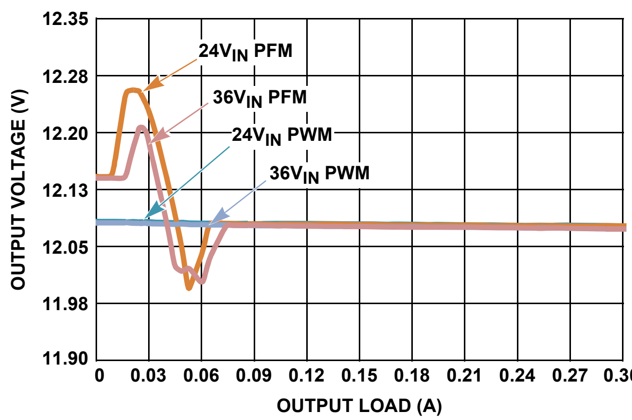


FIGURE 18. V_{OUT} REGULATION vs LOAD, V_{OUT} = 12V

Typical Performance Curves V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 700kHz, T_A = +25°C, C_{IN} = 20µF, C_{OUT} = 22µF

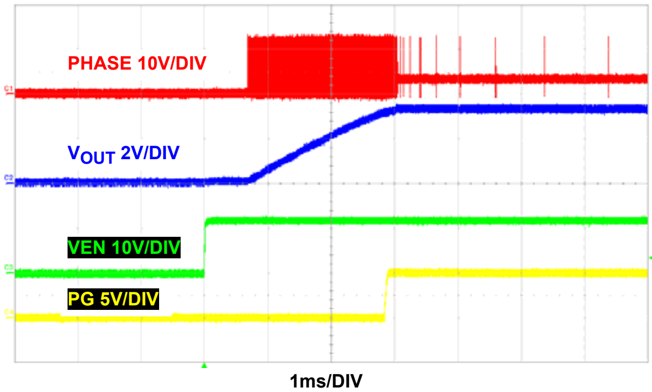


FIGURE 19. START-UP AT NO LOAD, PFM

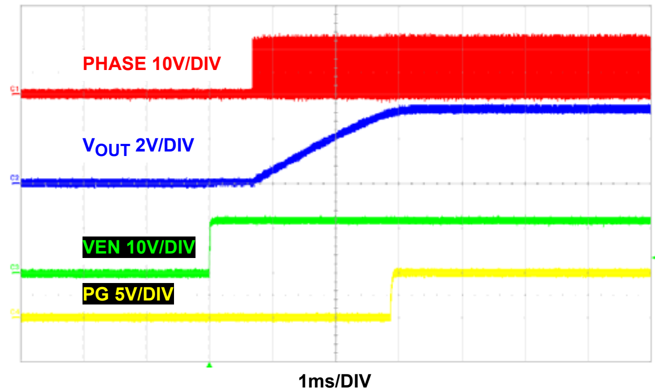


FIGURE 20. START-UP AT NO LOAD, PWM

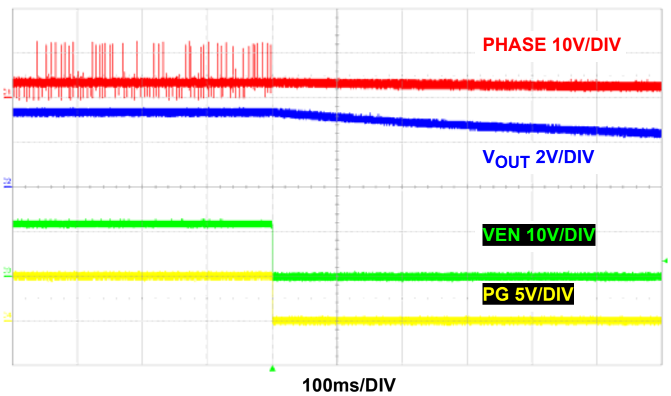


FIGURE 21. SHUTDOWN IN NO LOAD, PFM

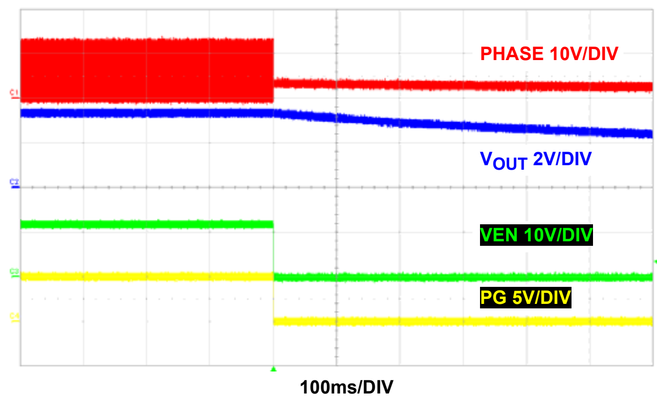


FIGURE 22. SHUTDOWN AT NO LOAD, PWM

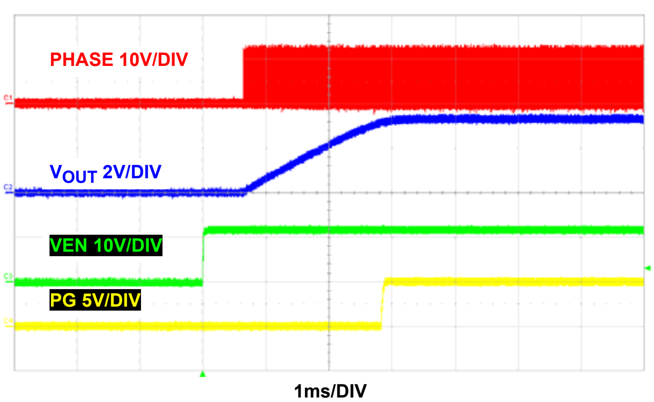


FIGURE 23. START-UP AT 300mA, PWM

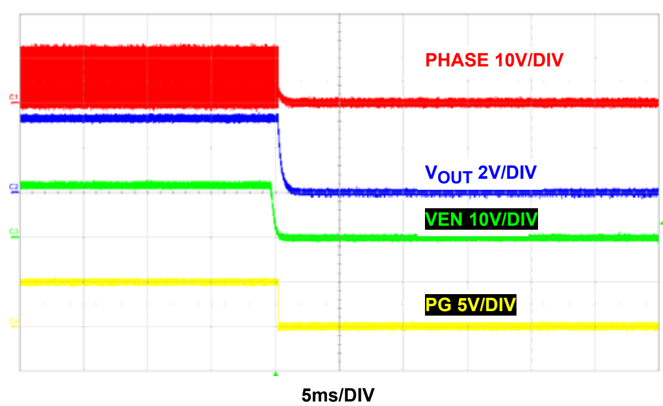


FIGURE 24. SHUTDOWN AT 300mA, PWM

Typical Performance Curves V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 700kHz, T_A = +25°C, C_{IN} = 20µF, C_{OUT} = 22µF (Continued)

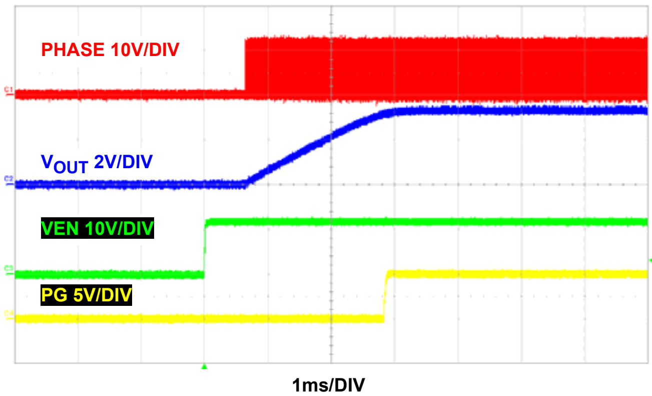


FIGURE 25. START-UP AT 300mA, PFM

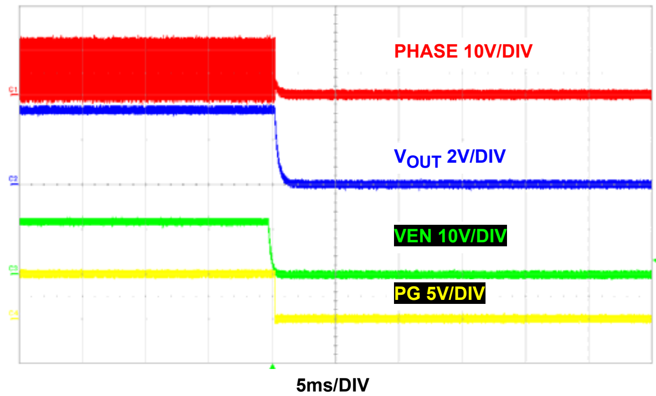


FIGURE 26. SHUTDOWN AT 300mA, PFM

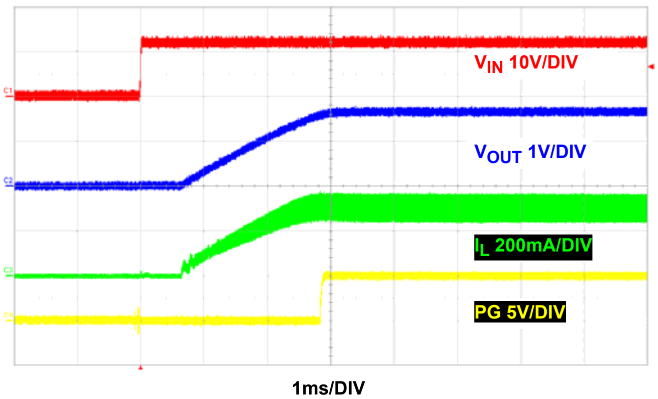


FIGURE 27. START-UP V_{IN} AT 300mA LOAD, PFM

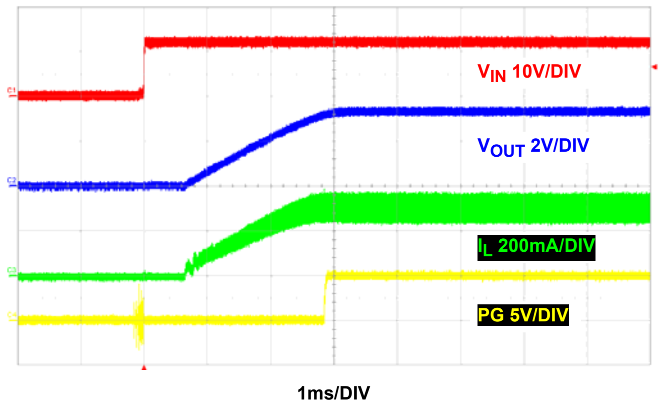


FIGURE 28. START-UP V_{IN} AT 300mA LOAD, PWM

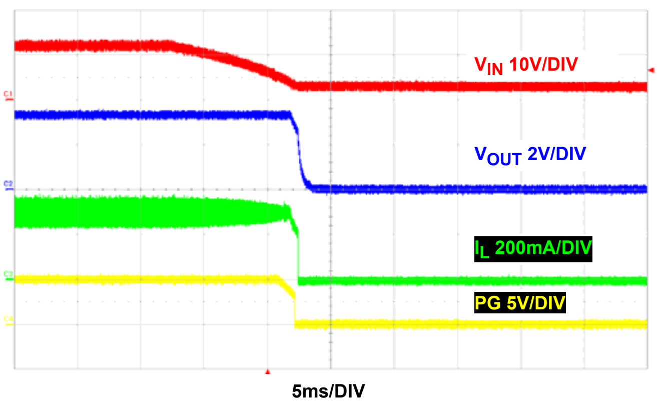


FIGURE 29. SHUTDOWN V_{IN} AT 300mA LOAD, PFM

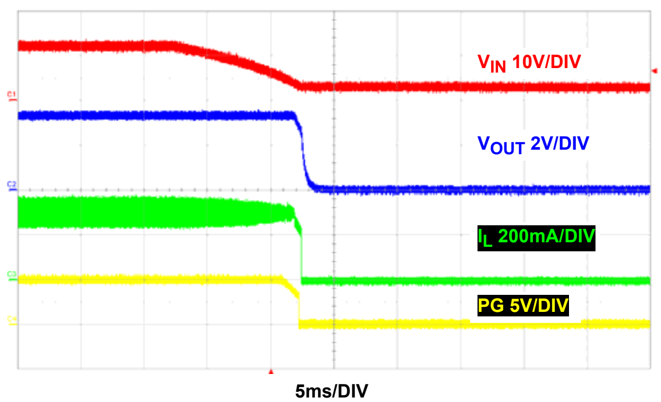


FIGURE 30. SHUTDOWN V_{IN} AT 300mA LOAD, PWM

Typical Performance Curves
V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 700kHz, T_A = +25°C, C_{IN} = 20µF, C_{OUT} = 22µF (Continued)

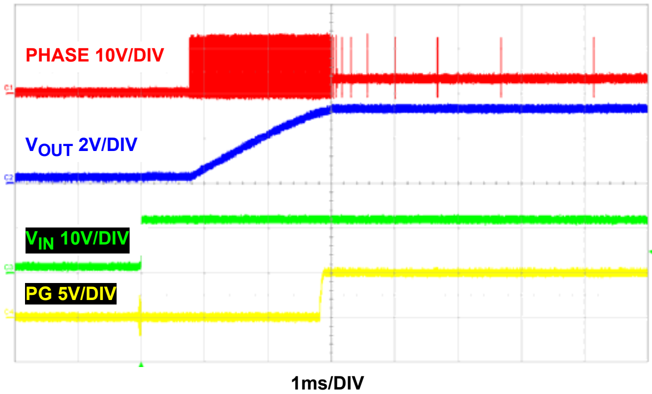


FIGURE 31. START-UP V_{IN} AT NO LOAD, PFM

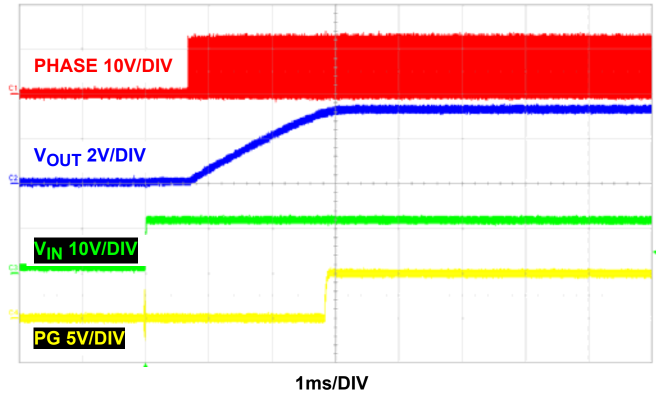


FIGURE 32. START-UP V_{IN} AT NO LOAD, PWM

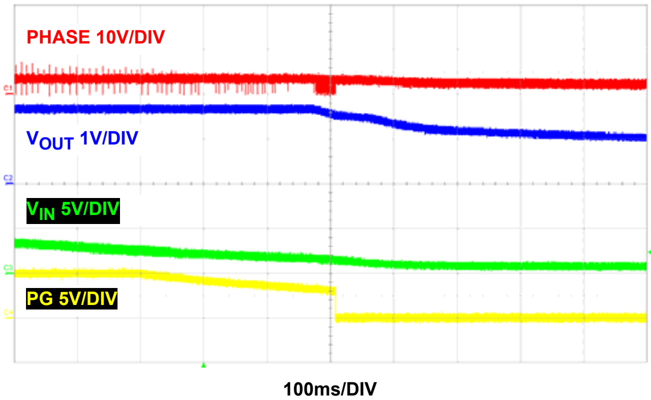


FIGURE 33. SHUTDOWN V_{IN} AT NO LOAD, PFM

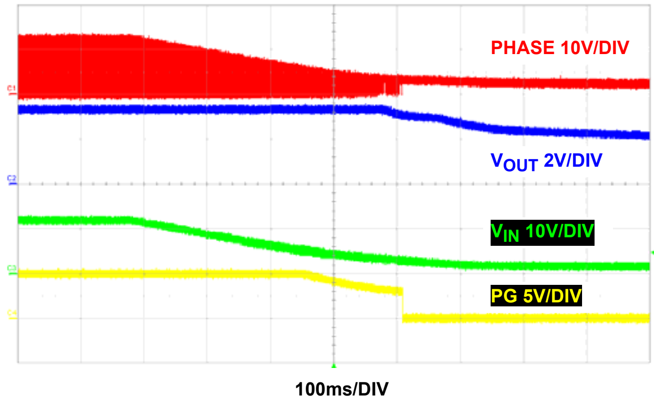


FIGURE 34. SHUTDOWN V_{IN} AT NO LOAD, PWM

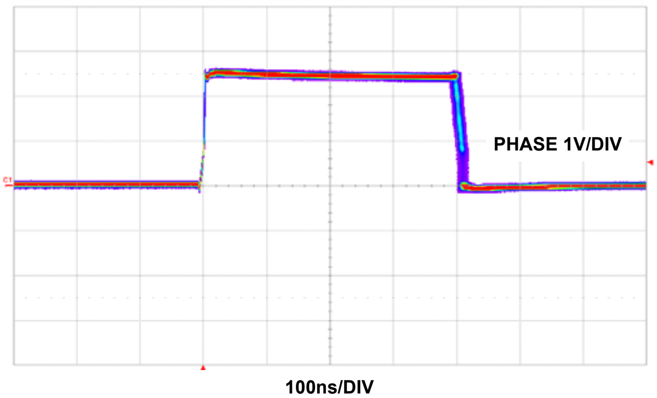


FIGURE 35. JITTER AT NO LOAD, PWM

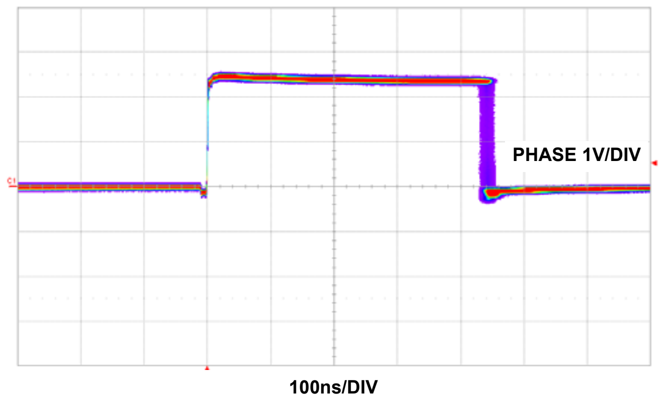


FIGURE 36. JITTER AT FULL LOAD, PWM

Typical Performance Curves V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 700kHz, T_A = +25°C, C_{IN} = 20µF, C_{OUT} = 22µF (Continued)

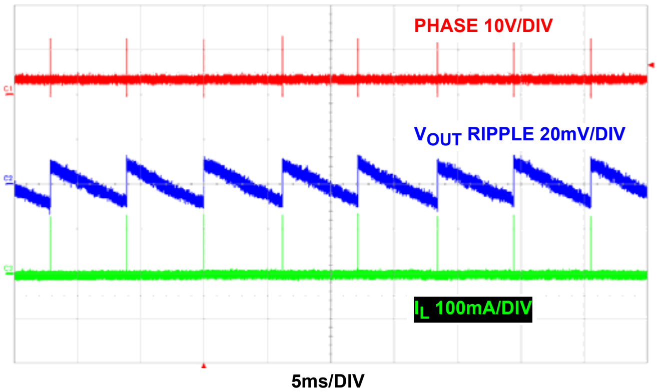


FIGURE 37. STEADY STATE AT NO LOAD, PFM

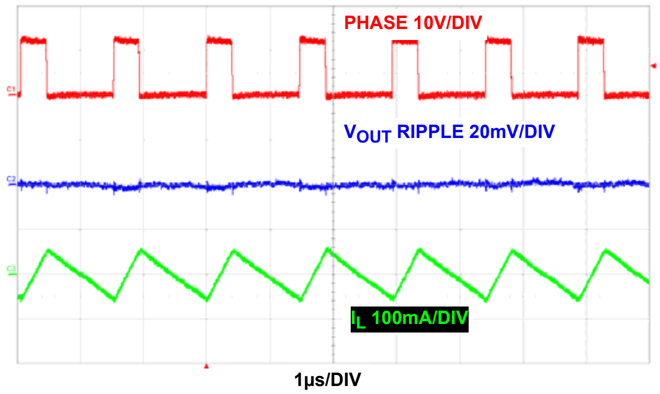


FIGURE 38. STEADY STATE AT NO LOAD, PWM

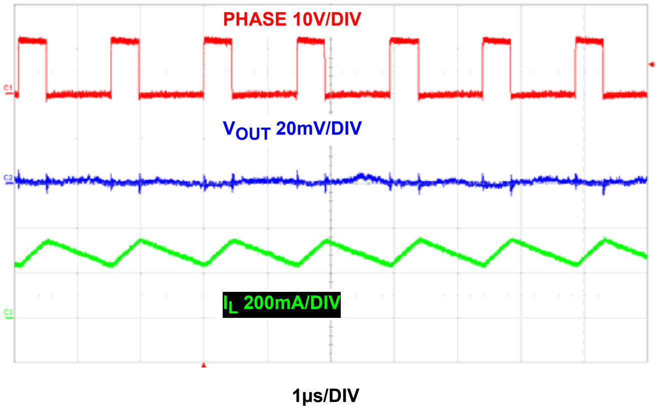


FIGURE 39. STEADY STATE AT 300mA LOAD, PWM

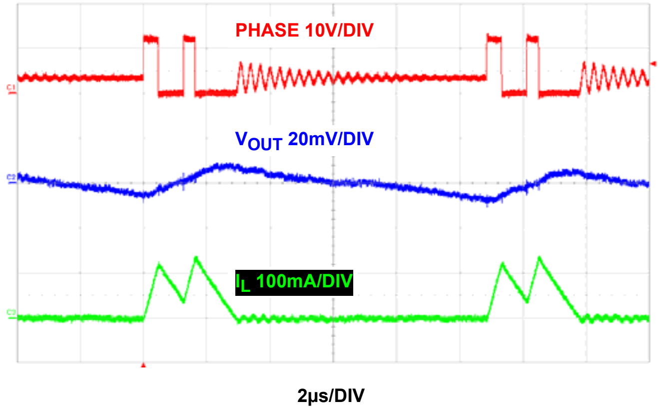


FIGURE 40. STEADY STATE AT 20mA LOAD, PFM

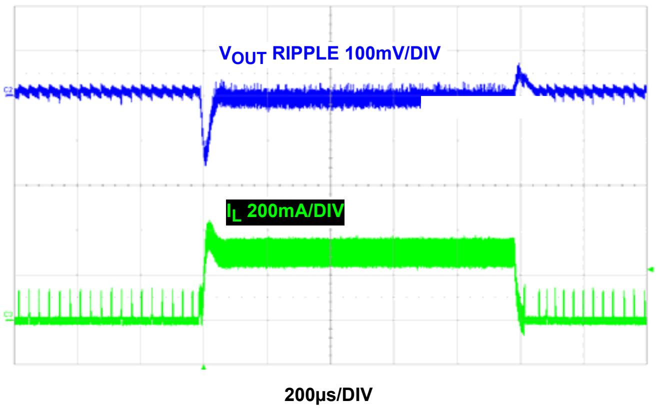


FIGURE 41. LOAD TRANSIENT, PFM

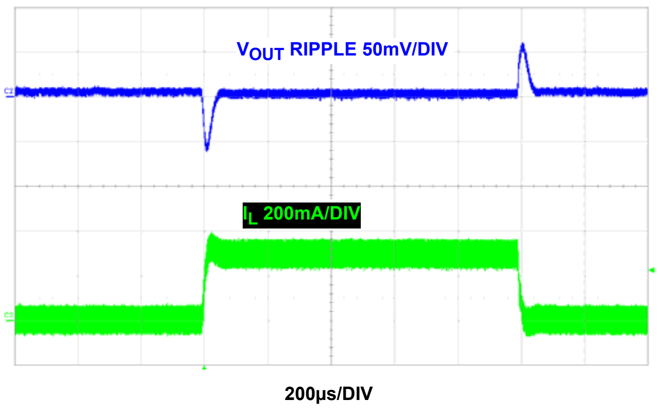


FIGURE 42. LOAD TRANSIENT, PWM

Typical Performance Curves V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 700kHz, T_A = +25°C, C_{IN} = 20µF, C_{OUT} = 22µF (Continued)

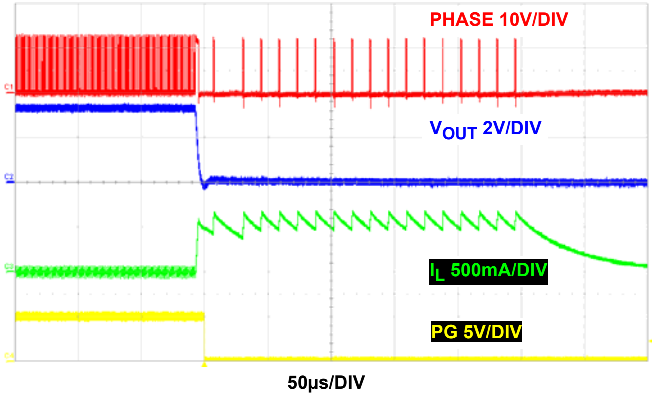


FIGURE 43. OUTPUT SHORT CIRCUIT

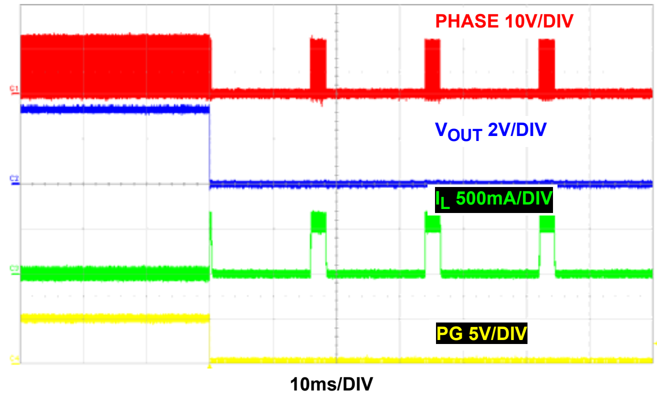


FIGURE 44. OVERCURRENT PROTECTION

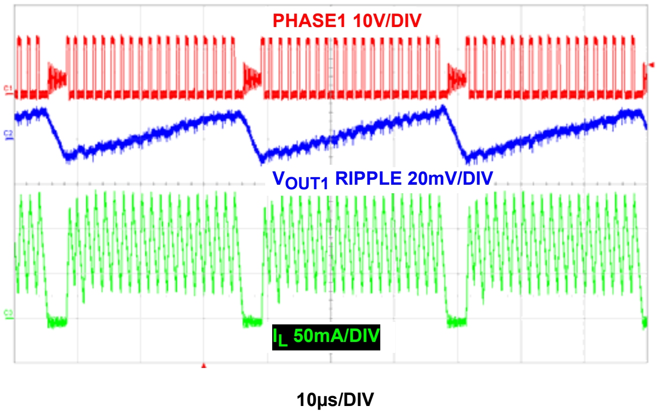


FIGURE 45. PFM TO PWM TRANSITION

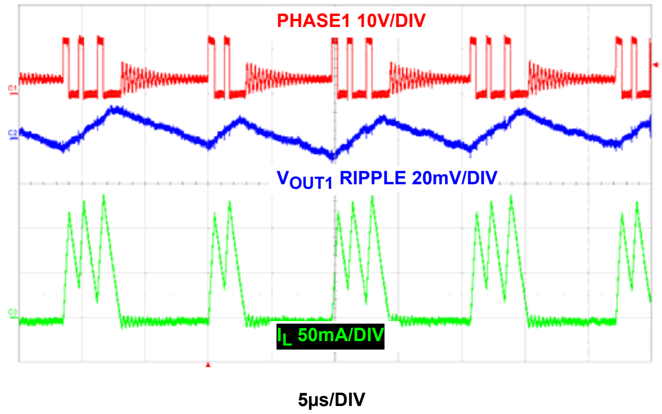


FIGURE 46. PWM TO PFM TRANSITION

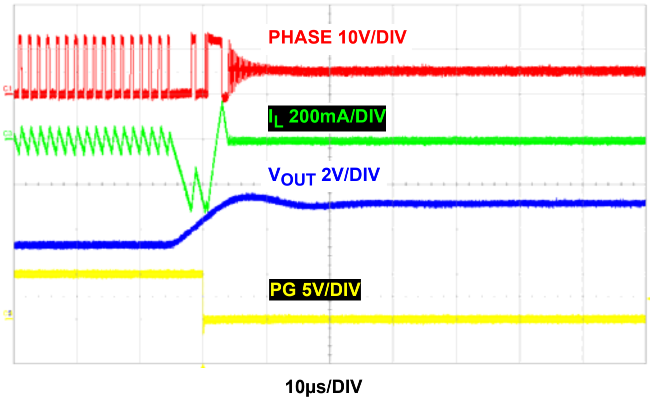


FIGURE 47. OVERVOLTAGE PROTECTION

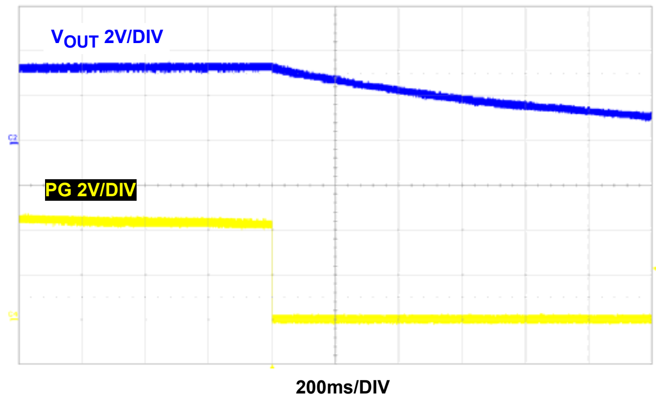


FIGURE 48. OVER-TEMPERATURE PROTECTION

Detailed Description

The ISL85413 combines a synchronous buck PWM controller with integrated power switches. The buck controller drives internal high-side and low-side N-channel MOSFETs to deliver load current up to 300mA. The buck regulator can operate from an unregulated DC source, such as a battery, with a voltage ranging from +3.5V to +40V. An internal LDO provides bias to the low voltage portions of the IC.

Peak current mode control is utilized to simplify feedback loop compensation and reject input voltage variation. User selectable internal feedback loop compensation further simplifies design. The ISL85413 switches at a default 700kHz.

The buck regulator is equipped with an internal current sensing circuit and the peak current limit threshold is typically set at 0.6A.

Power-On Reset

The ISL85413 automatically initializes upon receipt of the input power supply and continually monitors the EN pin state. If EN is held below its logic rising threshold, the IC is held in shutdown and consumes typically 1.8µA from the VIN supply. If EN exceeds its logic rising threshold, the regulator will enable the bias LDO and begin to monitor the VCC pin voltage. When the VCC pin voltage clears its rising POR threshold, the controller will initialize the switching regulator circuits. If VCC never clears the rising POR threshold, the controller will not allow the switching regulator to operate. If VCC falls below its falling POR threshold while the switching regulator is operating, the switching regulator will be shut down until VCC returns.

Soft-Start

To avoid large inrush current, V_{OUT} is slowly increased at startup to its final regulated value in 2.3ms.

Power-Good

PG is the open-drain output of a window comparator that continuously monitors the buck regulator output voltage via the FB pin. PG is actively held low when EN is low and during the buck regulator soft-start period. After the soft-start period completes, PG becomes high impedance provided the FB pin is within the range specified in the “Electrical Specifications” on page 6. Should FB exit the specified window, PG will be pulled low until FB returns. Over-temperature faults also force PG low until the fault condition is cleared by an attempt to soft-start. There is an internal 5MΩ internal pull-up resistor.

PWM Control Scheme

The ISL85413 employs peak current-mode pulse-width modulation (PWM) control for fast transient response and pulse-by-pulse current limiting, as shown in the “Functional Block Diagram” on page 4. The current loop consists of the current sensing circuit, slope compensation ramp, PWM comparator, oscillator and latch. Current sense transresistance is typically 930mV/A and slope compensation rate, Se, is typically 450mV/T where T is the switching cycle period. The control reference for the current loop comes from the error amplifier’s output.

A PWM cycle begins when a clock pulse sets the PWM latch and the upper FET is turned on. Current begins to ramp up in the upper FET and inductor. This current is sensed (V_{CSA}), converted to a voltage and summed with the slope compensation signal. This combined signal is compared to V_{COMP} and when the signal is equal to V_{COMP}, the latch is reset. Upon latch reset the upper FET is turned off and the lower FET turned on allowing current to ramp down in the inductor. The lower FET will remain on until the clock initiates another PWM cycle. Figure 49 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the current sense and slope compensation signal.

Output voltage is regulated as the error amplifier varies its output and thus output inductor current. The error amplifier is a transconductance type and its output is terminated with a series RC (150k/54pF) network to GND. The transconductance of the error amplifier is 50µs. Its noninverting input is internally connected to a 600mV reference voltage and its inverting input is connected to the output voltage via the FB pin and its associated divider network.

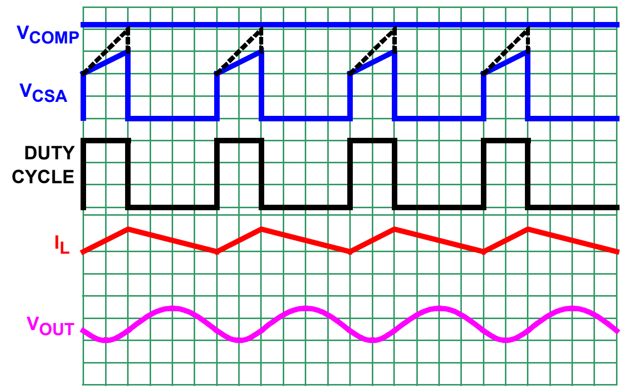


FIGURE 49. PWM OPERATION WAVEFORMS

Light Load Operation

At light loads, converter efficiency may be improved by enabling variable frequency operation (PFM). Connecting the MODE pin to GND will allow the controller to choose such operation automatically when the load current is low. Figure 50 shows the PFM operation. The IC enters the PFM mode of operation when 8 consecutive cycles of inductor current crossing zero are detected. This corresponds to a load current equal to 1/2 the peak-to-peak inductor ripple current and set by Equation 1:

$$I_{OUT} = \frac{V_{OUT}(1-D)}{2Lf_{SW}} \quad \text{(EQ. 1)}$$

where D = duty cycle, f_{SW} = switching frequency, L = inductor value, I_{OUT} = output loading current, V_{OUT} = output voltage.

While operating in PFM mode, the regulator controls the output voltage with a simple comparator and pulsed FET current. A comparator signals the point at which FB is equal to the 600mV reference at which time the regulator begins providing pulses of current until FB is moved above the 600mV reference by 1%. The current pulses are approximately 200mA and are issued at a frequency equal to the converter’s PWM operating frequency.

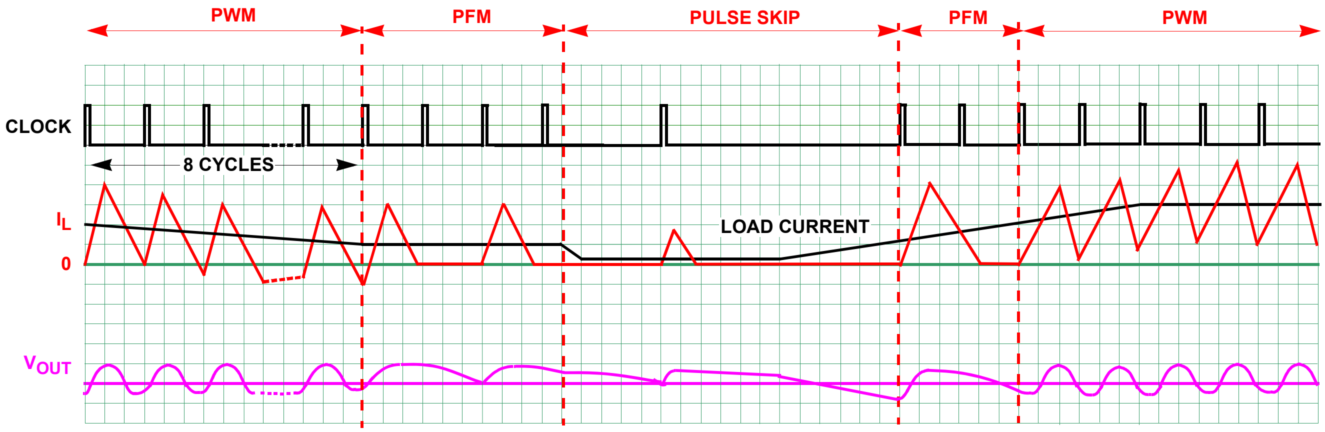


FIGURE 50. PFM MODE OPERATION WAVEFORMS

Due to the pulsed current nature of PFM mode, the converter can supply limited current to the load. Should load current rise beyond the limit, V_{OUT} will begin to decline. A second comparator signals an FB voltage 1% lower than the 600mV reference and forces the converter to return to PWM operation.

Output Voltage Selection

The regulator output voltage is easily programmed using an external resistor divider to scale V_{OUT} relative to the internal reference voltage. The scaled voltage is applied to the inverting input of the error amplifier; refer to Figure 51.

The output voltage programming resistor, R_2, depends on the value chosen for the feedback resistor, R_1, and the desired output voltage, V_{OUT}, of the regulator. Equation 2 describes the relationship between V_{OUT} and resistor values.

$$R_2 = \frac{R_1 x 0.6V}{V_{OUT} - 0.6V} \qquad \text{(EQ. 2)}$$

If the desired output voltage is 0.6V, then R_2 is left unpopulated and R_1 is 0Ω.

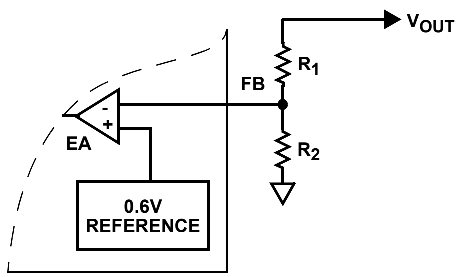


FIGURE 51. EXTERNAL RESISTOR DIVIDER

Protection Features

The ISL85413 is protected from overcurrent, negative overcurrent and over-temperature. The protection circuits operate automatically.

Overcurrent Protection

During PWM on-time, current through the upper FET is monitored and compared to a nominal 0.6A peak overcurrent limit. In the event that current reaches the limit, the upper FET will be turned off until the next switching cycle. In this way, FET peak current is always well limited.

If the overcurrent condition persists for 17 sequential clock cycles, the regulator will begin its hiccup sequence. In this case, both FETs will be turned off and PG will be pulled low. This condition will be maintained for 8 soft-start periods after which the regulator will attempt a normal soft-start.

Should the output fault persist, the regulator will repeat the hiccup sequence indefinitely. There is no danger even if the output is shorted during soft-start.

If V_{OUT} is shorted very quickly, FB may collapse below $5/8^{ths}$ of its target value before 17 cycles of overcurrent are detected. The ISL85413 recognizes this condition and will begin to lower its switching frequency proportional to the FB pin voltage. This insures that under no circumstance (even with V_{OUT} near 0V) will the inductor current run away.

Negative Current Limit

Should an external source somehow drive current into VOUT, the controller will attempt to regulate VOUT by reversing its inductor current to absorb the externally sourced current. In the event that the external source is low impedance, current may be reversed to unacceptable levels and the controller will initiate its negative current limit protection. Similar to normal overcurrent, the negative current protection is realized by monitoring the current through the lower FET. When the valley point of the inductor current reaches negative current limit, the lower FET is turned off and the upper FET is forced on until current reaches the positive current limit or an internal clock signal is issued. At this point, the lower FET is allowed to operate. Should the current again be pulled to the negative limit on the next cycle, the upper FET will again be forced on and current will be forced to 1/6th of the positive current limit. At this point the controller will turn off both FETs and wait for the error amplifier's output to indicate return to normal operation. During this time, the controller will apply a 100W load from PHASE to PGND and attempt to discharge the output. Negative current limit is a pulse-by-pulse style operation and recovery is automatic. Negative current limit protection is disabled in PFM operating mode because reverse current is not allowed to build due to the diode emulation behavior of the lower FET.

Over-Temperature Protection

Over-temperature protection limits maximum junction temperature in the ISL85413. When junction temperature (T_J) exceeds +150°C, both FETs are turned off and the controller waits for temperature to decrease by approximately 20°C. During this time PG is pulled low. When temperature is within an acceptable range, the controller will initiate a normal soft-start sequence. For continuous operation, the +125°C junction temperature rating should not be exceeded.

Boot Undervoltage Protection

If the Boot capacitor voltage falls below 1.8V, the Boot undervoltage protection circuit will turn on the lower FET for 400ns to recharge the capacitor. This operation may arise during long periods of no switching such as PFM no load situations. In PWM operation near dropout (V_{IN} near V_{OUT}), the regulator may hold the upper FET on for multiple clock cycles. To prevent the boot capacitor from discharging, the lower FET is forced on for approximately 200ns every 34 clock cycles.

Application Guidelines

Simplifying the Design

Table 1 on page 3 provides component value selections for a variety of output voltages and will allow the designer to implement solutions with a minimum of effort.

Output Inductor Selection

The inductor value determines the converter's ripple current. Choosing an inductor current requires a somewhat arbitrary choice of ripple current, ΔI. A reasonable starting point is 30% of total load current. The inductor value can then be calculated using Equation 3:

$$L = \frac{V_{IN} - V_{OUT}}{f_{SW} \times \Delta I} \times \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 3)}$$

Increasing the value of inductance reduces the ripple current and thus, the ripple voltage. However, the larger inductance value may reduce the converter's response time to a load transient. The inductor current rating should be such that it will not saturate in overcurrent conditions. For typical ISL85413 applications, inductor values generally lies in the 10µH to 47µH range. In general, higher V_{OUT} will mean higher inductance.

Buck Regulator Output Capacitor Selection

An output capacitor is required to filter the inductor current. The current mode control loop allows the use of low ESR ceramic capacitors and thus supports very small circuit implementations on the PC board. Electrolytic and polymer capacitors may also be used.

While ceramic capacitors offer excellent overall performance and reliability, the actual in-circuit capacitance must be considered. Ceramic capacitors are rated using large peak-to-peak voltage swings and with no DC bias. In the DC/DC converter application, these conditions do not reflect reality. As a result, the actual capacitance may be considerably lower than the advertised value. Consult the manufacturers data sheet to determine the actual in-application capacitance. Most manufacturers publish capacitance vs DC bias so that this effect can be easily accommodated. The effects of AC voltage are not frequently published, but an assumption of ~20% further reduction will generally suffice. The result of these considerations may mean an effective capacitance 50% lower than nominal and this value should be used in all design calculations. Nonetheless, ceramic capacitors are a very good choice in many applications due to their reliability and extremely low ESR.

The following equations allow calculation of the required capacitance to meet a desired ripple voltage level. Additional capacitance may be used.

For the ceramic capacitors (low ESR):

$$V_{OUTripple} = \frac{\Delta I}{8 * f_{SW} * C_{OUT}} \quad \text{(EQ. 4)}$$

where ΔI is the inductor's peak-to-peak ripple current, f_{SW} is the switching frequency and C_{OUT} is the output capacitor.

If using electrolytic capacitors then:

$$V_{OUTripple} = \Delta I * ESR \quad \text{(EQ. 5)}$$

Layout Considerations

Proper layout of the power converter will minimize EMI and noise and insure first pass success of the design. PCB layouts are provided in multiple formats on the Intersil web site. In addition, Figure 52 will make clear the important points in PCB layout. In reality, PCB layout of the ISL85413 is quite simple.

A multi-layer printed circuit board with GND plane is recommended. Figure 52 shows the connections of the critical components in the converter. Note that capacitors C_{IN} and C_{OUT} could each represent multiple physical capacitors. The most critical connections are to tie the PGND pin to the package GND pad and then use vias to directly connect the GND pad to the system GND plane. This connection of the GND pad to system plane insures a low impedance path for all return current, as well as an excellent thermal path to dissipate heat. With this connection made, place the high frequency MLCC input capacitor near the VIN pin and use vias directly at the capacitor pad to tie the capacitor to the system GND plane.

The boot capacitor is easily placed on the PCB side opposite the controller IC and 2 vias directly connect the capacitor to BOOT and PHASE.

Place a 1µF MLCC near the VCC pin and directly connect its return with a via to the system GND plane.

Place the feedback divider close to the FB pin and do not route any feedback components near PHASE or BOOT.

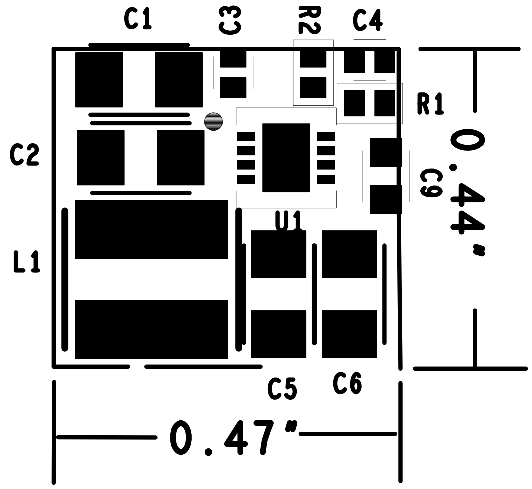


FIGURE 52. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
March 13, 2015	FN8379.1	On page 1, updated all 36V references to 40V. On page 5, under “Absolute Maximum Ratings”: for VIN to GND updated max from “+42V” to “+43V” for PHASE to GND updated max from “43V” to “+44V” for EN to GND updated max from “+42V” to “+43V” Under “Recommended Operating Conditions” updated supply voltage max from “36V” to “+40V”. In “Electrical Specifications”updated all occurrences of VIN value from “36V” to “40V”. On page 15, under the “Detailed Description” section updated voltage range max from “+36V” to “+40V”.
April 11, 2014	FN8379.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

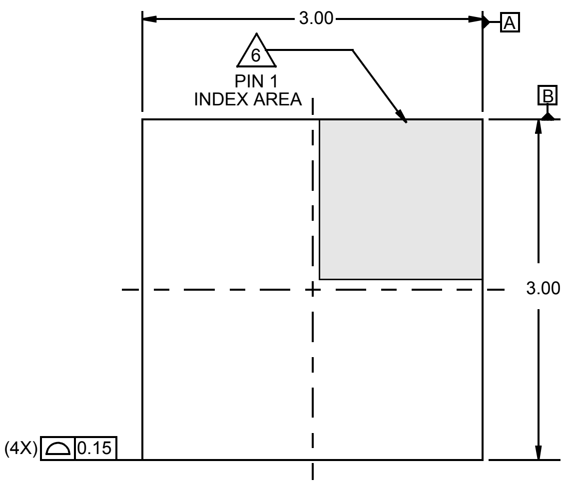
You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

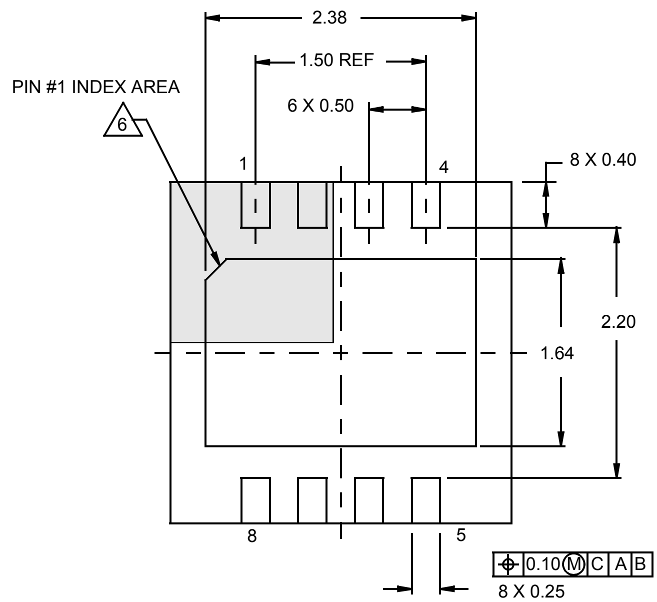
Package Outline Drawing

L8.3x3H

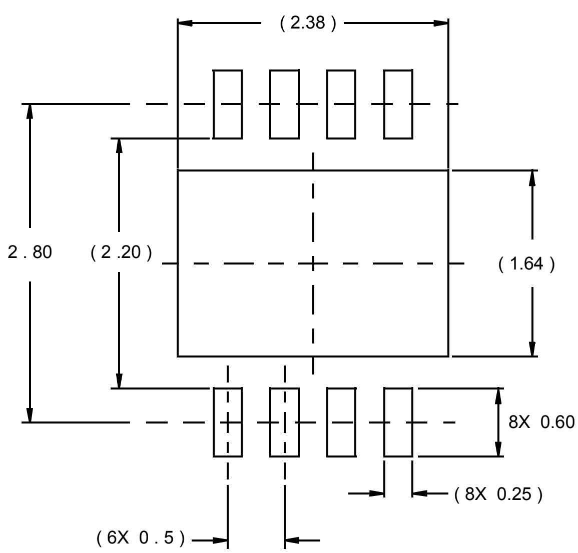
8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE (TDFN)
Rev 0, 2/08



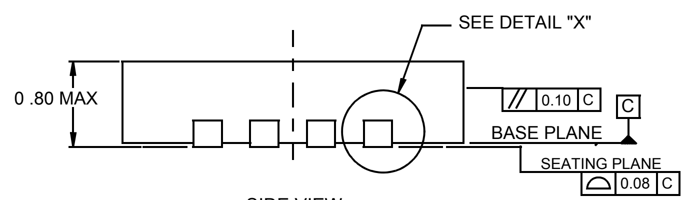
TOP VIEW



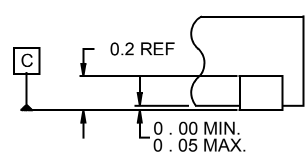
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Lead width dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.