CDB4353

Evaluation Board for the CS4353

Features

- Demonstrates Recommended Layout and Grounding Arrangements
- CS8416 Receives S/PDIF, & EIAJ-340-Compatible Digital Audio
- Headers for External PCM Audio
- Single-ended Stereo Analog Outputs
- Requires Only a Digital Signal Source and a +3.3 V Power Supply for a Complete Digital-to-Analog Converter System
- Configured by On-board Hardware Controls
- Power, Digital Source Select, and S/PDIF Error Indicator LEDs
- Current Sense Resistors for CS4353 Supplies (VA, VL, and VCP)

Description

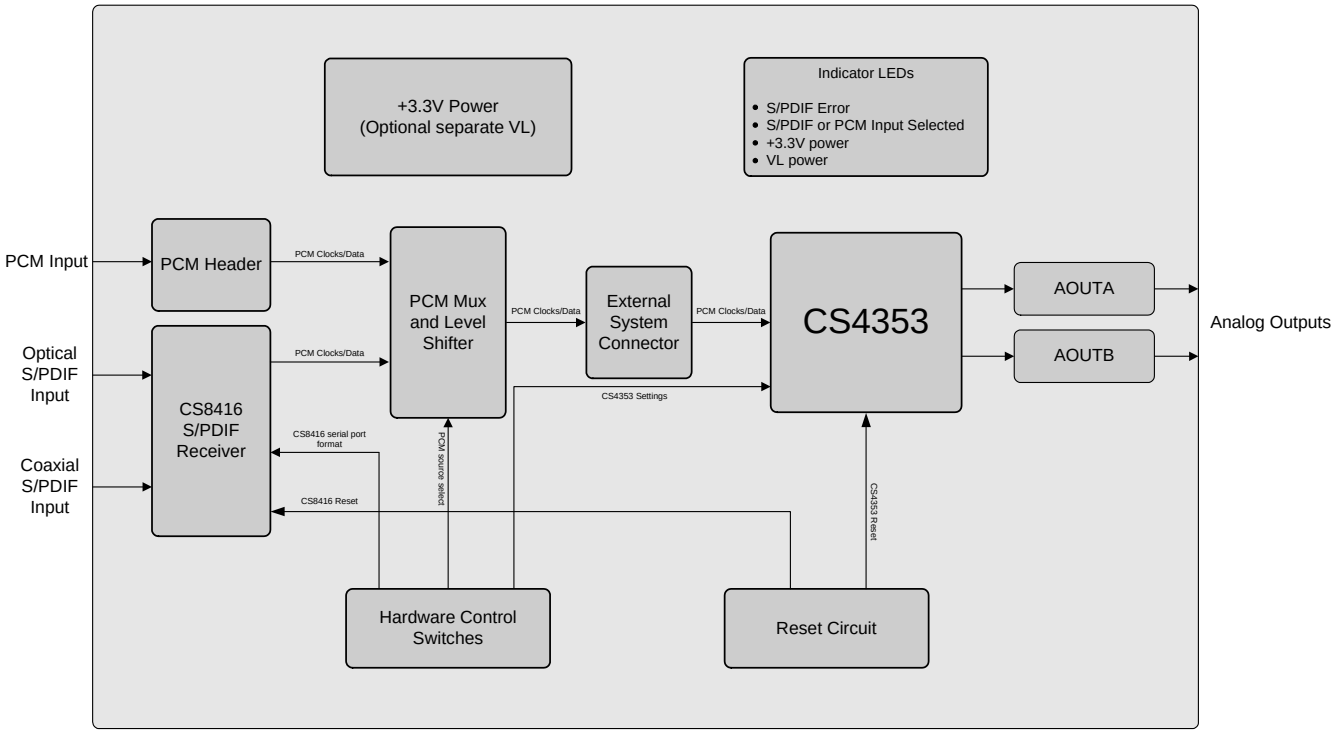
The CDB4353 evaluation board is an excellent means for quickly evaluating the CS4353 24-bit, high-performance stereo D/A converter. Evaluation requires an analog signal analyzer, a digital signal source, and a +3.3 V power supply. Analog line-level outputs are provided via RCA phono jacks.

The CS8416 digital audio receiver IC provides the system timing necessary to operate the Digital-to-Analog converter and will accept S/PDIF and EIAJ-340-compatible audio data. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

The CDB4353 is controlled by switches to select the digital signal source and configuration options for the CS4353. Current sense resistors allow for easy power calculations during system development.

ORDERING INFORMATION

CDB4353 Evaluation Board



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1. CDB4353 SYSTEM OVERVIEW

The CDB4353 evaluation board is an excellent means of quickly evaluating the CS4353. The CS8416 digital audio interface receiver provides an easy interface to digital audio signal sources, including the majority of digital audio test equipment. The evaluation board also allows the user to supply external PCM clocks and data through two separate header options for system development. Configuration of the CDB4353 can be modified through piano switch S1, see Table 4. The CDB4353 system block diagram and signal flow is shown in Figure 31, and the CDB4353 schematics are shown in Figures 32 and 33.

2. CS4353 DIGITAL-to-ANALOG CONVERTER

A description of the CS4353 is included in the CS4353 datasheet.

3. CS8416 DIGITAL AUDIO RECEIVER

The system receives and decodes the standard S/PDIF data format using a CS8416 Digital Audio Receiver, Figure 32. The outputs of the CS8416 include a serial bit clock, serial data, left-right clock, and a 128/256 Fs master clock. The operation of the CS8416 and a discussion of the digital audio interface is included in the CS8416 datasheet.

The evaluation board has been designed such that the input can be either optical or coaxial, see Figure 32. However, both inputs cannot be driven simultaneously.

Position 3 of piano switch S1 sets the CS8416 output data format to either I²S (down) or LJ (up). Position 2 of S1 sets the output MCLK to LRCK ratio of the CS8416. This switch should be set to 256 (down) for input Fs<=48 kHz and can be either 256 (down) or 128 (up) for Fs>48 kHz. The CS8416 must be manually reset via S2 after either switch has been toggled for the change to take effect.

4. INPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow interfacing to external systems via headers J13 and J4. Header J13 allows the evaluation board to accept externally generated PCM clocks and data at a nominal voltage of 3.3 V. The PCM clocks and data are buffered, level-shifted to the VL supply, and then input to the CS4353. The schematic for the clock/data input is shown in Figure 33. Position 1 of S1 selects the CS4353 PCM source as either the CS8416 (up) or header J13 (down).

Note: If the VL supply is set to a low voltage level (VL<1.8 V), termination resistors may need to be added to the J13 header signals to match the source and transmission-line impedances that are driving the header. This may be accomplished by soldering resistors across the rows of J13 on the back of the evaluation board.

Header J4 bypasses position 1 of S1 and allows for a direct connection of PCM clocks and data to the CS4353. Under normal operation, shunts placed across the left two rows of J4 connects the PCM clocks and data from the source specified by position 1 of S1 to the CS4353. An external system can be directly connected to the CS4353 by removing the shunts on J4 and connecting PCM clocks and data across the right two rows of J4 using a ribbon cable. A single row of “GND” pins are provided to maintain signal ground integrity. Signals input to header J4 must be at the same voltage level as the VL supply on the evaluation board. The schematic for the header J4 and CS4353 is shown in Figure 32.

Please see the CS4353 datasheet for more information on clocking data into the CS4353.

5. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by two binding posts, GND and +3.3 V (see Figure 33). The allowable input voltage range for the binding posts is 3.13 V to 3.47 V. The VL supply can be connected to the +3.3 V binding post by shunting J1 or provided externally by removing the shunt on J1 and connecting another voltage to pin 2 of J1 (labeled VL). VCP and VA are normally supplied by the 3.3 V binding post but can be set to separate voltages by removing the shunts on J8 and J10, removing R9 and R14, and then applying external voltages to pin 1 of J8 and J10.

Power consumption of the CS4353 can be measured through the voltage drop at J8, J9, and J10 when the shunts are removed.

WARNING: Refer to the CS4353 datasheet for maximum allowable voltages levels. Operation outside of this range can cause permanent damage to the device.

6. GROUNDING AND POWER SUPPLY DECOUPLING

As with any high-performance converter, the CS4353 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 32 details the connections to the CS4353 and Figures 34, 35, and 36 show the component placement and top and bottom layout. The decoupling capacitors are located as close to the CS4353 as possible.

7. HARDWARE CONTROL

The CDB4353 is controlled through settings on switch S1. This allows for configuration of the board without a PC. Switch S1 can toggle settings for CS8416 MCLK speed, CS8416 and CS4353 PCM data format, clock and data source for the board, and the Hardware Mode configuration of the CS4353. Table 1 below shows S1 settings for S/PDIF input and PCM input header quick setup modes. See Table 4 for details on each switch S1 setting.

S1 POSITION	S/PDIF INPUT - OPT1 or J16	PCM INPUT - J3
1	Up	Down
2	Down	Down
3	Down	Down
4	Up	Up
5	Down	Down

Table 1. Switch S1 Quick Setup

8. CS8416 AND CS4353 RESET

Pressing switch S2 resets the CS8416. Jumper J5 sets whether the CS4353 is reset by switch S2 (External) or by the CS4353's internal power-on reset function (POR).

9. ANALOG OUTPUT FILTERING

The analog output on the CDB4353 has been designed according to the CS4353 datasheet. This output circuit consists of a single-pole R and C filter. J11 selects the output ground reference for the CS4353. The output reference can be set to the evaluation board's ground (shunted) or J14 and J15's ground connection (not shunted). See Figure 33 for details of CS4353 output filter.

10.BOARD CONNECTIONS AND SETTINGS

Board connections and settings are shown in Table 2, Table 3, and Table 4 below.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
3.3 V - J3	Input	+3.3 V power for the evaluation board
GND - J2	Input	Ground connection from power supply
SPDIF INPUT - J16	Input	Digital audio interface input via coaxial cable
SPDIF INPUT - OPT1	Input	Digital audio interface input via optical cable
PCM INPUT - J13	Input	Input for master, serial, left/right clocks and serial data
EXT SYS CONN - J4	Input	Input for master, serial, left/right clocks and serial data - direct to CS4353
AOUTA - J14 AOUTB - J15	Output	RCA line-level analog outputs

Table 2. System Connections

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
J1	Selects source of voltage for the VL supply	*shunted not shunted	Voltage source is +3.3 V binding post (J3) Voltage source is pin 2 of J1
J8	Current measure for VCP	*shunted	When shunt is removed, the voltage can be measured across a fixed resistance to determine current.
J9	Current measure for VL	*shunted	When shunt is removed, the voltage can be measured across a fixed resistance to determine current.
J10	Current measure for VA	*shunted	When shunt is removed, the voltage can be measured across a fixed resistance to determine current.
J5	CS4353 Reset Select	*EXTERNAL POR	CS4353 reset by S2 CS4353 uses internal power-on reset
J11	CS4353 Output Reference	*shunted not shunted	Output reference is board ground Output reference is J14 and J15 ground

Table 3. CDB4353 Jumper Settings

SWITCH	PURPOSE	POSITION	FUNCTION SELECTED
S1	Selects PCM source for CS4353	1	down = PCM Header J3 *up = CS8416
	CS8416 MCLK/LRCK Ratio	2	*down = MCLK is 256xFs up = MCLK is 128xFs
	CS8416 and CS4353 PCM Format	3	*down = I^2S up = LJ
	CS4353 Output Amplitude	4	down = 1 V_{rms} output *up = 2 V_{rms} output
	CS4353 De-emphasis select	5	*down = De-emphasis off up = De-emphasis on
S2	Resets CS4353 and CS8416	-	CS8416 must be reset if switch S1 position 2 or 3 is changed

Table 4. CDB4353 Switch Settings

Note: All settings denoted by an asterisk (*) are the Default Factory Settings.

11.PERFORMANCE PLOTS

Test conditions (unless otherwise specified): TA = 25°C; VCP = VA = VL = 3.3 V; AGND = DGND =CPGND = 0 V; OPT1 S/PDIF input source; PCM data Left-Justified format; 2 V_{RMS} output; De-emphasis off; input test signal is a 997 Hz sine wave at 0 dBFS; dB values relative to 2.1 V_{RMS} full-scale output; measurement bandwidth 10 Hz to 20 kHz. CDB4353 revision A3 with CS4353 revision B1 used.

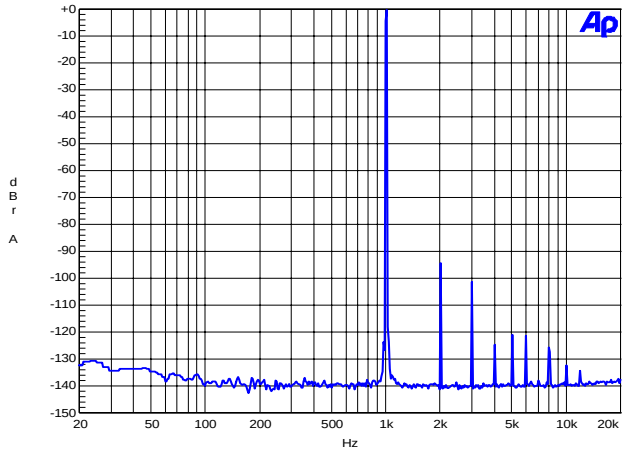

Figure 1. FFT (48 kHz, 0 dB)

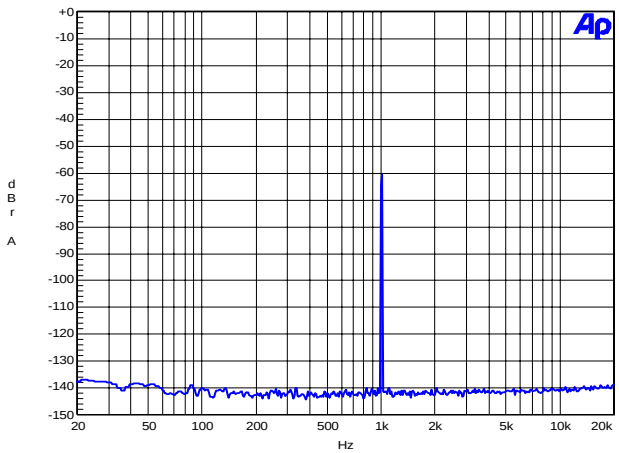

Figure 2. FFT (48 kHz, -60 dB)

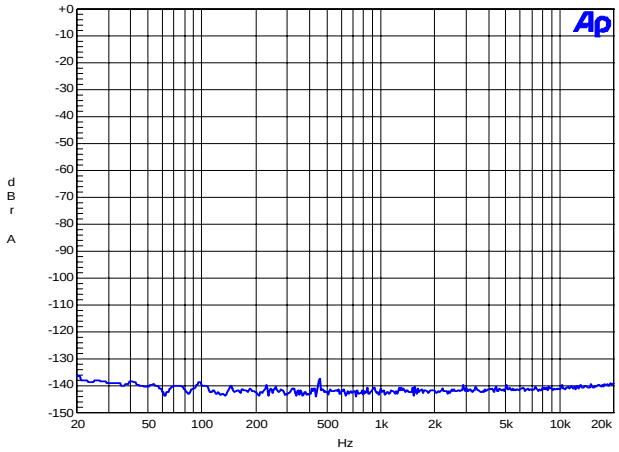

Figure 3. FFT (48 kHz, No Input)

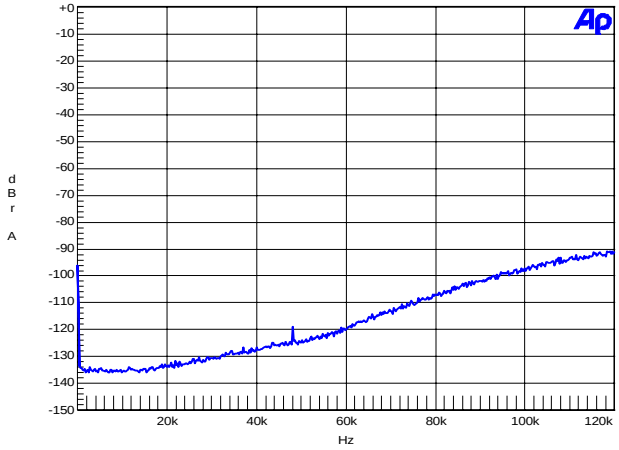

Figure 4. FFT (48 kHz Out-of-Band, No Input)

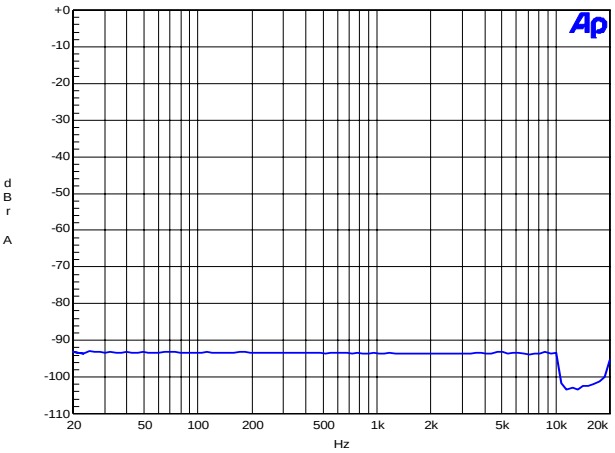

Figure 5. 48 kHz, THD+N vs. Input Freq

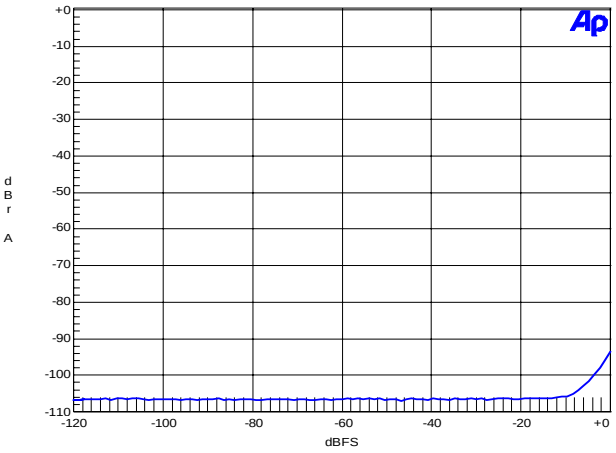

Figure 6. 48 kHz, THD+N vs. Level

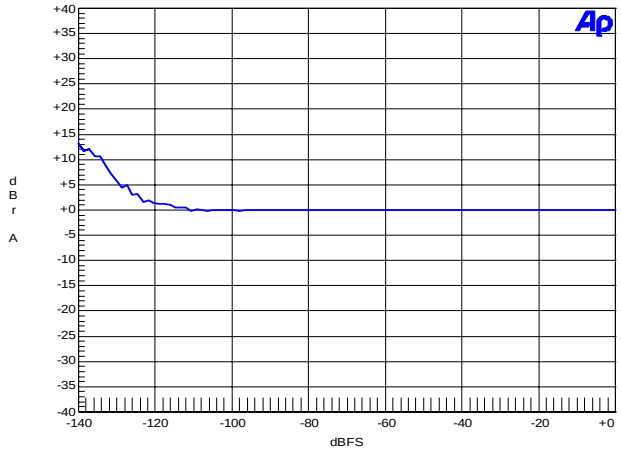

Figure 7. 48 kHz, Fade-to-Noise Linearity

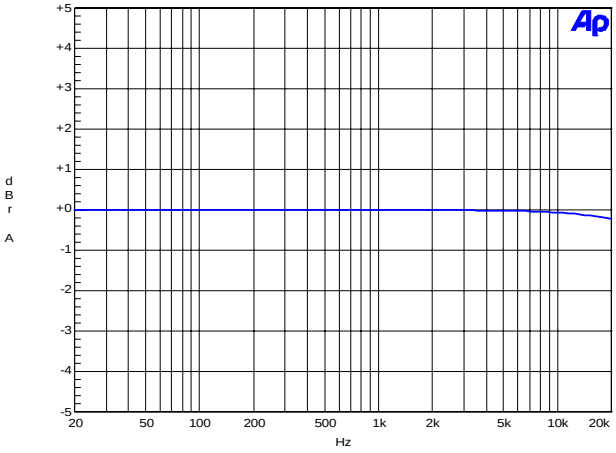

Figure 8. 48 kHz, Frequency Response

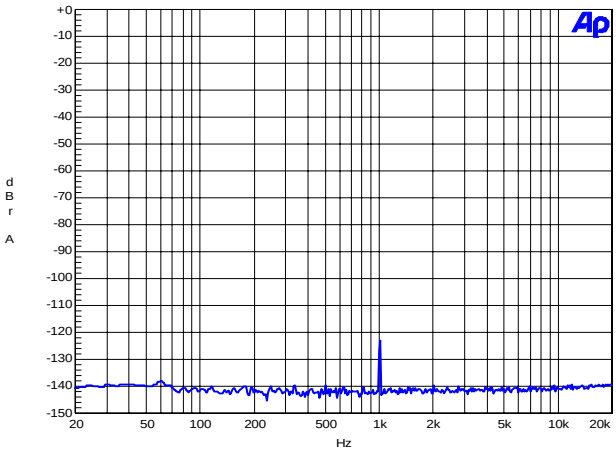

Figure 9. 48 kHz, Crosstalk

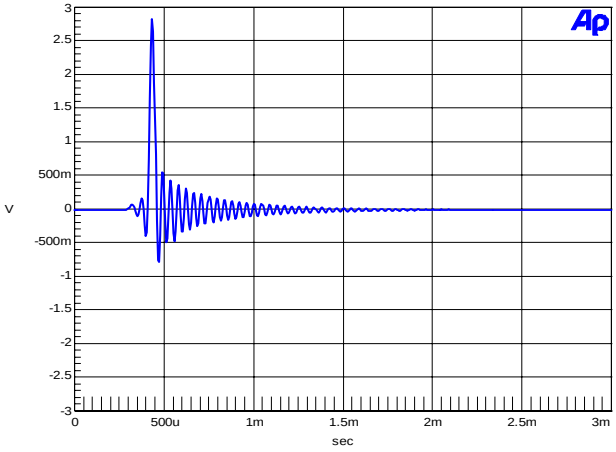

Figure 10. 48 kHz, Impulse Response

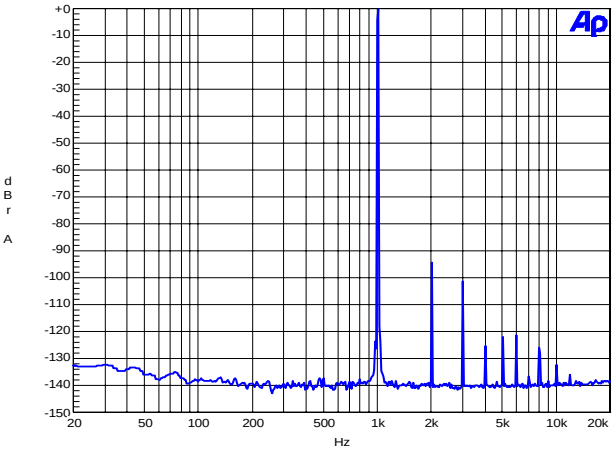

Figure 11. FFT (96 kHz, 0 dB)

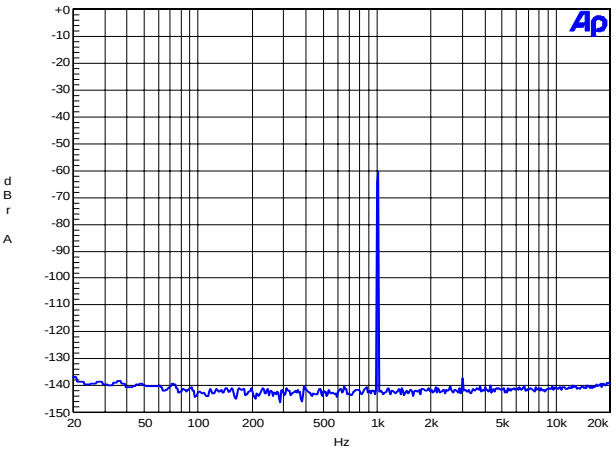

Figure 12. FFT (96 kHz, -60 dB)

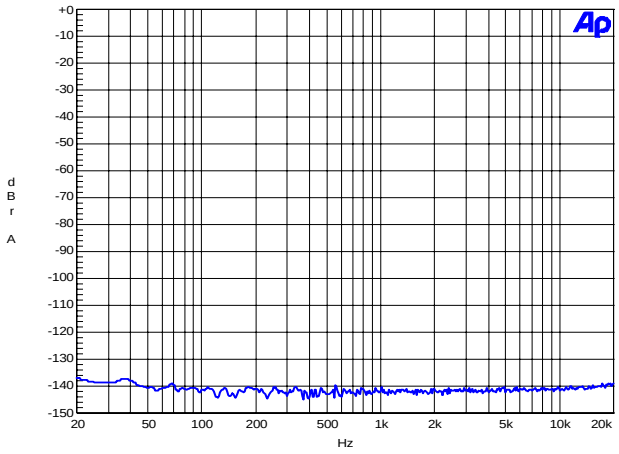

Figure 13. FFT (96 kHz, No Input)

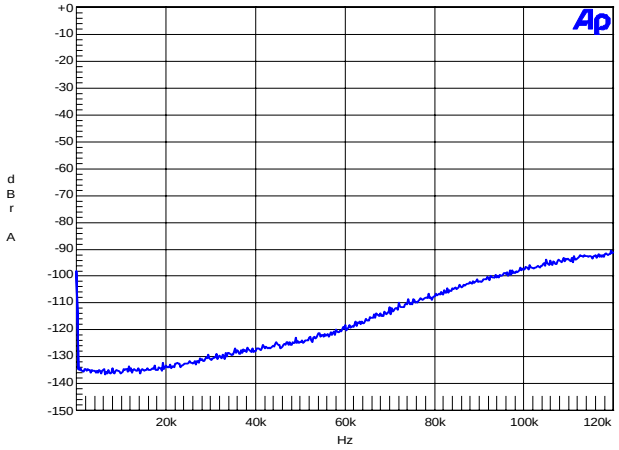

Figure 14. FFT (96 kHz Out-of-Band, No Input)

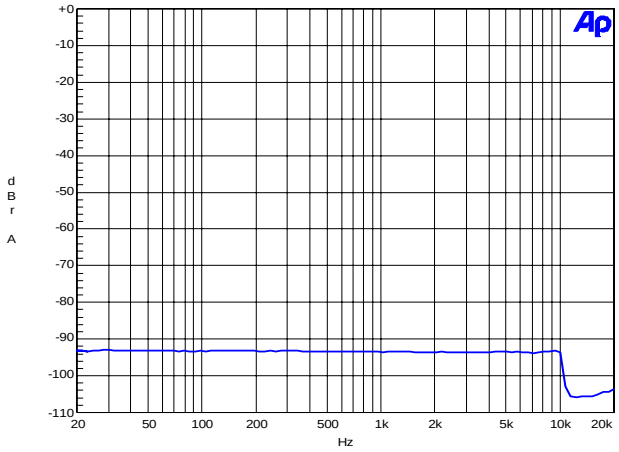

Figure 15. 96 kHz, THD+N vs. Input Freq

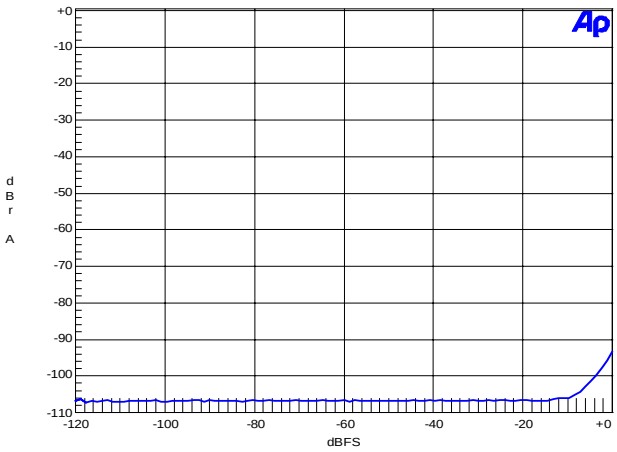

Figure 16. 96 kHz, THD+N vs. Level

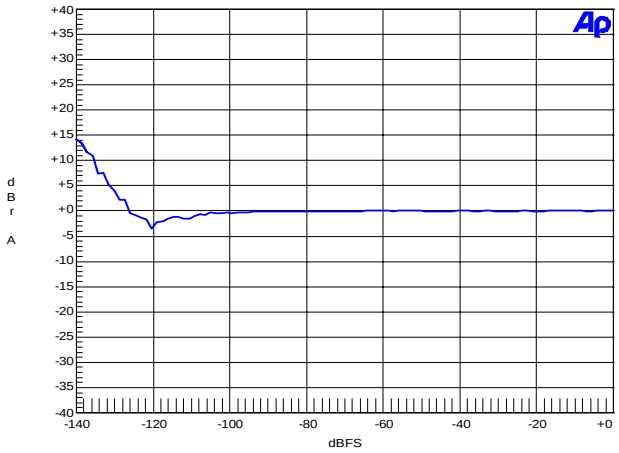

Figure 17. 96 kHz, Fade-to-Noise Linearity

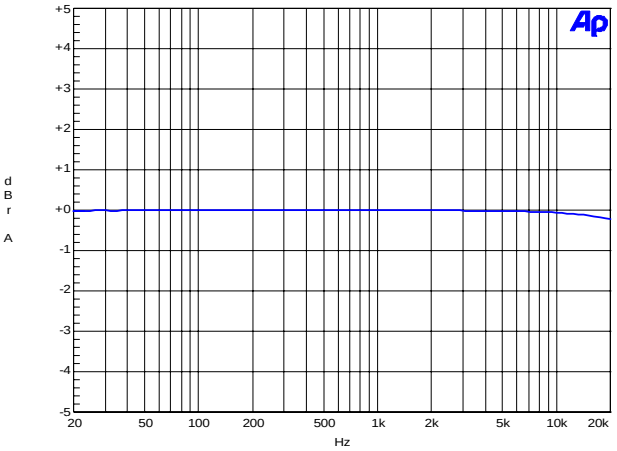

Figure 18. 96 kHz, Frequency Response

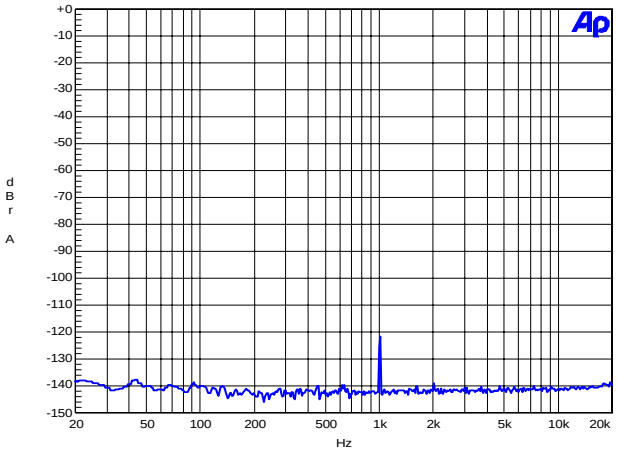

Figure 19. 96 kHz, Crosstalk

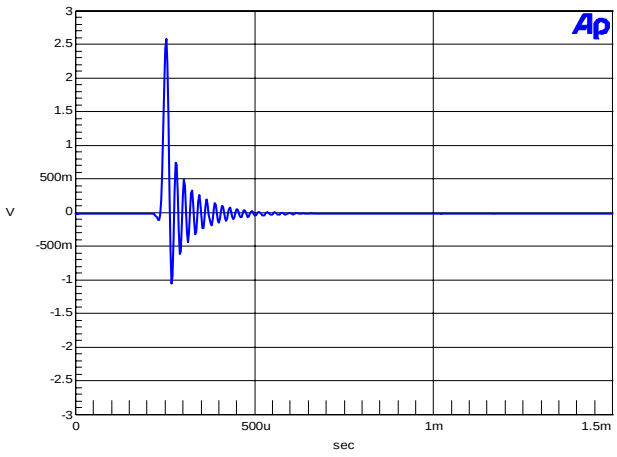

Figure 20. 96 kHz, Impulse Response

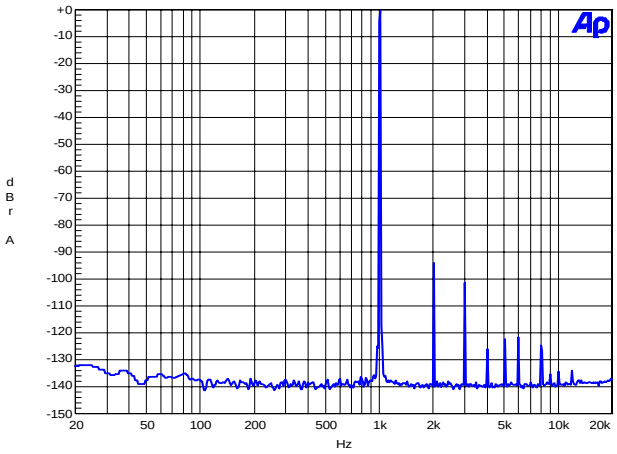

Figure 21. FFT (192 kHz, 0 dB)

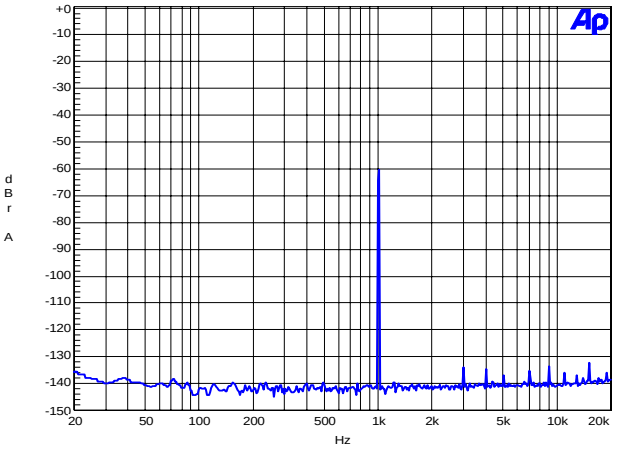

Figure 22. FFT (192 kHz, -60 dB)

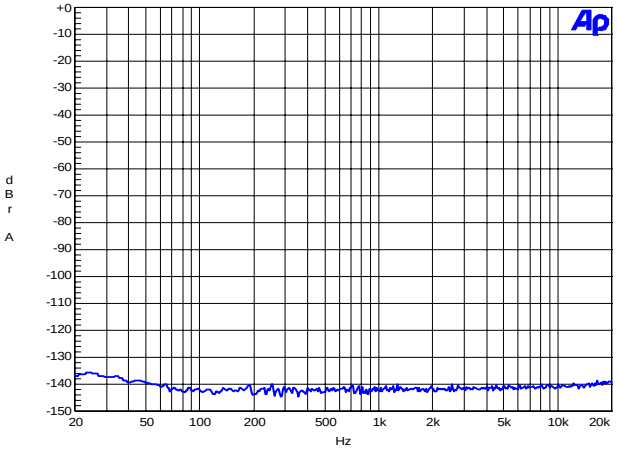

Figure 23. FFT (192 kHz, No Input)

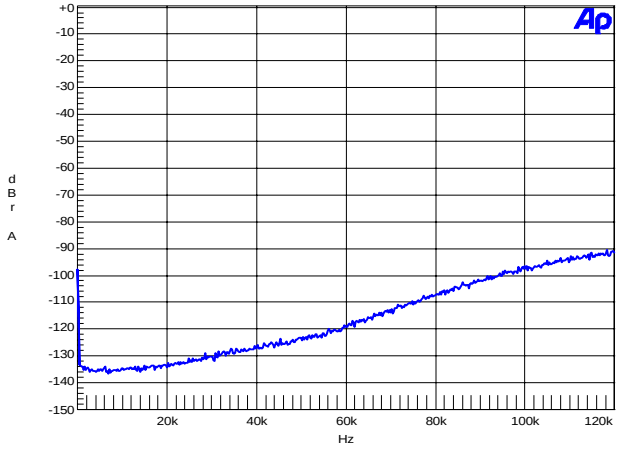

Figure 24. FFT (192 kHz Out-of-Band, No Input)

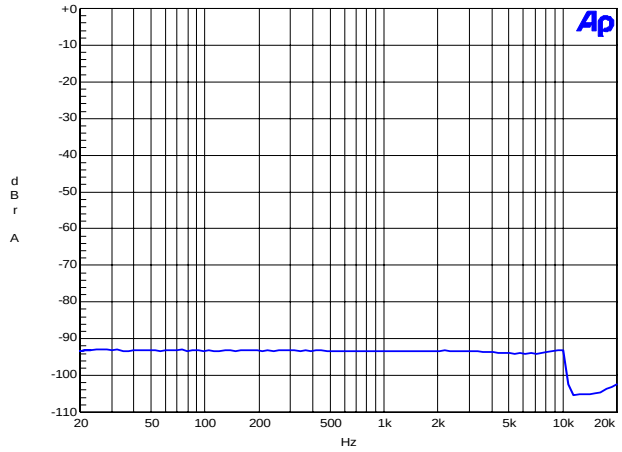

Figure 25. 192 kHz, THD+N vs. Input Freq

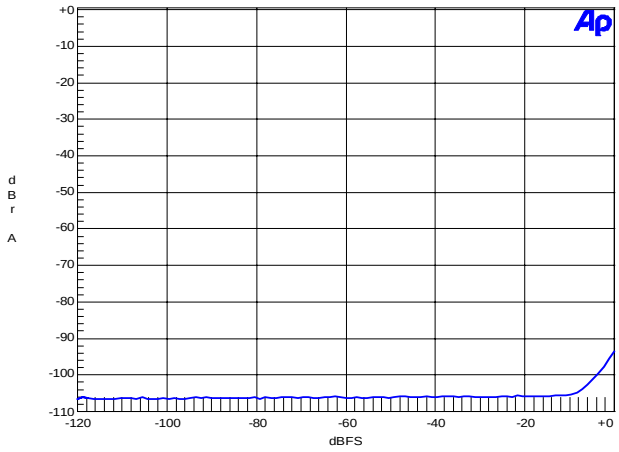

Figure 26. 192 kHz, THD+N vs. Level

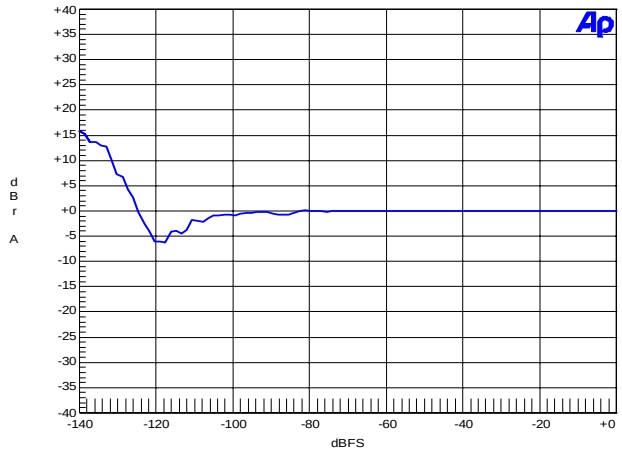

Figure 27. 192 kHz, Fade-to-Noise Linearity

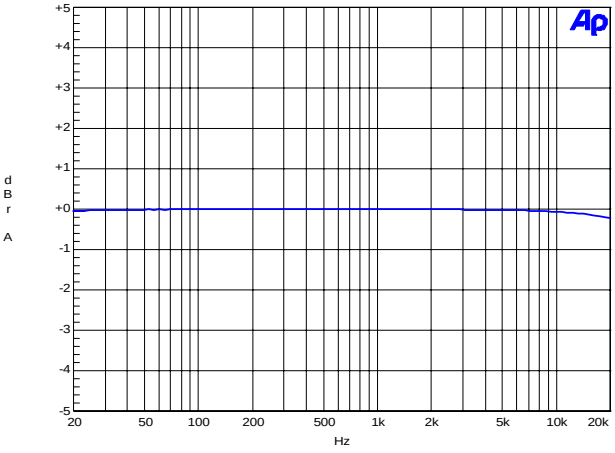

Figure 28. 192 kHz, Frequency Response

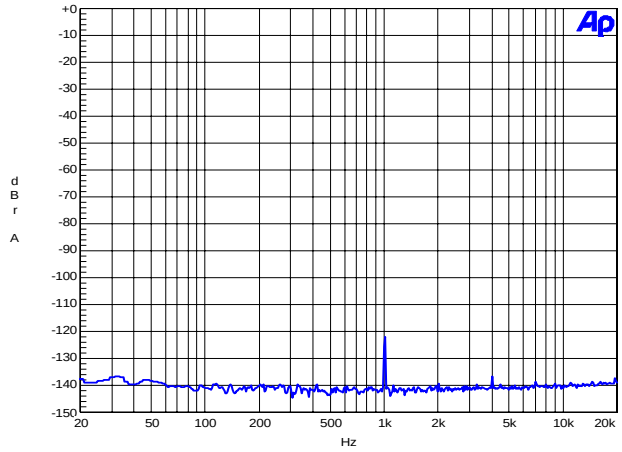

Figure 29. 192 kHz, Crosstalk

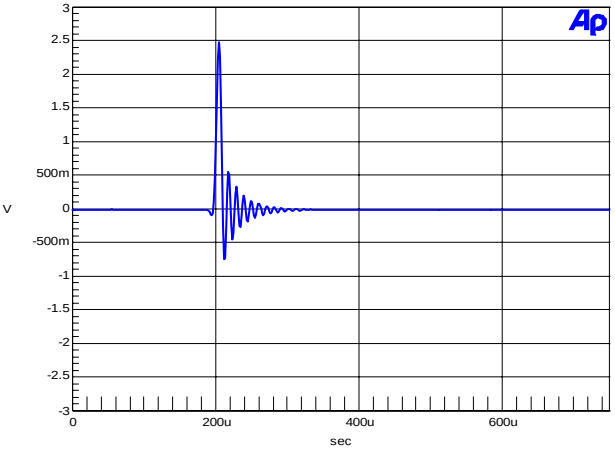

Figure 30. 192 kHz, Impulse Response

12.SCHEMATICS AND LAYOUT

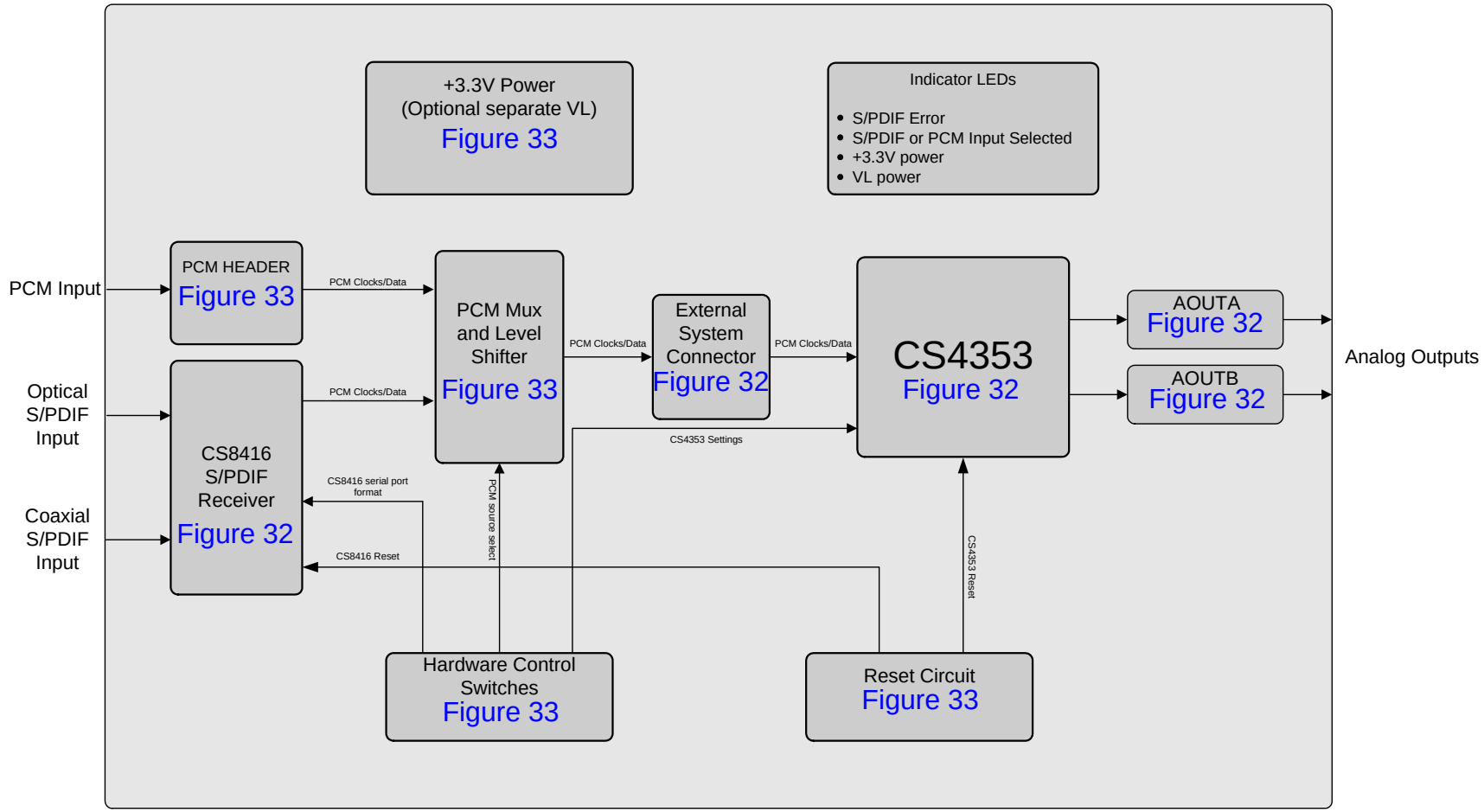

Figure 31. System Block Diagram and Signal Flow

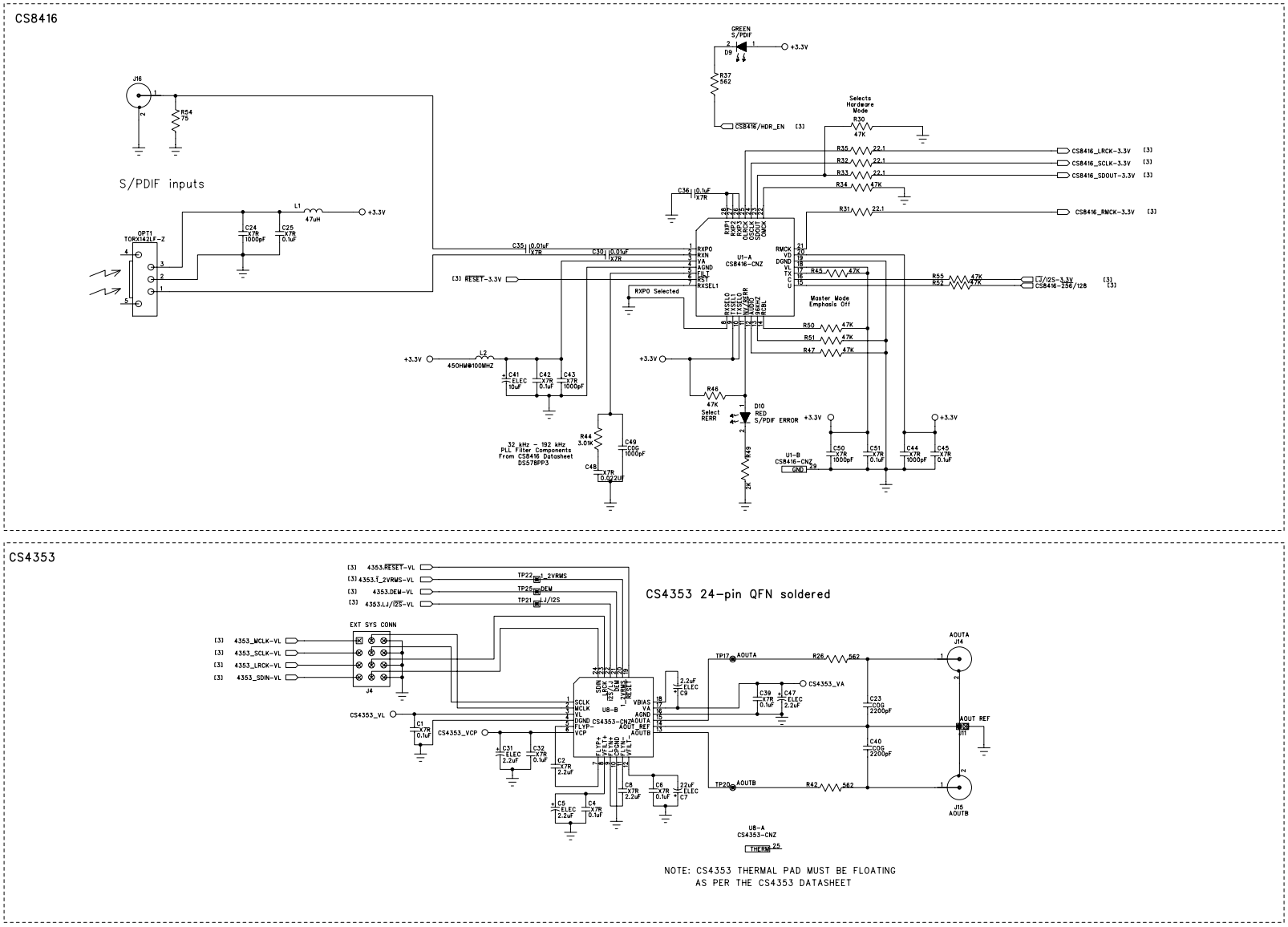

Figure 32. CS8416 and CS4353

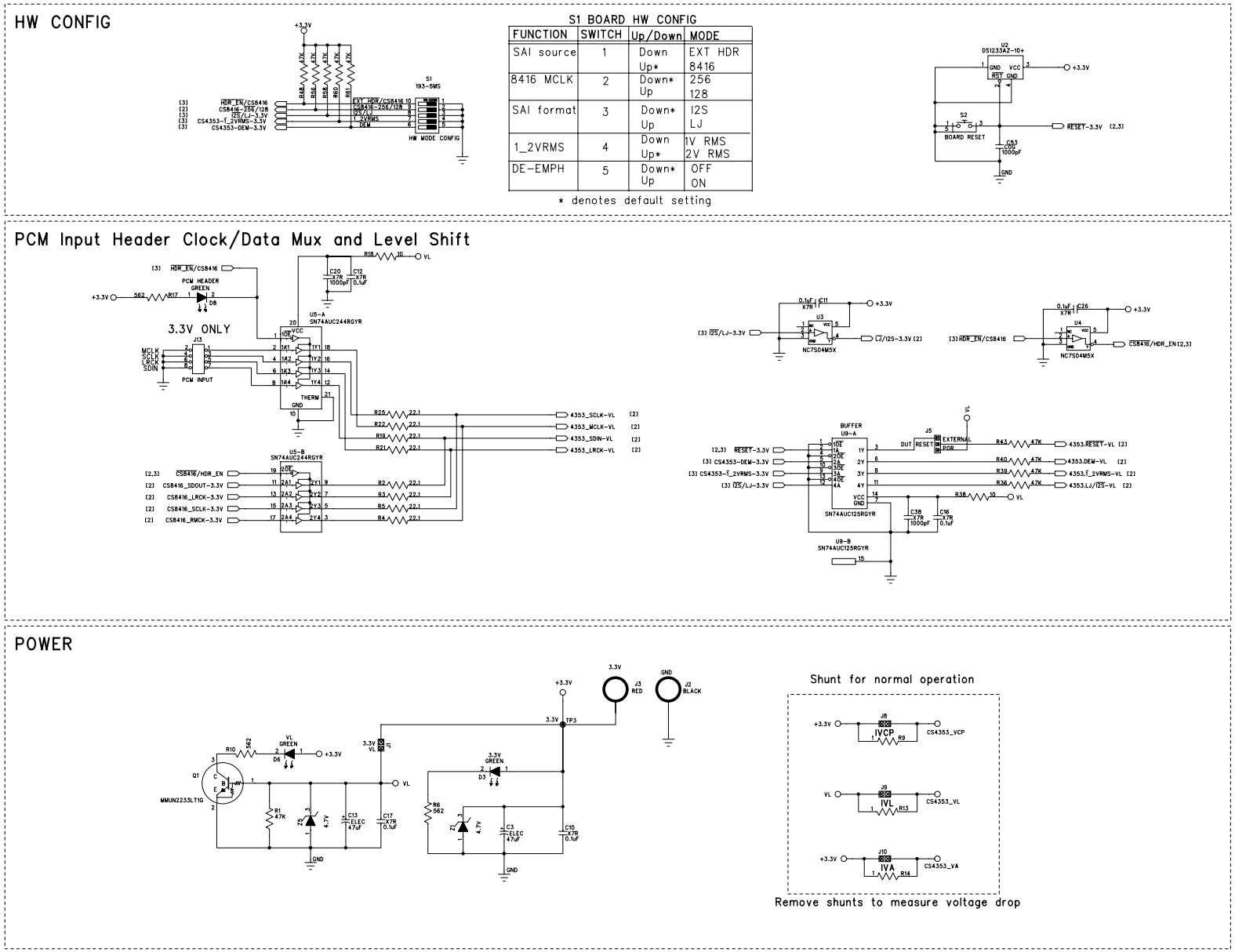

Figure 33. HW Configuration, PCM Header, and Power

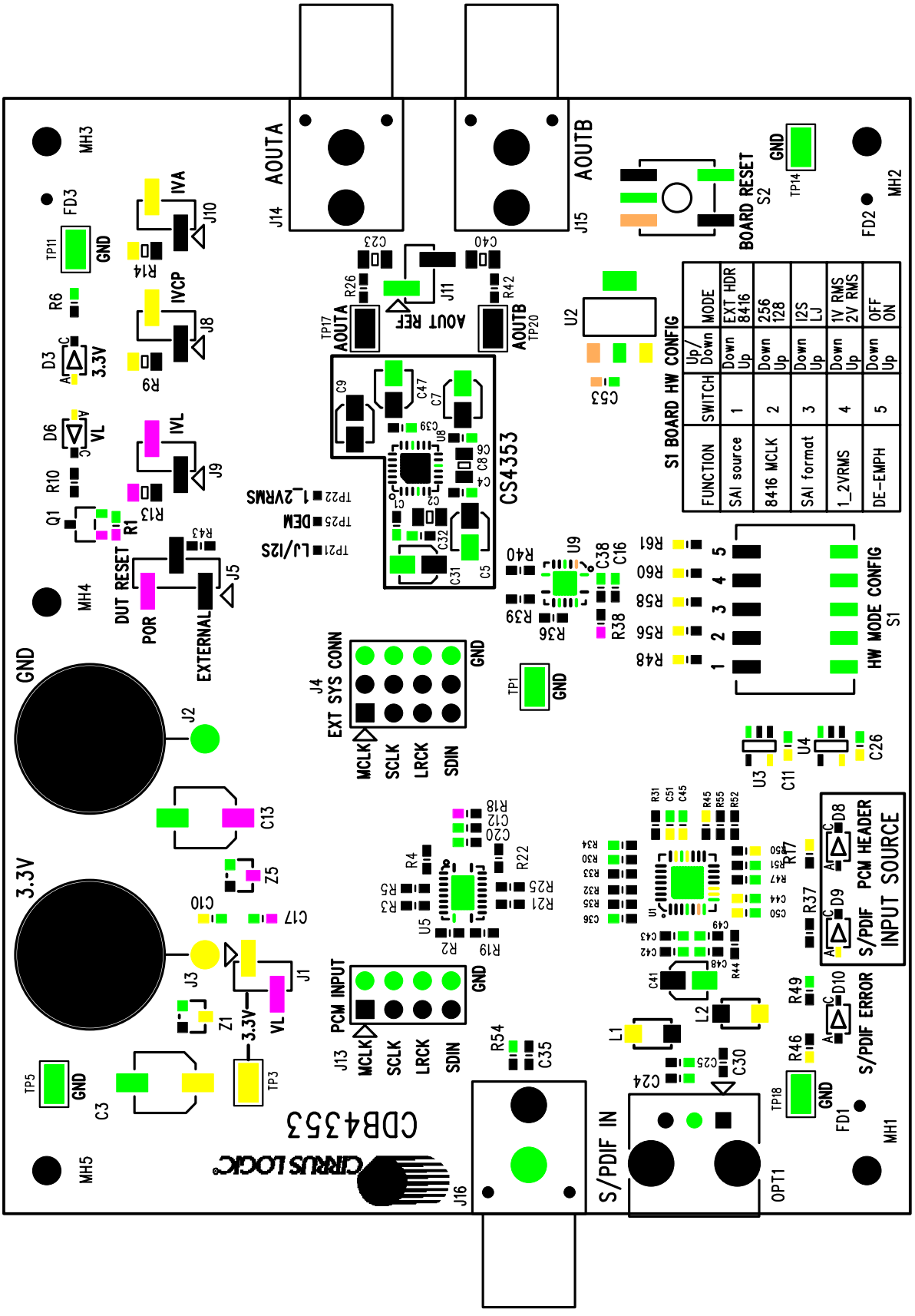

Figure 34. Silkscreen Top

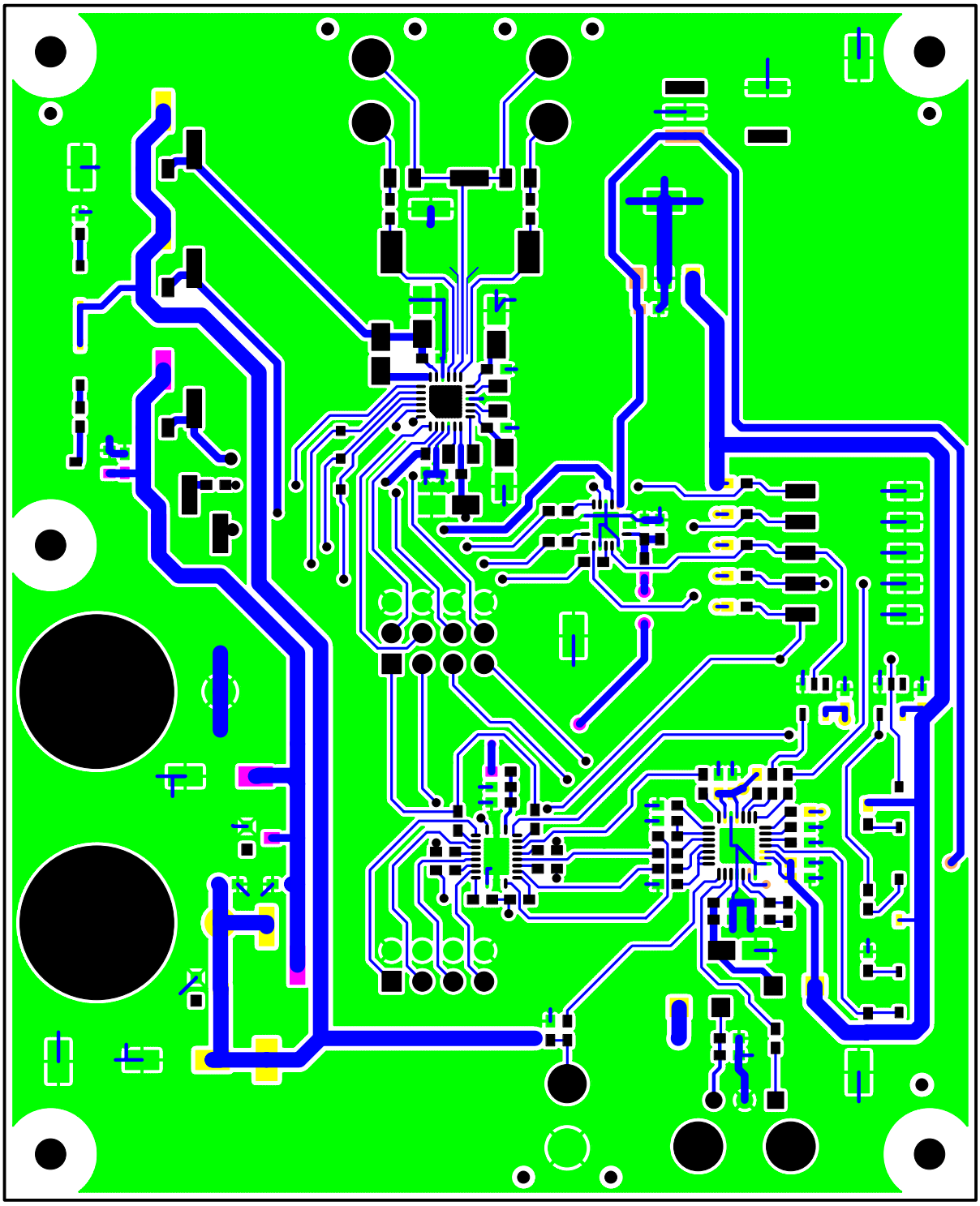

Figure 35. Top Side

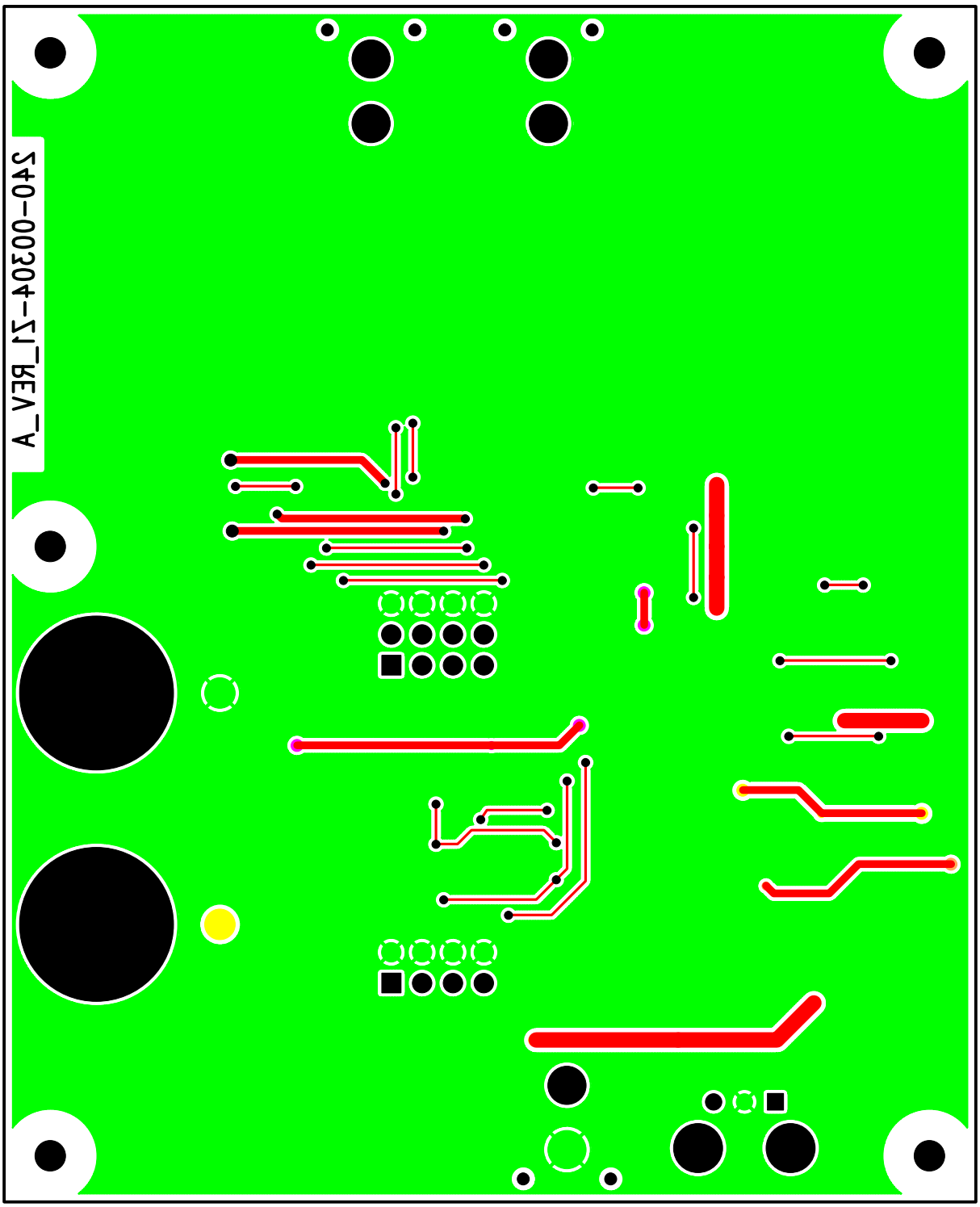

Figure 36. Bottom Side

13.REVISION HISTORY

Release	Changes
DB1	Initial Release
DB2	Updated block diagram on page 1 and Figure 31. Updated features and description on page 1. Updated plots in Section 11. Performance Plots. Updated Figure 32 and Figure 33.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.