



# VSC3340-01

## 6.5 Gbps 40 × 40 Asynchronous Crosspoint Switch

Datasheet

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Vitesse  
Corporate Headquarters  
741 Calle Plano  
Camarillo, California 93012  
United States

[www.vitesse.com](http://www.vitesse.com)

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# Contents

<b>Revision History</b> .....	<b>9</b>
<b>1 Product Overview</b> .....	<b>10</b>
1.1 Features and Benefits .....	11
1.2 Applications.....	12
<b>2 Functional Descriptions</b> .....	<b>13</b>
2.1 Reset.....	13
2.2 Initialization .....	13
2.3 Page-Based Programming.....	13
2.4 Two-Wire Serial Interface (Slave Mode) .....	14
2.4.1 Serial Write.....	14
2.4.2 Serial Read .....	14
2.4.3 Serial Addressing.....	15
2.5 Two-Wire Serial Interface (Master Mode) .....	16
2.6 Four-Wire (SPI) Serial Interface .....	16
2.7 Parallel Programming Interface .....	17
2.8 Crosspoint Connections.....	17
2.8.1 Program a Connection through the Switch Core .....	17
2.8.2 Configure the Selected Input .....	17
2.9 Simultaneous Connections using the Config Pins.....	18
2.10 Protection Mode Switching.....	18
2.11 Input Configuration .....	19
2.11.1 Input Signal Equalization (ISE) .....	19
2.11.2 Standard Input Port Termination .....	19
2.11.3 Input Port Disable.....	20
2.11.4 Input LOS.....	20
2.12 Output Configuration .....	21
2.12.1 Output Pre-Emphasis .....	21
2.12.2 Output Power Level.....	22
2.12.3 Output Signal Suppression.....	22
2.12.4 Out of Band Signal Forwarding .....	23
2.12.5 PCI-Express Receive Detect.....	23
2.13 Core Configuration .....	24
2.13.1 Core Bandwidth.....	24
2.13.2 Core Equalization.....	24
2.14 Status Pins.....	24
2.15 Channel Status .....	24
2.16 Pin Status .....	25
2.17 Global Programming .....	25
2.18 Inject and Sense Ports .....	26
2.19 Green Mode.....	26
<b>3 Registers</b> .....	<b>28</b>
3.1 Individual Register Map.....	28
3.2 Global Register Map.....	28
3.3 Individual Registers .....	30
3.3.1 Connection .....	30
3.3.2 Input ISE 1.....	30
3.3.3 Input ISE 2.....	31
3.3.4 Input Gain.....	31

3.3.5	Input State .....	32
3.3.6	Input LOS .....	33
3.3.7	Output PE 1 .....	33
3.3.8	Output PE 2 .....	34
3.3.9	Output Level .....	34
3.3.10	Output Mode .....	35
3.3.11	Core Control 1 .....	36
3.3.12	Core Control 2 .....	37
3.3.13	Status Pin Configuration .....	37
3.3.14	Unused .....	38
3.3.15	Protection Connect .....	38
3.3.16	Channel Status .....	38
3.4	Global Registers .....	39
3.4.1	Global Connection .....	39
3.4.2	Global Input ISE 1 .....	39
3.4.3	Global Input ISE 2 .....	40
3.4.4	Global Input Gain .....	41
3.4.5	Global Input State .....	41
3.4.6	Global Input LOS .....	42
3.4.7	Global Output PE 1 .....	42
3.4.8	Global Output PE 2 .....	43
3.4.9	Global Output Level .....	43
3.4.10	Global Output Mode .....	44
3.4.11	Global Core Control 1 .....	45
3.4.12	Global Core Control 2 .....	45
3.4.13	Global Status Pin Configuration .....	46
3.4.14	Unused .....	46
3.4.15	Global Protection Connect .....	47
3.4.16	Global Status Pin State .....	47
3.4.17	Test1 .....	48
3.4.18	Test2 .....	48
3.4.19	Test3 .....	49
3.4.20	Test4 .....	49
3.4.21	Test5 .....	50
3.4.22	Test6 .....	51
3.4.23	Core Configuration .....	51
3.4.24	Rx Detect Delay0 .....	52
3.4.25	Rx Detect Delay1 .....	52
3.4.26	Serial Address .....	52
3.4.27	Interface Mode .....	53
3.4.28	Test7 .....	53
3.4.29	Test8 .....	54
3.4.30	Test9 .....	55
3.4.31	Test10 .....	55
3.4.32	RevID .....	56
3.4.33	Current Page .....	56
<b>4</b>	<b>Electrical Specifications .....</b>	<b>57</b>
4.1	DC Characteristics .....	57
4.1.1	High-Speed Data Inputs .....	57
4.1.2	High-Speed Data Outputs .....	58
4.1.3	LVTTTL Inputs and Outputs .....	59
4.1.4	Power Supply Requirements .....	60
4.2	AC Characteristics .....	61
4.2.1	High-Speed Data Inputs .....	61

4.2.2	High-Speed Data Outputs .....	61
4.2.3	Two-Wire Serial Interface.....	62
4.2.4	Parallel Programming Interface.....	63
4.2.5	Four-Wire Serial Interface.....	64
4.3	Operating Conditions .....	65
4.4	Stress Ratings .....	65
<b>5</b>	<b>Pin Descriptions .....</b>	<b>67</b>
5.1	Pin Diagram .....	67
5.2	Pins by Function.....	68
5.2.1	High-Speed Data Inputs .....	68
5.2.2	High-Speed Data Outputs .....	70
5.2.3	Control Pins .....	72
5.2.4	Power Supplies.....	73
5.3	Pins by Number .....	75
5.4	Pins by Name .....	79
<b>6</b>	<b>Package Information.....</b>	<b>83</b>
6.1	Package Drawing.....	83
6.2	Thermal Specifications .....	85
6.3	Moisture Sensitivity .....	85
<b>7</b>	<b>Ordering Information.....</b>	<b>86</b>

## Figures

Figure 1.	Block Diagram .....	11
Figure 2.	LOS Threshold vs. CINPLOS.....	21
Figure 3.	Register Map for Individual Registers .....	28
Figure 4.	Register Map for Global Registers .....	29
Figure 5.	High-Speed Input Buffer Equivalent Circuit .....	58
Figure 6.	High-Speed Output Driver Equivalent Circuit .....	59
Figure 7.	Two-Wire Serial Timing Diagram .....	63
Figure 8.	Parallel Programming Timing Diagram.....	64
Figure 9.	Four-Wire Serial Timing Diagram.....	65
Figure 10.	Pin Diagram .....	67
Figure 11.	Package Drawing .....	84

## Tables

Table 1.	Features and Benefits .....	11
Table 2.	Mapping of Register Address to EEPROM Address .....	16
Table 3.	Connection Map Configuration .....	18
Table 4.	Main-Protection Switching .....	19
Table 5.	Global Programming .....	25
Table 6.	Block Control .....	26
Table 7.	Bandwidth Control .....	27
Table 8.	Connection .....	30
Table 9.	Input ISE 1 .....	30
Table 10.	Input ISE 2 .....	31
Table 11.	Input Gain .....	32
Table 12.	Input State .....	32
Table 13.	Input LOS .....	33
Table 14.	Output PE 1 .....	34
Table 15.	Output PE 2 .....	34
Table 16.	Output Level .....	35
Table 17.	Output Mode .....	35
Table 18.	Core Control 1 .....	36
Table 19.	Core Control 2 .....	37
Table 20.	Status Pin Configuration .....	37
Table 21.	Unused .....	38
Table 22.	Protection Connect .....	38
Table 23.	Channel Status .....	39
Table 24.	Global Connection .....	39
Table 25.	Global Input ISE 1 .....	40
Table 26.	Global Input ISE 2 .....	40
Table 27.	Global Input Gain .....	41
Table 28.	Global Input State .....	42
Table 29.	Global Input LOS .....	42
Table 30.	Global Output PE 1 .....	43
Table 31.	Global Output PE 2 .....	43
Table 32.	Global Output Level .....	44
Table 33.	Global Output Mode .....	44
Table 34.	Global Core Control 1 .....	45
Table 35.	Global Core Control 2 .....	46
Table 36.	Global Status Pin Configuration .....	46
Table 37.	Unused .....	47
Table 38.	Global Protection Connect .....	47
Table 39.	Global Status Pin State .....	47
Table 40.	Test1 .....	48
Table 41.	Test2 .....	48
Table 42.	Test3 .....	49
Table 43.	Test4 .....	50
Table 44.	Test5 .....	50
Table 45.	Test6 .....	51
Table 46.	Core Configuration .....	51
Table 47.	Rx Delay Detect0 .....	52
Table 48.	Rx Delay Detect1 .....	52
Table 49.	Serial Address .....	53
Table 50.	Interface Mode .....	53
Table 51.	Test7 .....	54

Table 52.	Test8.....	54
Table 53.	Test9.....	55
Table 54.	Test10.....	55
Table 55.	RevID.....	56
Table 56.	Current Page.....	56
Table 57.	High-Speed Inputs.....	57
Table 58.	High-Speed Outputs.....	58
Table 59.	LVTTL I/O Specifications.....	59
Table 60.	Power Requirements.....	60
Table 61.	Power Modes.....	60
Table 62.	High-Speed Inputs.....	61
Table 63.	High-Speed Outputs.....	61
Table 64.	Two-Wire Serial Interface Timing Parameters.....	62
Table 65.	Parallel Programming Interface Parameters.....	63
Table 66.	Four-Wire Serial Interface Parameters.....	64
Table 67.	Recommended Operating Conditions.....	65
Table 68.	Stress Ratings.....	65
Table 69.	High-Speed Data Input Pins.....	68
Table 70.	High-Speed Data Output Pins.....	70
Table 71.	Control Pins.....	72
Table 72.	Power Supplies.....	73
Table 73.	Thermal Resistances.....	85
Table 74.	Ordering Information.....	86



## Revision History

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

### Revision 4.0

Revision 4.0 of this datasheet was published in January 2011. This was the first production-level publication of the document.

# 1 Product Overview

The VSC3340-01 device is a cost-effective, power-efficient asynchronous crosspoint switch capable of data rates up to 6.5 Gbps. The VSC3340-01 device has 40 input and 40 output ports. Each port has integrated terminations.

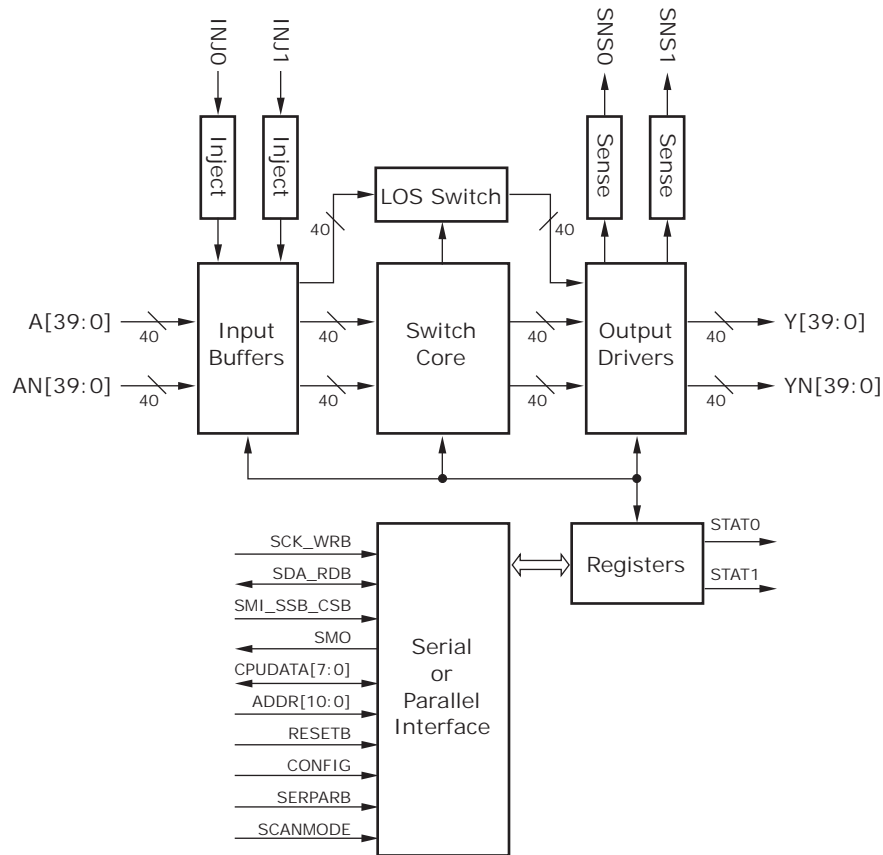
The VSC3340-01 device features programmable input signal equalization and output pre-emphasis (each with multiple settings), which makes it ideal for countering signal degradation over a wide variety of transmission media types and lengths.

Typical power consumption for the device is 110 mW per active channel in 3.2 Gbps (Green mode) and 155 mW per active channel in 6.5 Gbps mode. Unused channels may be deactivated to save the power associated with those ports. Further power savings can be realized by configuring the output level settings to the minimum effective value for a specific application. For more information about Green mode operation, see "[Green Mode](#)," page 26.

The VSC3340-01 device has a loss of signal (LOS) detector on every input port with programmable thresholds. The LOS status can be directed to either of two status pins for external use. The LOS signal is also switched to each of the outputs with the high-speed switching core. Out of band (OOB) signal forwarding can be enabled for each of the outputs, which causes the outputs to be squelched in response to an LOS detect at the corresponding input, thereby propagating an OOB envelope through the switch.

The VSC3340-01 device can be programmed through a two-wire or four-wire serial interface, or a parallel interface with 11-bit address and 8-bit data. The two-wire interface address can be hardwired using the address pins or a proprietary method that allows for address selection after power-up. The four-wire serial interface uses the SSB pin to select the device. All pin functions such as configuration, reset, and status pin states are also accessible using the registers to ensure maximum flexibility.

**Figure 1. Block Diagram**



## 1.1 Features and Benefits

The following table lists the features and benefits of the VSC3340-01 device.

**Table 1. Features and Benefits**

Feature	Benefit
6.5 Gbps operation	Supports all the latest high-speed protocols
Flexible switching options: multicast, loopback, and snoop capability	Allows great flexibility in routing and fanning signals in distributed and centralized architectures
Two-wire serial bus	Simple programming interface
Four-wire serial bus	Faster programming interface
Asynchronous operation	Data agnostic transfers allow each lane to run speed independent without an external reference clock
User-programmable input and output signal equalization	Flexibility in correcting transmission line losses in a variety of media
LOS detection and forwarding	Supports signal monitoring and OOB signal forwarding for SAS, SATA, and PCIe applications

**Table 1. Features and Benefits (continued)**

Feature	Benefit
Optional output signal squelch on a per-channel basis	Supports OOB signal forwarding for SAS, SATA, and PCIe applications

## 1.2 Applications

The following are some of the applications for the VSC3340-01 device:

- Wideband signal switching and clean-up
- Line driver or receiver
- Backplane signal fanout, driver, or receiver
- Copper cable driver or receiver
- PCB signal enhancement
- Broadcast video routers
- Broadcast video switchers
- SAS/SATA signal routing and switching
- PCIe signal routing and switching
- HDMI/DVI switching applications

## 2 Functional Descriptions

This section describes the functions supported by the VSC3340-01 device.

### 2.1 Reset

The VSC3340-01 device can be reset either by pulling the RESETB pin low or by using the internal power-on reset circuit linked to the power supply. The reset state can be released either by energizing the power supply or by releasing the RESETB pin. There are three ways to release the reset state:

- Energize the power supply.
- Externally drive the RESETB pin high.
- Allow the internal pull-up resistor to set the RESETB pin high.

In general, the power-on reset circuit ensures that the VSC3340-01 device powers up correctly. However, the order in which the device is energized is irrelevant if the RESETB pin is held low until the power supply is stable.

The minimum threshold for the power-on reset circuit is approximately 1.6 V for VDD. Therefore, it is important that there is sufficient decoupling on the circuit board to ensure that the supply voltage at the pins of the package does not drop below this value when multiple connection paths on the VSC3340-01 device are energized simultaneously.

### 2.2 Initialization

On reset, the VSC3340-01 device is in low-power state. The only initialization required is to write a value to address 79'h to enable the two-wire or four-wire serial interface if serial interface is desired (SERPARB = 1).

For more information, see ["Two-Wire Serial Interface \(Slave Mode\),"](#) page 14 or ["Four-Wire \(SPI\) Serial Interface,"](#) page 16.

Upon reset, all inputs, outputs, and bias generators are in an off state to reduce the power consumption. Before any connections can be activated, setting the appropriate registers bits energizes these circuits.

Use the global programming registers or the CONFIG pin to transition multiple paths from an off state to an on state simultaneously.

### 2.3 Page-Based Programming

The VSC3340-01 device uses page-based register programming to configure the features and functions of the device. Pages are grouped according to function, and each page typically has a maximum of 40 addresses with a potential address space of 128 8-bit words. The register address within each page corresponds to the number of the input or output that it controls with pages 28'h and 29'h controlling the associated

Inject or Sense buffers. A specific page is selected by programming the value for the desired page into the Current Page register at address 7F'h.

The Current Page register and all other registers that have an address of 50'h or higher are not linked to a specific page; they can be programmed regardless of the value in the Current Page register (address 7F'h). These registers are used to set features and functions of the VSC3340-01 device globally by either setting all 40 registers in an associated page with a single programming step or by setting a configuration that affects the operation of the entire device. For more information about the registers and their functions, see "Registers," page 28.

## 2.4 Two-Wire Serial Interface (Slave Mode)

The VSC3340-01 device supports a slave mode two-wire serial interface where an external master device controls the VSC3340-01 slave device. The two-wire serial interface operates in both standard mode (up to 100 Kbps) and fast mode (up to 400 Kbps) data transfer rates.

A master device generates a start condition <S> by transitioning SDA high to low while SCK is high. Data is then transferred on the SDA line with the most significant bit (MSB) first and the SCK line clocking each bit. Data transitions occur when the SCK is low and is valid (read) or stable (write) when on the high to low transition of the SCK. Data transfers are acknowledged (ACK or <A>) by the receiving device (VSC3340-01 for data writes and the master device for data reads) by holding the SDA signal low while strobing SCK high then low. The master generates a stop condition <P> (terminates the data transfer) with a low to high transition on the SDA signal while SCK is high. For more information, see [Figure 7](#), page 63.

### 2.4.1 Serial Write

A serial write starts with the master sending a byte to the VSC3340-01 device. The first seven bits represent the serial interface address, and the eighth must be a 0 to indicate a write operation. The VSC3340-01 device compares its serial interface address (set by the SADDR[6:0] or the Serial Address register) to the one transmitted. An acknowledge is generated only if they match.

Without issuing a start or stop condition, the master then sends a second byte to the VSC3340-01 device. The VSC3340-01 device interprets this byte as the register address. Finally, the master sends a third byte to the VSC3340-01 device. This is interpreted as the data for the register write. At this point, the write has taken effect.

The following is an example of the write sequence (assuming the serial interface address is set to 00'h):

Write: <S><00'h><A><Address><A><Data><A><P>

### 2.4.2 Serial Read

A read cycle starts with the master sending a byte to the VSC3340-01 device. A stop condition is issued immediately after the desired register address (the second byte) is sent. The master then sends the serial interface address again but this time uses a 1 in the LSB to indicate a read operation. After the acknowledge cycle from the VSC3340-01

device, the master stops driving the SDA line. At this point, the VSC3340-01 device outputs one bit at a time on the falling edge of SCK, transmitting the MSB first until eight bits are transmitted.

After the eighth falling edge of the SCK, the VSC3340-01 device releases control of the SDA bus and the master issues the clock for the acknowledge cycle. After the master issues the acknowledge cycle, the master issues a stop condition to signal the end of the transmission.

The following is an example sequence (assuming the serial interface address is set to 00'h):

Read: <S><00'h><A><Address><A><P>

### 2.4.3 Serial Addressing

The VSC3340-01 device two-wire serial interface supports a 7-bit slave address. This address may be set either of two ways:

- Hardwire the appropriate ADDR[6:0] pins to VDD or GND.
- Use a proprietary interface that requires two additional signal wires (SMI and SMO) and permits the address to be programmed on initialization.

On reset, the address of the VSC3340-01 device is read from the ADDR[6:0] pins. If no address is programmed into the Serial Address register, then the pin voltages define the permanent address for the device. When a value other than all zeros is programmed into the Serial Address register, that new value overrides the value on the ADDR[6:0] pins. The SMI pin must be held high to program the Serial Address register.

The Serial Address register does not latch a programmed value unless the SMI pin is held high concurrent with the programming instruction. Also, the MSB (bit 7) of the Serial Address register controls the state of the SMO pin. By chaining the SMO of one VSC3340-01 device to the SMI pin of the next, it is possible to change the address of up to 64 different devices connected to the same SCK and SDA lines even if they all have identical addresses initially. Writing an address to the first device with the SMI pin held high changes the address of that device, but the remaining devices all have their SMI pins low, so they do not latch the address.

When the address is written to the first device, the state of the SMO can be set high, which sets the SMI pin of the next device high. Now the first device has a different address from the remaining devices, and the SMI pin of the second device is high. The first device does not acknowledge the programming instruction to write to the Serial Address register, and only the second device latches the new address. This process is repeated until all of the devices on the serial bus are defined.

The first programming instruction to the VSC3340-01 device is used to enable the two-wire serial interface. The programming instruction is in the standard format and sets the address 79'h to the value 02'h. (The value 01'h sets the device in four-wire serial mode. The value 11'h is not valid but enables two-wire serial mode by default.)

## 2.5 Two-Wire Serial Interface (Master Mode)

The two-wire serial master mode is activated when the two-wire serial pin is pulled high. In this mode, the VSC3340-01 device drives SCK and uses SDA to communicate with an external serial EEPROM, and reads the contents into its internal register map to provide a loadable user configuration. The global register space of the VSC3340-01 device is not accessed during the master mode to prevent the overwriting of values already placed in the individual channel registers. Eleven-bits of EEPROM address space contain all the data necessary to write to the VSC3340-01 individual register space. The two-wire serial master controller skips over unused register space to speed the load time of the memory space.

The following table shows how the memory layout of the EEPROM maps to the internal register space.

**Table 2. Mapping of Register Address to EEPROM Address**

Page Address (6-bits)	Base Address (6-bits)	EEPROM Address (11-bits)	EEPROM Address Space
00'h	00–29'h	000–029'h	Used
00'h	2A–3F'h	02A–03F'h	Not used
01'h	00–29'h	040–069'h	Used
01'h	2A–3F'h	06A–07F'h	Not used
02'h	00–29'h	080–0A9'h	Used
02'h	2A–3F'h	0AA–0BF'h	Not used
			Used
			Not used
0E'h	00–29'h	380–3A9'h	Used
0E'h	2A–3F'h	3AA–3FF'h	Not used

## 2.6 Four-Wire (SPI) Serial Interface

With the four-wire SPI bus, the SSB signal is the active low serial select signal, which must be low to activate the port. Data is input to the device on the MOSI (SDA) signal (master out, slave in) and sampled on the falling edge of the SCK clock signal. Data is output on the MISO (SMO) signal (master in, slave out) synchronous with the rising edge of SCK. Each four-wire transaction is 3 bytes in length. An 8-bit OPCODE is transferred first, which specifies whether a read (OP = 1) or write (OP = 0) operation is to take place, followed by the 8-bit register address, finally followed by the 8-bit data word. For more information about the four-wire serial interface parameters, refer to ["Four-Wire Serial Interface,"](#) page 64.

In single read/write (R/W) mode, a single 8-bit data word is transferred. After the 8 bits are transferred, the SSB line is brought high, indicating the end of the data transfer. If SSB is brought high before all 8 bits in a given word are transferred, none of the 8 bits in that word are transferred.

The four-wire SPI serial bus is designed for applications where higher data transfer rates are required. The four-wire interface has a maximum data transfer rate of 10 Mbps. Unlike the two-wire serial interface, the chip selection is done through an active low serial select signal (SSB). When SSB is low, the VSC3340-01 device will



respond as a slave device. An external tri-state buffer is required to use the four-wire serial interface in an application where the MISO pins are bused together.

The first programming instruction to the VSC3340-01 device is used to enable the four-wire serial interface. The programming instruction is in the standard format and sets the address 79'h to the value 01'h.

## 2.7 Parallel Programming Interface

The parallel programming mode is activated by setting SERPARB = 0. To write a register using this interface, parallel address and data are presented on the ADDR and CPUDATA[7:0] buses respectively and a rising edge on SCK\_WRB strobes it into the target register. To read, address is presented and SDA\_RDB is driven low to make the CPUDATA[7:0] bus pins into outputs and read out register contents.

Addressing can be in 7-bit paged mode for use with a lower-cost controller, or in combined page/register mode for maximum programming rate. In paged mode, ADDR[10:7] is wired to 0D'h and the page address is drawn from the current page register as with the serial modes, with the current page set to access registers on a given page. For any other value of ADDR[10:7], those bits are interpreted as the page address. In either mode, ADDR[6:0] is the register address within the page.

## 2.8 Crosspoint Connections

A complete connection through the VSC3340-01 device requires that the inputs and outputs are properly energized and configured. This section provides the necessary steps to create a complete connection.

### 2.8.1 Program a Connection through the Switch Core

The connection page is on page 00'h. The first step is to set the current page in the Current Page register (7F'h = 00'h). Next, the value of the desired output port is the value that is used as the address in the connection programming instruction. The data value in the programming instruction is the number of the input port to be connected.

The default state for an output is minimum swing and no pre-emphasis. For more information about configuring the output, see ["Output Configuration,"](#) page 21.

### 2.8.2 Configure the Selected Input

By default, all inputs are turned off to save power on start-up. To turn on the power for a given input, the correct page in the register map must be selected. The Input State register is in page 04'h.

Programming the Current Page register 7F'h to 13'h selects the Input State register page. Bit [1] of the Input State register controls the on and off state of the corresponding input. On reset, this bit is set to 1 to turn off the input. To turn the input on, this bit must be set to 0. The selected input becomes the value for the address on this register page, and the value to be written for a basic connection is 0. For more

information about configuring the input to optimize performance, see [“Input Configuration,”](#) page 19.

## 2.9 Simultaneous Connections using the Config Pins

Use the CONFIG signal to activate multiple connection instructions nearly simultaneously. When the CONFIG pin is held low (value is 0), programming instructions can be written to the connection registers without changing the active connections. When the CONFIG signal is changed to 1, the new connections become active all at once. If the CONFIG signal value is held at 1, programming instructions that are written to the connection registers become active immediately.

The CONFIG\_WP (bit 0) setting of the Core Configuration register inverts the sense of the CONFIG pin. Use this programming interface to assert the CONFIG signal by changing the sense of it regardless of the CONFIG pin state.

When CONFIG\_WP of the Core Configuration register is set to 0, the CONFIG signal operates as previously described. When CONFIG\_WP of the Core Configuration register is set to 1, the operation of the CONFIG pin is inverted so that new connections take effect immediately, as they are programmed. When CONFIG\_WP is set to 1, the programming instructions are queued until the CONFIG pin is set to 0. The following table shows the connection map configurations.

**Table 3. Connection Map Configuration**

PROTECT_MODE Bit	CONFIG_WP Bit	CONFIG Pin	Connection Map Update
0	0	0	No
0	0	1	Yes
0	1	0	Yes
0	1	1	No

For most applications, the crosspoint switch core auto-configures when a connection is made. In some instances, however, it may be desirable to override the default configuration powering down half of the core to reduce power consumption or keeping all switch buffers energized to reduce switching time (at the expense of increased power). For information about setting up the switch core for maximum power efficiency and switching properties, see [“Core Configuration,”](#) page 24.

## 2.10 Protection Mode Switching

Enable Protection Mode to configure the VSC3340-01 device for protection switching. Protection Mode switching is enabled by setting the PROTECT\_MODE bit in the Core Configuration register (address 75'h) of the global register map. The Main connection map is set by the value in the Connection registers (page address 00'h) bits [5:0] and the Protection connection map is set by the value in the Protection Connect register (page address 0E'h) bits [5:0]. For more information, see [“Protection Connect,”](#) page 38 and [“Global Protection Connect,”](#) page 47. In Protection Mode the active connection configuration will switch between main and protection connection maps

when the value of the CONFIG pin or the configuration register bit is changed as shown in the following table.

**Table 4. Main-Protection Switching**

PROTECT_MODE Bit	CONFIG_WP Bit	CONFIG Pin	Active Connection Map
1	0	0	Main
1	0	1	Protection
1	1	0	Protection
1	1	1	Main

## 2.11 Input Configuration

Each input has three sets of registers that are used to configure the various features associated with it. Each of the three sets of registers are on three separate pages of the memory map. Setting the Current Page register (address 7F'h) to 01'h, 02'h, 03'h, 04'h, or 05'h provides access to the five pages named Input ISE 1 (Input Signal Equalization 1), Input ISE 2 (Input Signal Equalization 2), Input Gain, Input State, and Input LOS respectively. There are a total of 40 input ports.

### 2.11.1 Input Signal Equalization (ISE)

The input signal equalization on the VSC3340-01 device helps combat the intersymbol interference (ISI) of high-speed data as it passes through lossy media. This is accomplished by increasing the sensitivity of the receive circuits to the high frequency components of the data edges and works to reverse, in part or in whole, the degradation of signal quality due to propagation through the transmission media.

Discontinuities and losses in the transmission media act as low-pass filters and attenuate the high frequency components of a signal. The cut-off frequency and slope of the filter depend on the specifics of the discontinuities and the losses of the data path. Typically, electrically short discontinuities, such as solder pads and connectors, have a high cutoff frequency. Lossy media, such as transmission lines or backplanes, have a lower cutoff frequency bandwidth. The electrical length of the transmission line or the size of a discontinuity affects the magnitude of the attenuation.

The VSC3340-01 device provides flexibility in correcting for transmission losses by providing two independent ISE stages. Each stage has an adjustable gain and adjustable short, and long time constants associated with it. Each ISE stage can be de-activated or set to a level, depending on the magnitude of the signal filtering that occurred during propagation. The bits that control the ISE settings are in the input ISE registers (pages 01'h, 02'h, 03'h). For more information about these registers, see ["Input ISE 1,"](#) page 30.

### 2.11.2 Standard Input Port Termination

Each input is terminated to a 100  $\Omega$  differential impedance. It is also possible to connect the center of the termination resistor to VDD if necessary to support specific application requirements. The bit that controls this is bit 1 in the Input State register (page 04'h). The reset value of bit 1 for normal differential termination is 1. Setting this

bit to a 1 connects the center of this termination to VDD through  $\sim 20 \Omega$  so that each differential input has a common-mode impedance to VDD through  $70 \Omega$ .

### 2.11.3 Input Port Disable

Each input port must be enabled before it forwards received data to the switching core. The on and off control bit for the inputs is located on page 04'h. Each address on this page refers to the number of the corresponding input. When bit 0 is set to 1, the input port is disabled and the power associated with that port is conserved. When the part is reset, this bit is set to a 1 by default. Therefore, inputs must be enabled before use. For more information about these registers, see "[Input State,](#)" page 32.

### 2.11.4 Input LOS

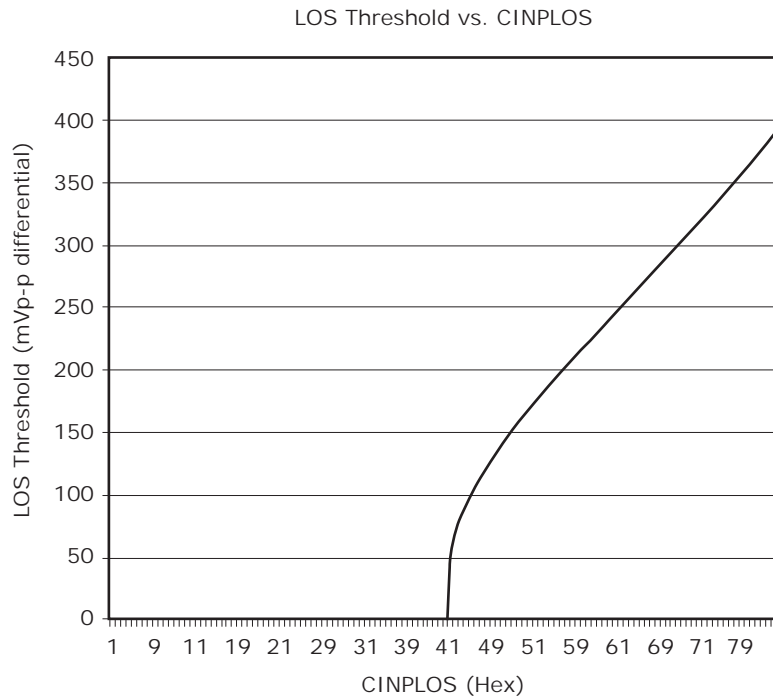
Each input has an LOS (loss of signal) detector associated with it that sets a bit high whenever the signal level drops below a selected value. Although there is a time component to the detection, the primary metric for asserting the LOS signal is the signal amplitude. This amplitude is selectable in the registers on the Input LOS page (05'h). For more information about the amplitude settings, see "[Input LOS,](#)" page 33.

The LOS signal is asserted upon a loss of signal or deasserted when a signal is present for more than 3 ns from when the signal level again exceeds the threshold. This signal can be read from the registers on the CLOS bit of the Channel Status register (0F'h) or it can be connected to either the STAT0 or STAT1 pin using the Global Status Pin Configuration register (5C'h).

This signal is also forwarded to any output connected to the corresponding input and can be used to squelch a transmitted signal when the connected input goes into an LOS state. This is how OOB signaling is propagated.

LOS is available when the CLOSMODE bit, Input LOS register bit 7, is set to 1 and is not available when set to 0, which disables the LOS circuitry to reduce power consumption when LOS function is not required. The following illustration shows the LOS threshold mapped against CINPLOS.

**Figure 2. LOS Threshold vs. CINPLOS**



## 2.12 Output Configuration

Each output has four sets of registers that are used to configure the various features associated with the selected output. Each of the four registers is on a separate page of the memory map. Setting the Current Page register (address 7F'h) to 06'h, 07'h, 08'h, or 09'h provides access to the four pages named Output PE 1, Output PE 2, Output Level, or Output Mode respectively. There are a total of 40 output ports.

### 2.12.1 Output Pre-Emphasis

The output pre-emphasis function of the VSC3340-01 device helps combat the intersymbol interference (ISI) of high-speed data as it passes through lossy media. This is accomplished by shaping the output waveform to boost the magnitude of those frequency components of the transmitted signal that are most susceptible to attenuation as it propagates through the transmission media.

Discontinuities and losses in the transmission media act as low-pass filters and attenuate the high-frequency components of a signal. The cutoff frequency and slope of the filter depend on the specifics of the discontinuities and the losses as the signal propagates through the discontinuities or media. Typically, electrically short discontinuities, such as solder pads and connectors, have a high cutoff frequency. Lossy media, such as transmission lines or backplanes, have a lower cutoff frequency bandwidth. The electrical length of the transmission line or the size of a discontinuity affects the magnitude of the attenuation.

The VSC3340-01 device provides flexibility in correcting for transmission losses with two independent pre-emphasis stages that are additive. Each stage has a different adjustable time constant associated with it.

Each pre-emphasis stage can be deactivated or set to one of 7 levels, depending on the magnitude of the signal filtering that occurred during propagation. Additionally, each of the pre-emphasis stages permits the bandwidth of the boosted signal to be adjusted. Both pre-emphasis stages have eight bandwidth settings.

The bandwidth settings adjust the lower limit of the signal boost and have a single pole roll-off. The uppermost frequency of the signal boost is limited by the slew rate of the output amplifier.

The bits that control the pre-emphasis settings are in the Output PE 1 and Output PE 2 registers (06'h and 07'h). The PE 1 registers control a fast-decay pre-emphasis, and the PE 2 registers control a longer-decay pre-emphasis that is most useful for long cables and extremely long PCB traces. PE 2 is generally used in addition to PE 1, if required. For more information about these settings, see ["Output PE 1,"](#) page 33 and ["Output PE 2,"](#) page 34.

Maintain the following relationship between pre-emphasis settings and output drive to preserve pre-emphasis effectiveness and to avoid exceeding specified maximum device power:

$$\text{CODRV} + \text{CPE1LEVEL} + \text{CPE2LEVEL} < 1111'b$$

Although an operation with a sum that exceeds this will not damage the device, the maximum specified power may be exceeded and the output signal wave shape may be compromised.

## 2.12.2 Output Power Level

The VSC3340-01 device provides a selection of 14 power levels that enable compliance with most popular transmission standards. The output level is selectable using bits [3:0] in the registers on the Output Level page (page 08'h). The register address within the page is used to identify the number of the output that it controls.

For more information about the specific output levels and the values used to select them, see ["Output Level,"](#) page 34.

## 2.12.3 Output Signal Suppression

The VSC3340-01 device can be configured to selectively suppress an output signal to reduce signal noise in a system. When the output signal is suppressed, the true and complement values are driven to the common mode value. This signal level is stable and maintains a DC level that is within  $\pm 50$  mV.

Output signal suppression is controlled by the CDRVCM bit [2] of the register on the Output Mode page 09'h. For more information about the bit values that set the state of the output for normal, power-off, or suppressed operations, see ["Output Mode,"](#) page 35.

## 2.12.4 Out of Band Signal Forwarding

The VSC3340-01 device has the ability to suppress the output signal in response to an LOS assertion at the connected input. For more information, see “[Input LOS](#),” page 20. This feature is compatible with SAS, SATA, and PCIe operation, and its purpose is to propagate out of band (OOB) signaling information through the VSC3340-01 device.

The VSC3340-01 device features an OOB forwarding switch core that duplicates the connections in the high-speed switch core. This core is used to switch the LOS detect signal. With bit 1 of an Output Mode register set to 1, the selected output is suppressed whenever the connected input asserts an LOS condition. This overrides the current output state for as long as the LOS from the input remains asserted. After the LOS condition is removed and the LOS is deasserted, the output assumes whatever state is present on the currently selected input.

It takes approximately 4 ns for the LOS condition to be propagated from the input to the output. For more information, see “[Output Mode](#),” page 35.

## 2.12.5 PCI-Express Receive Detect

To function in a PCIe application, the VSC3340-01 device has two features that can be used with the aid of an external controller:

- The input termination has a switch to produce a low-common-mode impedance at the input, allowing it to appear as an active receiver from the perspective of a PCIe transmitter performing a receive detect operation. For more information, see “[Standard Input Port Termination](#),” page 19.
- The output driver has the capability to generate a receive-detect pulse and compare the rise time of that pulse to a criterion that indicates the presence or absence of an active PCIe receiver at the far end of the line.

To perform a receive detect, bit 7 of the Output Mode register is set to 1. The VSC3340-01 device then automatically performs the following sequence:

1. The output driver is placed in the squelched output mode before measuring the rise time of a common-mode pulse that is generated.
2. A comparator compares the output common-mode voltage to an internal threshold and flips a latch when the common-mode pulse rises past that threshold.
3. The latched comparator output is sampled at pre-defined intervals set by the Rx Detect Delay0 and Rx Detect Delay1 registers, and at the end of the interval count (50 ms approximately, default setting).
4. The results of the two samples are available in the Channel Status register bits [2:1]. A value of 11 indicates a fast rise time (no receiver present) and a value of 10 indicates a slow rise time (receiver present). The 00 and 01 values represent error conditions.

Clear bit 7 of the Output Mode register to reset the state machine after the values have been read.

## 2.13 Core Configuration

Each output is driven by a configurable switch core that has two sets of registers that are used to configure the core. Each of the two registers is on a separate page of the memory map. Setting the Current Page register (address 7F'h) to 0A'h or 0B'h provides access to the two pages named Core Control 1 or Core Control 2 respectively. There are a total of 40 ports, each corresponding to the desired output port. Each core channel is enabled by setting the COREPOFF bit in the Core Control 1 register to 0 for the register address corresponding to the desired output channel.

### 2.13.1 Core Bandwidth

The VSC3340-01 device provides control of the power consumption and bandwidth of the switch core using the CLCOLDRVHP, CSCOLDRVHP, COREOUTH, and CMAINHP control bits in the Core Control 1 and 2 registers. In most cases, for 3 GHz (Green mode) operation, setting CLCOLDRVHP = 10 and the remaining bits to 00 provides the lowest power consumption with sufficient bandwidth. For 6 GHz operation, setting the CMAINHP = 11 and the remaining bits to 10 is sufficient, with slightly higher bandwidth and power consumption when set to 11.

### 2.13.2 Core Equalization

The VSC3340-01 device provides for some amount of internal equalization using the CCOREEQ2 bits in the Core Control 2 register. Some small performance improvement may be realized by increasing the amount of core equalization when operating at the highest supported data rate. However, excessive core equalization can lead to a degraded output signal.

## 2.14 Status Pins

The VSC3340-01 device provides two status pins (STAT0 and STAT1) that permit external monitoring of LOS conditions of one or more selected inputs. LOS signals from one or more of the inputs can be OR'ed together to generate the final signal that appears at a status pin.

There is a separate page for both the STAT0 and STAT1 pins. The registers on the Status Pin State page (5F'h) control both STAT0 and STAT1 pins. Each address on each page refers to the input with the same number.

## 2.15 Channel Status

The VSC3340-01 device has a register associated with each input that reflects its LOS status. These registers are located on the Channel Status page (address 0F'h) and the address of each register corresponds to the number value of the input that it represents. Bit 0 is described as the LOS bit. This is the bit that reflects the current LOS state for the input as identified by the address that is read. For more information about these registers, see "[Channel Status](#)," page 38.



## 2.16 Pin Status

The state of the STAT0 and STAT1 pins can also be monitored using the programming interface. The Pin Status register is located at register address 5F'h. The two LSBs of this register show the current state of the STAT0 and STAT1 pins. Bit 0 reflects the state of STAT0, and bit 1 reflects the state of STAT1.

This provides a convenient and efficient way of polling the VSC3340-01 device for the LOS conditions of multiple inputs by using a single register read when external pin connections are not available or practical. The LOS condition of each input can be assigned to one pin or divided between the STAT0 and STAT1 pins using the registers on the Status 0 and Status 1 pages. When the value is nonzero, more detailed polling of each of the registers on the Channel Status page reveals which input exhibited the LOS condition. If the LOS conditions of the inputs are split between the STAT0 and STAT1 pins, fewer reads are required to locate the input with the LOS condition. For more information about these registers, see "[Channel Status](#)," page 38.

## 2.17 Global Programming

Global programming registers reduce the number of instructions required to initialize the VSC3340-01 device. A global programming register is associated with each page of registers with the exception of the one read-only page (0F'h) that contains the Channel Status and Pin Status registers. A single programming instruction to one of the global programming registers copies the same value to all the registers on the associated page. The global programming registers are assigned to each page as shown in the following table.

**Table 5. Global Programming**

Register Name	Address	Function	Page Affected	Address Range
Global Connection	50'h	Set all connections (all outputs connected to 1 input)	00'h	00'h–27'h
Global Input ISE 1	51'h	Set all input ISE1 values	01'h	00'h–29'h
Global Input ISE 2	52'h	Set all input ISE2 values	02'h	00'h–29'h
Global Input Gain	53'h	Set all input Gain1 and Gain2	03'h	00'h–29'h
Global Input State	54'h	Set all channel input settings	04'h	00'h–29'h
Global Input LOS	55'h	Set all input LOS thresholds	05'h	00'h–29'h
Global Output PE 1	56'h	Set all output PE1 values	06'h	00'h–29'h
Global Output PE 2	57'h	Set all output PE2 values	07'h	00'h–29'h
Global Output Level	58'h	Set all output level values	08'h	00'h–29'h
Global Output Mode	59'h	Set all channel output settings	09'h	00'h–29'h
Global Core Control1	5A'h	Set all core controls	0A'h	00'h–29'h
Global Core Control2	5B'h	Set all core controls	0B'h	00'h–29'h
Global Status Pin Config	5C'h	Set all channels LOS OR'ed on STAT0/STAT1	0C'h	00'h–29'h

Exercise caution when using the global programming registers to change values on connection and input state pages. Because this programs all 40 outputs or inputs

simultaneously, it either turns all of them on, or all of them off, as well. This may cause a connection to be broken.

Turning on all outputs or inputs simultaneously also generates an instantaneous current spike. If there is insufficient decoupling capacitance connected to the package pins, the instantaneous power supply voltage may drop below the minimum level required to trip the device power-on reset that would change the device configuration.

## 2.18 Inject and Sense Ports

The inject and sense ports provide a full-speed input and output port that can be used to provide stimulus to the device without the need to use individual high-speed ports, relays, or external loopbacks on the board.

The Inject paths have the same input buffer as the main data inputs, but drive an internal net that connects each of the regular input buffers. Each input buffer has a switchable mux that can be enabled on a per-input basis to drive the signal from the inject port directly into the signal path of the input buffer, at a fairly low amplitude. The Inject signal mixes with the incoming signal from the input buffer pins, so the user needs to ensure that the channel receiving its signal from the Inject path does not simultaneously have a signal coming in from its pins.

The Sense path has the same output buffer as the main data outputs, but receives a signal from an internal sense net that can be driven from any one of the outputs by an optionally powered buffer embedded in each output driver, which takes a copy the output driver signal and buffers it onto the internal sense net.

The Sense and Inject paths are split into two halves, SNSP0/SNSN0 and INJP0/INJN0 for channels 0 through 19, and SNSP1/SNSN1 and INJP1/INJN1 for channels 20 through 39.

## 2.19 Green Mode

There are several ways to reduce power consumption of the VSC3340-01 device. The easiest is to disable unneeded circuitry using the control registers, as shown in the following table.

**Table 6. Block Control**

Bit Name	Page	Bit Number	Effect
CINPPOWEROFF	04'h	0	Power down input buffer
CODPOWEROFF	09'h	0	Power down output driver
COREPOFF	0A'h	3	Power down core (note that the register address is associated with the output driver it connects to, not the input buffer)

Additionally, bandwidth settings within the VSC3340-01 device allow reduction in power consumption with a corresponding decrease in performance. For lower data rate conditions, reduced performance may be acceptable. The following table summarizes the control bits that control various bandwidths within the VSC3340-01 device and Vitesse recommendations for different data rates. For particularly noisy signals, higher

settings may be required to meet performance requirements. For more information about added jitter specifications for these settings, see [Table 63](#), page 61.

**Table 7. Bandwidth Control**

<b>Bit Name</b>	<b>Page</b>	<b>Bit Number</b>	<b>Effect</b>	<b>3.2 Gbps Green Mode</b>	<b>6.5 Gbps Mode</b>
CINFLOW_PWR	04'h	3:2	Control input buffer bandwidth	00'b	10'b
CODHIGHPOWER	08'h	5:4	Control output driver bandwidth	00'b	10'b
CMAINHP	0A'h	7:6	Switch core main amplifier bandwidth	00'b	11'b
COREOUTH	0A'h	5:4	Switch core output amplifier bandwidth	00'b	10'b
CSCOLDRVHP <sup>(1)</sup>	0B'h	6:5	Switch core short column driver bandwidth	00'b	10'b
CLCOLDRVHP <sup>(1)</sup>	0B'h	4:3	Switch core long column driver bandwidth	10'b	10'b

1. When configured as a fan-out buffer (one receiver to multiple transmitters), if the number of transmitters exceeds two, both the CSCOLDRVHP and CLCOLDRVHP values should be set to at least 10'b.

## 3 Registers

This section provides information about the register maps, register descriptions, and register tables.

### 3.1 Individual Register Map

The individual register map provides a summary of the individual registers in the VSC3340-01 device.

**Figure 3. Register Map for Individual Registers**

Page	Address Range	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
00'h	00'h to 27'h	Connection	Reserved, read only		Main channel connection (0 to 39)						
01'h	00'h to 29'h	Input ISE 1	Reserved, read only		ISE 1, short time constant			ISE 1, long time constant			
02'h	00'h to 29'h	Input ISE 2	Reserved, read only		ISE 2, short time constant			ISE 2, long time constant			
03'h	00'h to 29'h	Input Gain	Reserved, read only		Input amp gain1			Input amp gain2			
04'h	00'h to 29'h	Input State	Offset compensation	Inject buffer control	Reserved	Reserved	Input low bandwidth		Low CM termination	Channel input power	
05'h	00'h to 29'h	Input LOS	LOS sampler		LOS threshold						
06'h	00'h to 29'h	Output PE 1	Reserved, read only		PE 1 level			PE 1 decay time constant			
07'h	00'h to 29'h	Output PE 2	Reserved, read only		PE 2 level			PE 2 decay time constant			
08'h	00'h to 29'h	Output Level	Reserved, read only		Power/Bandwidth level		Output drive level				
09'h	00'h to 29'h	Output Mode	Rx detect enable	Sense on	Reserved	Jam	Forced output value	Drive common mode	OOB enable	Output power off	
0A'h	00'h to 27'h	Core Control1	Main core high power/bandwidth		Core output high power/bandwidth		Core power off	Core main test top	Core main test bottom	Core Tx test	
0B'h	00'h to 27'h	Core Control2	Reserved, read only	Short column drive high power		Long column drive high power		Core EQ			
0C'h	00'h to 29'h	Status Pin Configuration	Reserved, read only						STAT1 pin config	STAT2 pin config	
0D'h	00'h to 29'h	Unused	Reserved, read only								
0E'h	00'h to 27'h	Protection Connect	Reserved, read only		Protection connection						
0F'h	00'h to 29'h	Channel Status	Reserved, read only					Rx detect res1	Rx detect res0	LOS status	

### 3.2 Global Register Map

The global register map provides a summary of the global registers in the VSC3340-01 device.

Figure 4. Register Map for Global Registers

Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
50'h	Global Connection	Reserved, read only		Main channel input connection (0 to 39)					
51'h	Global Input ISE 1	Reserved, read only		ISE 1, short time constant			ISE 1, long time constant		
52'h	Global Input ISE 2	Reserved, read only		ISE 2, short time constant			ISE 2, long time constant		
53'h	Global Input Gain	Reserved, read only		Input amp gain1			Input amp gain2		
54'h	Global Input State	Offset compensation	Inject on	Reserved	Reserved	Input low bandwidth		Low CM termination	Global input power
55'h	Global Input LOS	LOS sampler		LOS threshold					
56'h	Global Output PE 1	Reserved, read only		PE 1 level			PE 1 decay time constant		
57'h	Global Output PE 2	Reserved, read only		PE 2 level			PE 2 decay time constant		
58'h	Global Output Level	Reserved, read only		Power/Bandwidth level		Output drive level			
59'h	Global Output Mode	Reserved, read only		Reserved	Forced output	Forced output value	Drive common mode	OOB forwarding enable	Output power off
5A'h	Global Core Control1	Main core high power/bandwidth		Core output high power/bandwidth		Core power off	Core top test	Core bottom test	Core Tx test
5B'h	Global Core Control2	Reserved	Long column drive high power	Short column drive high power		Core EQ			
5C'h	Global Status Pin Config	Reserved, read only						STAT1 pin config	STAT0 pin config
5D'h	Unused	Reserved, read only							
5E'h	Global Protection Connect	Reserved, read only		Protection input connection (0 to 39)					
5F'h	Global Status Pin State	Reserved, read only						STAT1 pin state	STAT0 pin state
60'h-6C'h	Unused	Reserved, read only							
6D'h	Test1	A7	A6	A5	A4	A3	A2	A1	A0
6E'h	Test2	A15	A14	A13	A12	A11	A10	A9	A8
6F'h	Test3	A23	A22	A21	A20	A19	A18	A17	A16
70'h	Test4	A31	A30	A29	A28	A27	A26	A25	A24
71'h	Test5	A39	A38	A37	A36	A35	A34	A33	A32
72'h	Test6	P DAC test		N DAC test		AMUX select			
75'h	Core Configuration	Enable core bias				Tweak core bias		Protect mode	Connect map config
76'h	Rx Detect Delay0	Delay0 value							
77'h	Rx Detect Delay1	Delay1 value							
78'h	Serial Address	SMO	Serial port address						
79'h	Interface Mode	Reserved, read only			RESET	Unused		Enable 2-wire serial	Enable 4-wire serial
7A'h	Test7	SMI	TWS	CONFIG	INJ1	INJ0	ADDR9	ADDR9	ADDR8
7B'h	Test8	ADDR7	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0
7C'h	Test9	CPU DATA7	CPU DATA6	CPU DATA5	CPU DATA4	CPU DATA3	CPU DATA2	CPU DATA1	CPU DATA0
7D'h	Test10	Reserved, read only		CPU DATA OUT ALL	STAT1 value	STAT0 value	SMO value	CPUDATA input	I/O test mode
7E'h	RevID	Revision code							
7F'h	Current Page	Current page address							

### 3.3 Individual Registers

This section provides information about the individual registers.

#### 3.3.1 Connection

The settings in the Connection register make connections through the switch core. The CCONNCHA\_MAIN bit controls the main connection map.

Register name: Connection

Page address: 00'h

Register address: 00'h–27'h

Register type: R/W

**Table 8. Connection**

Bit	Label	Description	Access	Reset
7:6	Reserved	Reserved	R	
5:0	CCONNCHA_MAIN	Main channel connection 0–39: Input channel to connect to output	R/W	000000

#### 3.3.2 Input ISE 1

The Input ISE 1 register configures the input signal equalization (ISE) stage 1.

Register name: Input ISE 1

Page address: 01'h

Register address: 00'h–29'h

Register type: R/W

**Table 9. Input ISE 1**

Bit	Label	Description	Access	Reset
7:6	Reserved	Reserved	R	00
5:3	CISE1SHORT	ISE 1 short time constant 111: Maximum 110 101 100 011 010 001 000: Minimum	R/W	000

**Table 9. Input ISE 1 (continued)**

Bit	Label	Description	Access	Reset
2:0	CISE1LONG	ISE 1 long time constant 111: Maximum 110 101 100 011 010 001 000: Minimum	R/W	000

### 3.3.3 Input ISE 2

The Input ISE 2 register configures the input signal equalization (ISE) stage 2.

Register name: Input ISE 2

Page address: 02'h

Register address: 00'h–29'h

Register type: R/W

**Table 10. Input ISE 2**

Bit	Label	Description	Access	Reset
7:6	Reserved	Reserved	R	00
5:3	CISE2SHORT	ISE 2 short time constant 111: Maximum 110 101 100 011 010 001 000: Minimum	R/W	000
2:0	CISE2LONG	ISE 2 long time constant 111: Maximum 110 101 100 011 010 001 000: Minimum	R/W	000

### 3.3.4 Input Gain

The Input Gain register defines the main amplifier gain settings for the selected input.

Register name: Input Gain

Page address: 03'h

Register address: 00'h–29'h

Register type: R/W

**Table 11. Input Gain**

Bit	Label	Description	Access	Reset
7:6	Reserved	Reserved	R	00
5:3	CINPGAIN1	Main input amp gain1 111: Maximum 110 101 100 011 010 001 000: Minimum	R/W	111
2:0	CINPGAIN2	Main input amp gain2 111: Maximum 110 101 100 011 010 001 000: Minimum	R/W	111

### 3.3.5 Input State

The Input State register defines the input enable, inject, offset compensation, and termination settings for the selected input.

Register name: Input State

Page address: 04'h

Register address: 00'h–29'h

Register type: R/W

**Table 12. Input State**

Bit	Label	Description	Access	Reset
7	COFFCOMPDIS	Offset compensation 1: Disable offset compensation 0: Enable offset compensation	R/W	1
6	CINJECTON	Inject buffer control 1: Inject buffer on 0: Inject buffer off	R/W	0
5	CVSCOPON	Reserved	R/W	0
4	Reserved	Reserved	R/W	0
3:2	CINPLOW_PWR	Input low bandwidth 11: Maximum (6 Gbps) power/bandwidth operation 00: Minimum (3 Gbps) power/bandwidth operation	R/W	00



**Table 12. Input State (continued)**

Bit	Label	Description	Access	Reset
1	CINPTERMVDD	Low CM termination 1: Low input termination CM resistance to VDD 0: High input termination CM resistance to VDD	R/W	1
0	CINPPOWEROFF	Channel input power 1: Power off this input 0: Power on this input	R/W	1

### 3.3.6 Input LOS

The Input LOS register controls LOS and configures the input LOS threshold value for the selected input.

Register name: Input LOS

Page address: 05'h

Register address: 00'h–29'h

Register type: R/W

**Table 13. Input LOS**

Bit	Label	Description	Access	Reset
7	CLOSMODE	LOS sampler 1: Sampler on 0: Sampler off	R/W	0
6:0	CINPLOS	Channel input LOS threshold 1111111: 133 mV (maximum) --- --- --- 1000100: 26 mV (minimum useful value) 1000000: 0 mV (minimum) 0111111–0000000: Unsupported	R/W	01100000

### 3.3.7 Output PE 1

The Output PE 1 register configures the pre-emphasis amp 1 (PE 1) value and decay time constant for the selected output.

Register name: Output PE 1

Page address: 06'h

Register address: 00'h–29'h

Register type: R/W

**Table 14. Output PE 1**

Bit	Label	Description	Access	Reset
7:6	Reserved	Reserved	R	00
5:3	CPE1LEVEL1	PE 1 level 111: Maximum PE --- 001: Minimum PE 000: PE off	R/W	000
2:0	CPE1DECAY	PE 1 decay time constant 111: Fastest decay --- 000: Slowest decay	R/W	000

### 3.3.8 Output PE 2

The Output PE 2 register configures the pre-emphasis amp 2 (PE 1) value and decay time constant for the selected output.

Register name: Output PE 2

Page address: 07'h

Register address: 00'h–29'h

Register type: R/W

**Table 15. Output PE 2**

Bit	Label	Description	Access	Reset
7:6	Reserved	Reserved	R	00
5:3	CPE2LEVEL1	PE 2 level 111: Maximum PE --- 001: Minimum PE 000: PE off	R/W	000
2:0	CPE2DECAY	PE 2 decay time constant 111: Fastest decay --- 000: Slowest decay	R/W	000

### 3.3.9 Output Level

The Output Level register sets the output power level (peak-to-peak differential voltage) for the selected output.

Register name: Output Level

Page address: 08'h

Register address: 00'h–29'h

Register type: R/W

**Table 16. Output Level**

Bit	Label	Description	Access	Reset
7:6	Reserved	Reserved	R	00
5:4	CODHIGHPOWER	Reduce power/bandwidth 11: Maximum bandwidth/power (100%) 10: 75% power 01: 50% power 00: Minimum bandwidth/power (40%)	R/W	00
3:0	CODRV	Channel output drive level 1111: 1600 mV (maximum drive level) 1110: 1450 mV 1101: 1300 mV 1100: 1130 mV 1011: 1000 mV 1010: 900 mV 1001: 800 mV 1000: 740 mV 0111: 680 mV 0110: 630 mV 0101: 580 mV 0100: 540 mV 0011: 500 mV 0010: 450 mV (minimum drive level) 0001: Vitesse use only (unspecified output swing) 0000: Vitesse use only (unspecified output swing)	R/W	1001

### 3.3.10 Output Mode

The Output Mode register controls out-of-bound (OOB) signalling and output modes for the selected output.

Register name: Output Mode

Page address: 09'h

Register address: 00'h–29'h

Register type: R/W

**Table 17. Output Mode**

Bit	Label	Description	Access	Reset
7	CRXDETEN	Enable RX detect 1: Enable RX detect 0: Disable RX detect	R/W	0
6	CSENSEON	Activate the sense buffer 1: Sense buffer on 0: Sense buffer off	R/W	0
5	CSLEWLIM	Reserved	R/W	0
4	CJAM	Enable forced output 1: Output is forced to jam value 0: Output normal	R/W	0

**Table 17. Output Mode (continued)**

Bit	Label	Description	Access	Reset
3	CJAMVAL	Forced output value 1: Output value is 1 0: Output value is 0	R/W	0
2	CDRVCM	Channel drive common mode 1: Output suppressed (0 differential drive) 0: Output normal	R/W	0
1	COOBEN	Low channel OOB forwarding enable 1: Enable OOB (0 differential when LOS detected) 0: Disable OOB forwarding	R/W	0
0	CODPOWEROFF	Output power off 1: Output driver off 0: Output driver on	R/W	1

### 3.3.11 Core Control 1

The Core Control 1 register controls the switch core configuration and the output termination for the selected output.

Register name: Core Control 1

Page address: 0A'h

Register address: 00'h–27'h

Register type: R/W

**Table 18. Core Control 1**

Bit	Label	Description	Access	Reset
7:6	CMAINHP	Core main high power/bandwidth 11: Maximum 10 01 00: Minimum	R/W	00
5:4	COREOUTH	Core output high power/bandwidth 11: Maximum 10: 01: 00: Minimum	R/W	00
3	COREPOFF	Core power off 0: Core enabled 1: Core disabled	R/W	1
2	COREMAINTSTTOP	Core top testmode 0: Test mode disabled 1: Test mode enabled	R/W	0
1	COREMAINTSTBOT	Core bottom testmode 0: Test mode disabled 1: Test mode enabled	R/W	0
0	CORETXTEST	Core TX MUX testmode 0: Test mode disabled 1: Test mode enabled	R/W	0

### 3.3.12 Core Control 2

The Core Control 2 register configures the switch core signal equaliation and column drive strength.

Register name: Core Control 2

Page address: 0B'h

Register address: 00'h–27'h

Register type: R/W

**Table 19. Core Control 2**

Bit	Label	Description	Access	Reset
7	Reserved	Reserved	R	0
6:5	CSCOLDRVHP	Short column drive high power 11: Maximum 10: 01: 00: Minimum	R/W	00
4:3	CLCOLDRVHP	Long column drive high power 11: Maximum 10: 01: 00: Minimum	R/W	00
2:0	CCOREEQ2	Core EQ 111: Maximum 110: 101: 100: 011: 010: 001: 000: Minimum	R/W	000

### 3.3.13 Status Pin Configuration

The Status Pin Configuration register assigns LOS signals from the selected input to STAT0 and STAT1 pins.

Register name: Status Pin Configuration

Page address: 0C'h

Register address: 00'h–29'h

Register type: R/W

**Table 20. Status Pin Configuration**

Bit	Label	Description	Access	Reset
7:2	Reserved	Reserved	R	000000

**Table 20. Status Pin Configuration (continued)**

Bit	Label	Description	Access	Reset
1	STAT1CFG	STAT1 pin configuration 1: LOS value OR'ed on STAT1 pin 0: No connection	R/W	0
0	STAT0CFG	STAT0 pin configuration 1: LOS value OR'ed on STAT0 pin 0: No connection	R/W	0

### 3.3.14 Unused

This register is for Vitesse use only.

Register name: Local unused

Page address: 0D'h

Register address: 00'h

Register type: R/W

**Table 21. Unused**

Bit	Label	Description	Access	Reset
7:2	Reserved	Reserved	R	0000000

### 3.3.15 Protection Connect

The settings in the Protection Connect register make connections through the switch core. The CCONNCHA\_PROTECT bit controls the protection connection map.

Register name: Connection

Page address: 0E'h

Register address: 00'h–27'h

Register type: R/W

**Table 22. Protection Connect**

Bit	Label	Description	Access	Reset
7:6	Reserved	Reserved	R	00
5:0	CONNCHA_PROTECT	Protection connection 0–39: Input channel to connect to output	R/W	000000

### 3.3.16 Channel Status

The Channel Status register provides the Rx detect results and LOS status for the selected input.

Register name: Channel Status

Page address: 0F'h

Register address: 00'h–29'h

Register type: R

**Table 23. Channel Status**

Bit	Label	Description	Access	Reset
7:3	Reserved	Reserved	R	00000
2	CRXDETRES1	1: Output common-mode did pass threshold after longer delay period 0: Error condition; output common-mode never passed threshold	R	0
1	CRXDETRES0	1: Output common-mode did pass threshold after shorter delay period 0: Output common mode had not passed threshold by earlier sampling time	R	0
0	CLOS	Channel LOS status 1: LOS detected 0: Signal present	R	0

### 3.4 Global Registers

This section provides information about the global registers.

#### 3.4.1 Global Connection

The settings in the Global Connection register make global connections. The GCONNCHA\_MAIN bit controls the main connection map.

Register name: Global Connection

Register address: 50'h

Register type: R/W

**Table 24. Global Connection**

Bit	Label	Description	Access	Reset
7:6	Reserved	Reserved	R	
5:0	GCONNCHA_MAIN	Main channel connection 0–39: Input channel to connect to output	R/W	000000

#### 3.4.2 Global Input ISE 1

The Global Input ISE 1 register configures the input signal equalization (ISE) for all inputs.

Register name: Global Input ISE 1

Register address: 51'h

Register type: R/W

**Table 25. Global Input ISE 1**

Bit	Label	Description	Access	Reset
7:6	Reserved	Reserved	R	00
5:3	GISE1SHORT	Global ISE 1 short time constant 111: Maximum 110 101 100 011 010 001 000: Minimum	R/W	000
2:0	GISE1LONG	Global ISE 1 long time constant 111: Maximum 110 101 100 011 010 001 000: Minimum	R/W	000

### 3.4.3 Global Input ISE 2

The Global Input ISE 2 register configures the ISE 2 for all inputs.

Register name: Global Input ISE 2

Register address: 52'h

Register type: R/W

**Table 26. Global Input ISE 2**

Bit	Label	Description	Access	Reset
7:6	Reserved	Reserved	R	00
5:3	GISE2SHORT	Global ISE 2 short time constant 111: Maximum 110 101 100 011 010 001 000: Minimum	R/W	000



**Table 26. Global Input ISE 2 (continued)**

Bit	Label	Description	Access	Reset
2:0	GISE2LONG	Global ISE 2 long time constant 111: Maximum 110 101 100 011 010 001 000: Minimum	R/W	000

### 3.4.4 Global Input Gain

The Global Input Gain register configures input gain for all inputs.

Register name: Global Input Gain

Register address: 53'h

Register type: R/W

**Table 27. Global Input Gain**

Bit	Label	Description	Access	Reset
7:6	Reserved	Reserved	R	00
5:3	GINPGAIN1	Main input amp gain1 111: Maximum 110 101 100 011 010 001 000: Minimum	R/W	111
2:0	GINPGAIN2	Main input amp gain2 111: Maximum 110 101 100 011 010 001 000: Minimum	R/W	111

### 3.4.5 Global Input State

The Global Input State register defines the input enable, inject, offset compensation, and termination settings for all inputs.

Register name: Global Input State

Register address: 54'h

Register type: R/W

**Table 28. Global Input State**

Bit	Label	Description	Access	Reset
7	GOFFCOMPDIS	Global offset compensation 1: Disable offset compensation 0: Enable offset compensation	R/W	1
6	GINJECTON	Global inject buffer control 1: Inject buffers on 0: Inject buffers off	R/W	0
5	GLOSMODE	Reserved	R/W	0
4	Reserved	Reserved	R/W	0
3:2	GINPLOW_PWR	Global input low bandwidth 11: Maximum (6 Gbps) power/bandwidth operation 00: Minimum (3 Gbps) power/bandwidth operation	R/W	00
1	GINPTERMVDD	Global low CM termination 1: Low input termination CM resistance to VDD 0: High input termination CM resistance to VDD	R/W	1
0	GINPOWEROFF	Global input power 1: Power off all inputs 0: Power on all inputs	R/W	1

### 3.4.6 Global Input LOS

The Global Input LOS register controls the LOS threshold value for all inputs.

Register name: Global Input LOS

Register address: 55'h

Register type: R/W

**Table 29. Global Input LOS**

Bit	Label	Description	Access	Reset
7	GLOSMODE	Global LOS sampler 1: Sampler on 0: Sampler off	R/W	0
6:0	GINPLOS	Global LOS threshold 1111111: 133 mV (maximum) --- --- --- 1000100: 26 mV (minimum useful value) 1000000: 0 mV (minimum) 0111111–0000000: Unsupported	R/W	1100000

### 3.4.7 Global Output PE 1

The Global Output PE 1 register configures the pre-emphasis amp 1 (PE 1) value and decay time constant for all outputs.

Register name: Global Output PE 1

Register address: 56'h

Register type: R/W

**Table 30. Global Output PE 1**

Bit	Label	Description	Access	Reset
7:6	Reserved	Reserved	R	00
5:3	GPE1LEVEL1	Global PE 1 level 111: Maximum PE --- 001: Minimum PE 000: PE off	R/W	000
2:0	GPE1DECAY	Global PE 1 decay time constant 111: Fastest decay --- 000: Slowest decay	R/W	000

### 3.4.8 Global Output PE 2

The Global Output PE 2 register configures the pre-emphasis amp 2 (PE 2) value and decay time constant for all outputs.

Register name: Global Output PE 2

Register address: 57'h

Register type: R/W

**Table 31. Global Output PE 2**

Bit	Label	Description	Access	Reset
7:6	Reserved	Reserved	R	00
5:3	GPE2LEVEL1	Global PE 2 level 111: Maximum PE --- 001: Minimum PE 000: PE OFF	R/W	000
2:0	GPE2DECAY	Global PE 2 decay time constant 111: Slowest decay --- 000: Fastest decay	R/W	000

### 3.4.9 Global Output Level

The Global Output Level register sets the output power level (peak-to-peak differential voltage) for all outputs.

Register name: Global Output Level

Register address: 58'h

Register type: R/W

**Table 32. Global Output Level**

Bit	Label	Description	Access	Reset
7:6	Reserved	Reserved	R	00
5:4	GODHIGHPOWER	Reduce power/bandwidth 11: Maximum bandwidth/power (100%) 10: 75% power 01: 50% power 00: Minimum bandwidth/power (40%)	R/W	00
3:0	GODRV	Global output drive level 1111: 1600 mV (maximum drive level) 1110: 1450 mV 1101: 1300 mV 1100: 1130 mV 1011: 1000 mV 1010: 900 mV 1001: 800 mV 1000: 740 mV 0111: 680 mV 0110: 630 mV 0101: 580 mV 0100: 540 mV 0011: 500 mV 0010: 450 mV (minimum drive level) 0001: Vitesse use only (unspecified output swing) 0000: Vitesse use only (unspecified output swing)	R/W	1001

### 3.4.10 Global Output Mode

The Global Output Mode register controls out-of-bound (OOB) signaling and output modes for all outputs.

Register name: Global Output Mode

Register address: 59'h

Register type: R/W

**Table 33. Global Output Mode**

Bit	Label	Description	Access	Reset
7:6	Reserved	Reserved	R	0
5	GSLEWLIM	Reserved	R/W	0
4	GJAM	Global forced output 1: Output is forced to jam value 0: Output normal	R/W	0
3	GJAMVAL	Global forced output value 1: Output value is 1 0: Output value is 0	R/W	0
2	GDRVCM	Global drive common mode 1: Output suppressed (0 differential drive) 0: Output normal	R/W	0

**Table 33. Global Output Mode (continued)**

Bit	Label	Description	Access	Reset
1	GOOBEN	Global OOB forwarding enable 1: Enable OOB (0 differential when LOS detected) 0: Disable OOB forwarding	R/W	0
0	GODPOWEROFF	Global output power off 1: Output driver off 0: Output driver on	R/W	1

### 3.4.11 Global Core Control 1

The Global Core Control 1 register controls the switch core configuration and the output termination for all outputs.

Register name: Global Core Control 1

Register address: 5A'h

Register type: R/W

**Table 34. Global Core Control 1**

Bit	Label	Description	Access	Reset
7:6	GMAINHP	Core main high power/bandwidth 11: Maximum 10 01 00: Minimum	R/W	00
5:4	GCOREOUTHHP	Core output high power/bandwidth 11: Maximum 10: 01: 00: Minimum	R/W	00
3	GCOREPOFF	Core power off 0: Core enabled 1: Core disabled	R/W	1
2	GCOREMAINTTESTTOP	Core top testmode 0: Test mode disabled 1: Test mode enabled	R/W	0
1	GCOREMAINTTESTBOT	Core bottom testmode 0: Test mode disabled 1: Test mode enabled	R/W	0
0	GCORETXTEST	Core TX MUX testmode 0: Test mode disabled 1: Test mode enabled	R/W	0

### 3.4.12 Global Core Control 2

The Global Core Control 2 register configures the switch core signal equaliation and column drive strength.

Register name: Global Core Control 2

Register address: 5B'h

Register type: R/W

**Table 35. Global Core Control 2**

Bit	Label	Description	Access	Reset
7	Reserved	Reserved	R	0
6:5	GLCOLDRVHP	Long column drive high power 11: Maximum 10: 01: 00: Minimum	R/W	00
4:3	GSCOLDRVHP	Short column drive high power 11: Maximum 10: 01: 00: Minimum	R/W	00
2:0	GCOREEQ2	Core EQ 111: Maximum 110: 101: 100: 011: 010: 001: 000: Minimum	R/W	000

### 3.4.13 Global Status Pin Configuration

The Global Status Pin Configuration register assigns LOS signals from all inputs to STAT0 and STAT1 pins.

Register name: Global Status Pin Configuration

Register address: 5C'h

Register type: R/W

**Table 36. Global Status Pin Configuration**

Bit	Label	Description	Access	Reset
7:2	Reserved	Reserved	R	000000
1	GSTAT1CFG	Global STAT1 pin configuration 1: LOS value OR'ed to STAT1 pin 0: No connection	R/W	0
0	GSTAT0CFG	Global STAT0 pin configuration 1: LOS value OR'ed to STAT0 pin 0: No connection	R/W	0

### 3.4.14 Unused

This register is for Vitesse use only.

Register name: Local unused

Register address: 5D'h

Register type: R/W

**Table 37. Unused**

Bit	Label	Description	Access	Reset
7:0	Reserved	Reserved	R	0000000

### 3.4.15 Global Protection Connect

The settings in the Global Protection Connect register make connections through the switch core. The GCONNCHA\_PROTECT bit controls the protection connection map.

Register name: Global Protection Connect

Register address: 5E'h

Register type: R/W

**Table 38. Global Protection Connect**

Bit	Label	Description	Access	Reset
7:6	Reserved	Reserved	R	00
5:0	GCONNCHA_PROTECT	Protection connection 0–39: Input channel to connect to output	R/W	000000

### 3.4.16 Global Status Pin State

The Global Status Pin State register contains the LOS signals from designated inputs to the STAT0 and STAT1 pins.

Register name: Global Status Pin State

Register address: 5F'h

Register type: R

**Table 39. Global Status Pin State**

Bit	Label	Description	Access	Reset
7:2	Reserved	Reserved	R	000000
1	GSTAT1STATE	Global STAT1 pin state 1: LOS values OR'ed on STAT1 pin 0: No LOS detected	R	0
0	GSTAT0STATE	Global STAT0 pin state 1: LOS values OR'ed on STAT0 pin 0: No LOS detected	R	0

### 3.4.17 Test1

The Test1 register is for Vitesse use only.

Register name: Test1

Register address: 6D'h

Register type: R

**Table 40. Test1**

Bit	Label	Description	Access
7	A7	1: A7 pin high 0: A7 pin low	R
6	A6	1: A6 pin high 0: A6 pin low	R
5	A5	1: A5 pin high 0: A5 pin low	R
4	A4	1: A4 pin high 0: A4 pin low	R
3	A3	1: A3 pin high 0: A3 pin low	R
2	A2	1: A2 pin high 0: A2 pin low	R
1	A1	1: A1 pin high 0: A1 pin low	R
0	A0	1: A0 pin high 0: A0 pin low	R

### 3.4.18 Test2

The Test2 register is for Vitesse use only.

Register name: Test2

Register address: 6E'h

Register type: R

**Table 41. Test2**

Bit	Label	Description	Access
7	A15	1: A15 pin high 0: A15 pin low	R
6	A14	1: A14 pin high 0: A14 pin low	R
5	A13	1: A13 pin high 0: A13 pin low	R
4	A12	1: A12 pin high 0: A12 pin low	R
3	A11	1: A11 pin high 0: A11 pin low	R



**Table 41. Test2 (continued)**

Bit	Label	Description	Access
2	A10	1: A10 pin high 0: A10 pin low	R
1	A9	1: A9 pin high 0: A9 pin low	R
0	A8	1: A8 pin high 0: A8 pin low	R

### 3.4.19 Test3

The Test3 register is for Vitesse use only.

Register name: Test3

Register address: 6F'h

Register type: R

**Table 42. Test3**

Bit	Label	Description	Access
7	A23	1: A23 pin high 0: A23 pin low	R
6	A22	1: A22 pin high 0: A22 pin low	R
5	A21	1: A21 pin high 0: A21 pin low	R
4	A20	1: A20 pin high 0: A20 pin low	R
3	A19	1: A19 pin high 0: A19 pin low	R
2	A18	1: A18 pin high 0: A18 pin low	R
1	A17	1: A17 pin high 0: A17 pin low	R
0	A16	1: A16 pin high 0: A16 pin low	R

### 3.4.20 Test4

The Test4 register is for Vitesse use only.

Register name: Test4

Register address: 70'h

Register type: R

**Table 43. Test4**

Bit	Label	Description	Access
7	A31	1: A31 pin high 0: A31 pin low	R
6	A30	1: A30 pin high 0: A30 pin low	R
5	A29	1: A29 pin high 0: A29 pin low	R
4	A28	1: A28 pin high 0: A28 pin low	R
3	A27	1: A27 pin high 0: A27 pin low	R
2	A26	1: A26 pin high 0: A26 pin low	R
1	A25	1: A25 pin high 0: A25 pin low	R
0	A24	1: A24 pin high 0: A24 pin low	R

### 3.4.21 Test5

The Test5 register is for Vitesse use only.

Register name: Test5

Register address: 71'h

Register type: R

**Table 44. Test5**

Bit	Label	Description	Access
7	A39	1: A39 pin high 0: A39 pin low	R
6	A38	1: A38 pin high 0: A38 pin low	R
5	A37	1: A37 pin high 0: A37 pin low	R
4	A36	1: A36 pin high 0: A36 pin low	R
3	A35	1: A35 pin high 0: A35 pin low	R
2	A34	1: A34 pin high 0: A34 pin low	R
1	A33	1: A33 pin high 0: A33 pin low	R
0	A32	1: A32 pin high 0: A32 pin low	R

### 3.4.22 Test6

The Test6 register is for Vitesse use only (select control for the APAD pin).

Register name: Test6

Register address: 72'h

Register type: R/W

**Table 45. Test6**

Bit	Label	Description	Access	Reset
7:6	DAC_TEST_P_EN	01: Enable P DAC test for input buffers 0–19 and inject buffer 0 10: Enable P DAC test for input buffers 20–39 and inject buffer 1	R/W	00
5:4	DAC_TEST_N_EN	01: Enable N DAC test for input buffers 0–19 and inject buffer 0 10: Enable N DAC test for input buffers 20–39 and inject buffer 1	R/W	00
3:0	AMUXSEL	1001–1111: APAD off (HiZ) 1000: On-chip 123.2 $\Omega$ to ground 0111: On-chip 246.4 $\Omega$ to ground 0110: On-chip 1.8 V regulated voltage 0101: DAC test currents 0100: Left side IPTAT current 0011: Left side bandgap voltage 0010: Right side IPTAT current 0001: Right side bandgap voltage 0000: APAD off (HiZ)	R/W	0000

### 3.4.23 Core Configuration

The Core Configuration register contains the configuration bit and the PROTECT\_MODE bit.

Register name: Core Configuration

Register address: 75'h

Register type: R/W

**Table 46. Core Configuration**

Bit	Label	Description	Access	Reset
7:4	COREBIASENABLE	1111: All biases enabled 0000: All biases disabled	R/W	1111
3:2	COREBIASTWEAK	00: Nominal core biases 01: 25% core bias reduction 10: 25% core bias increase 11: 50% core bias increase	R/W	00
1	PROTECT_MODE	1: Protection mode enabled 0: Normal configuration mode	R/W	0

**Table 46. Core Configuration (continued)**

Bit	Label	Description	Access	Reset
0	CONFIG_WP	1: Configure connect map 0: Configure connect map See "Simultaneous Connections using the Config Pins," page 18		0

### 3.4.24 Rx Detect Delay0

The Rx Detect Delay0 register sets the delay before first sample for PCIe receive detect in units of 250 ns.

Register name: Rx Detect Delay0

Register address: 76'h

Register type: R/W

**Table 47. Rx Delay Detect0**

Bit	Label	Description	Access	Reset
7:0	RXDETDELO	Delay value 0–255: Delay of sample time in units of 250 ns	R/W	1000 (2000 ns)

### 3.4.25 Rx Detect Delay1

The Rx Detect Delay1 register sets the delay before first sample for PCIe receive detect in units of 4000 ns.

Register name: Rx Detect Delay1

Register address: 77'h

Register type: R/W

**Table 48. Rx Delay Detect1**

Bit	Label	Description	Access	Reset
7:0	RXDETDEL1	Delay value 0–255: Delay of sample time in units of 4000 ns	R/W	0101 (20000 ns)

### 3.4.26 Serial Address

The Serial Address register sets the two-wire serial address.

Register name: Serial Address

Register address: 78'h

Register type: R/W

**Table 49. Serial Address**

Bit	Label	Description	Access	Reset
7	SMO	Sets value of SMO pin in two-wire serial mode 1: SMO = 1 0: SMO = 0	R/W	0
6:0	SERADDR	11111111–0000000: Sets the device address for the two-wire serial mode. This setting overrides the value set on the ADDR[6:0] pins. The SMI pin must be high to enable a write to this register.	R/W	0000000

### 3.4.27 Interface Mode

The Interface Mode register sets the serial interface mode to two-wire or four-wire serial mode.

Register name: Interface Mode

Register address: 79'h

Register type: R/W

**Table 50. Interface Mode**

Bit	Label	Description	Access	Reset
7:5		Unused	R	000
4	Soft reset	1: Reset registers (self-clearing) 0: Normal operation	R/W	0
3:2		Unused	R/W	00
1	2WIRE	Two-wire serial enable 1: Selected 0: Not selected	R/W	0
0	4WIRE	Four-wire serial enable 1: Selected 0: Not selected	R/W	0

### 3.4.28 Test7

The Test7 register is for Vitesse use only.

Register name: Test7

Register address: 7A'h

Register type: R

**Table 51. Test7**

Bit	Label	Description	Access
7	SMI	1: SMI pin high 0: SMI pin low	R
6	TWS	1: TWS pin high 0: TWS pin low	R
5	CONFIG	1: CONFIG pin high 0: CONFIG pin low	R
4	INJ1	1: Inject 1 input high 0: Inject 1 input low	R
3	INJ0	1: Inject 0 input high 0: Inject 0 input low	R
2	ADDR9	1: ADDR9 pin high 0: ADDR9 pin low	R
1	ADDR8	1: ADDR8 pin high 0: ADDR8 pin low	R
0	ADDR7	1: ADDR7 pin high 0: ADDR7 pin low	R

### 3.4.29 Test8

The Test8 register is for Vitesse use only.

Register name: Test8

Register address: 7B'h

Register type: R

**Table 52. Test8**

Bit	Label	Description	Access
7	ADDR7	1: ADDR7 pin high 0: ADDR7 pin low	R
6	ADDR6	1: ADDR6 pin high 0: ADDR6 pin low	R
5	ADDR5	1: ADDR5 pin high 0: ADDR5 pin low	R
4	ADDR4	1: ADDR4 pin high 0: ADDR4 pin low	R
3	ADDR3	1: ADDR3 pin high 0: ADDR3 pin low	R
2	ADDR2	1: ADDR2 pin high 0: ADDR2 pin low	R
1	ADDR1	1: ADDR1 pin high 0: ADDR1 pin low	R
0	ADDR0	1: ADDR0 pin high 0: ADDR0 pin low	R

### 3.4.30 Test9

The Test9 register is for Vitesse use only.

Register name: Test9

Register address: 7C'h

Register type: R

**Table 53. Test9**

Bit	Label	Description	Access
7	CPUDATA7	1: CPUDATA7 pin high 0: CPUDATA7 pin low	R
6	CPUDATA6	1: CPUDATA6 pin high 0: CPUDATA6 pin low	R
5	CPUDATA5	1: CPUDATA5 pin high 0: CPUDATA5 pin low	R
4	CPUDATA4	1: CPUDATA4 pin high 0: CPUDATA4 pin low	R
3	CPUDATA3	1: CPUDATA3 pin high 0: CPUDATA3 pin low	R
2	CPUDATA2	1: CPUDATA2 pin high 0: CPUDATA2 pin low	R
1	CPUDATA1	1: CPUDATA1 pin high 0: CPUDATA1 pin low	R
0	CPUDATA0	1: CPUDATA0 pin high 0: CPUDATA0 pin low	R

### 3.4.31 Test10

The Test10 register is for Vitesse use only.

Register name: Test10

Register address: 7D'h

Register type: R/W

**Table 54. Test10**

Bit	Label	Description	Access	Reset
7:6	Reserved	Reserved	R	0
5	CPU DATA OUT ALL	1: CPUDATA[7:0] = 11111111b 0: CPUDATA[7:0] = 00000000b	R/W	0
4	STAT1 OUT	Value set on STAT1 1: Set STAT1 pin high 0: Set STAT1 pin low	R/W	0
3	STAT0 OUT	Value set on STAT0 1: Set STAT0 pin high 0: Set STAT0 pin low	R/W	0

**Table 54. Test10 (continued)**

Bit	Label	Description	Access	Reset
2	SMO OUT	Value to set on SMO 1: Set SMO pin high 0: Set SMO pin low	R/W	0
1	CPUDATA_OEN	1: CPUDATA output mode 0: CPUDATA input mode	R/W	0
0	I/O Test Mode	1: I/O test mode enabled 0: I/O test mode disabled	R/W	0

### 3.4.32 RevID

The RevID register provides the revision code.

Register name: RevID

Register address: 7E'h

Register type: R

**Table 55. RevID**

Bit	Label	Description	Access	Reset
7:0	REVID	10101010: Revision code	R	10101010

### 3.4.33 Current Page

The Current Page register sets the page value for register programming.

Register name: Current Page

Register address: 7F'h

Register type: R/W

**Table 56. Current Page**

Bit	Label	Description	Access	Reset
7:0	CURRPAGE	0000–11111111: Current page setting	R/W	00000000



## 4 Electrical Specifications

This section provides the DC characteristics, AC characteristics, recommended operating conditions, and stress ratings for the VSC3340-01 device.

### 4.1 DC Characteristics

This section contains the DC specifications for the VSC3340-01 device.

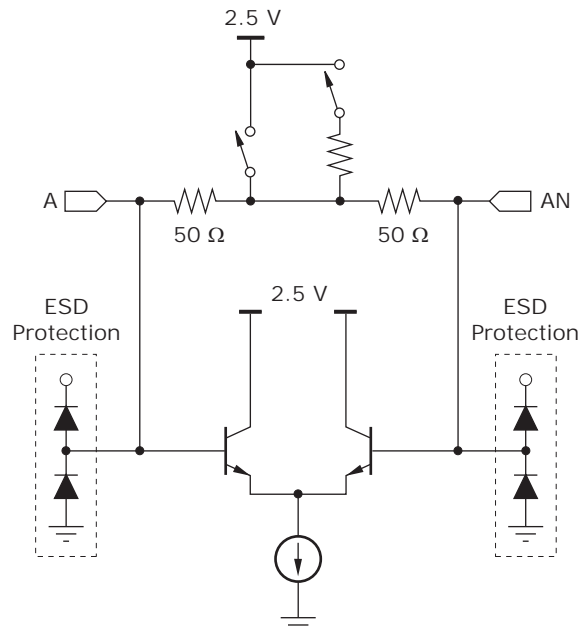
#### 4.1.1 High-Speed Data Inputs

This section provides information about the DC specifications for the high-speed data input pins: A and AN.

**Table 57. High-Speed Inputs**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Input voltage swing, differential drive	$V_{A\_DE}$	100		1800	mVp-p	Differential
Input common-mode voltage	$V_{ICM}$	1.9		$V_{DD}$	V	
Input resistance	$R_{IN}$	80	100	120	$\Omega$	Between true and complement of same input, with nominal setting
Input common-mode resistance	$R_{IN\_CM}$		35		$\Omega$	Input buffer enabled CINPTermVDD = 1
			3000		$\Omega$	Input buffer enabled CINPTermVDD = 0
		>50k			$\Omega$	Input buffer disabled

**Figure 5. High-Speed Input Buffer Equivalent Circuit**



### 4.1.2 High-Speed Data Outputs

This section provides information about the DC specifications for the high-speed data output pins: Y and YN.

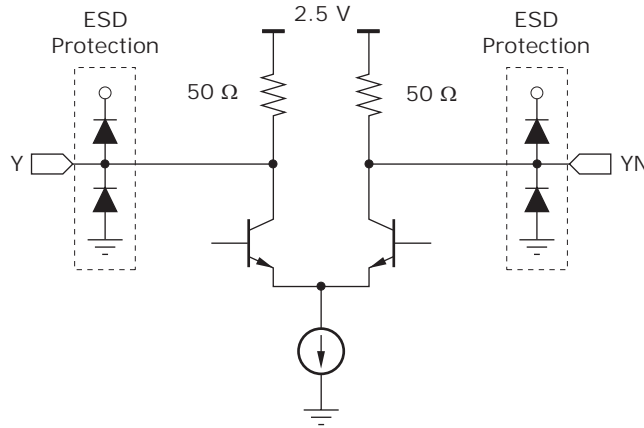
**Table 58. High-Speed Outputs**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Serial data output voltage swing, level 2	$V_{OUT\_2}$	380	450	570	mV	Differential peak-to-peak
Serial data output voltage swing, level 3	$V_{OUT\_3}$	410	500	620	mV	Differential peak-to-peak
Serial data output voltage swing, level 4	$V_{OUT\_4}$	440	540	670	mV	Differential peak-to-peak
Serial data output voltage swing, level 5	$V_{OUT\_5}$	470	580	720	mV	Differential peak-to-peak
Serial data output voltage swing, level 6	$V_{OUT\_6}$	530	630	790	mV	Differential peak-to-peak
Serial data output voltage swing, level 7	$V_{OUT\_7}$	560	680	830	mV	Differential peak-to-peak
Serial data output voltage swing, level 8	$V_{OUT\_8}$	610	740	890	mV	Differential peak-to-peak
Serial data output voltage swing, level 9	$V_{OUT\_9}$	660	800	960	mV	Differential peak-to-peak
Serial data output voltage swing, level 10	$V_{OUT\_10}$	760	900	1080	mV	Differential peak-to-peak

**Table 58. High-Speed Outputs (continued)**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Serial data output voltage swing, level 11	$V_{OUT\_11}$	850	1000	1190	mV	Differential peak-to-peak
Serial data output voltage swing, level 12	$V_{OUT\_12}$	950	1130	1350	mV	Differential peak-to-peak
Serial data output voltage swing, level 13	$V_{OUT\_13}$	1050	1300	1550	mV	Differential peak-to-peak
Serial data output voltage swing, level 14	$V_{OUT\_14}$	1230	1450	1710	mV	Differential peak-to-peak
Serial data output voltage swing, level 15	$V_{OUT\_15}$	1340	1600	1890	mV	Differential peak-to-peak
Back-terminated output resistance	$R_{OUT\_Y}$	40	50	60	$\Omega$	From true or complement to AC ground

**Figure 6. High-Speed Output Driver Equivalent Circuit**



### 4.1.3 LVTTTL Inputs and Outputs

The following table shows the LVTTTL I/O specifications for the VSC3340-01 device.

**Table 59. LVTTTL I/O Specifications**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Input high voltage	$V_{IH}$	1.7	$V_{DD} + 0.7$	V	$V_{DD} = 2.5\text{ V}$
Input low voltage	$V_{IL}$	0	0.6	V	$V_{DD} = 2.5\text{ V}$
Input high current	$I_{IH}$		500	$\mu\text{A}$	
Input low current	$I_{IL}$	-900		$\mu\text{A}$	
Output high voltage	$V_{OH}$	$V_{DD} - 0.4$	$V_{DD}$	V	DC load < 500 $\mu\text{A}$
Output low voltage	$V_{OL}$	0	0.4	V	DC load < 2 mA
Output tri-state leakage (high)	$I_{OZH}$		500	$\mu\text{A}$	

**Table 59. LVTTTL I/O Specifications (continued)**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output tri-state leakage (low)	I <sub>OZL</sub>	-900		μA	

#### 4.1.4 Power Supply Requirements

The following table shows the power dissipation for the VSC3340-01 device assuming all 40 channels are used. For information about the various power modes, see [Table 61](#), page 60.

**Table 60. Power Requirements**

Parameter	Symbol	Typical	Maximum	Unit
Power supply current, maximum	I <sub>DD-MAX</sub>	3.8	4.4	A
Power supply current, 6 Gbps nominal	I <sub>DD-6G-NOM</sub>	2.8	3.3	A
Power supply current, Green mode	I <sub>DD-GREEN</sub>	1.8	2.3	A
Total power dissipation, maximum	P <sub>D-MAX</sub>	9.7	11.5	W
Total power dissipation, 6 Gbps nominal	P <sub>D-6G-NOM</sub>	7.1	8.5	W
Total power dissipation, Green mode	P <sub>D-GREEN</sub>	4.8	5.5	W

The following table provides information about the various power modes.

**Table 61. Power Modes**

Control	Maximum Mode	Nominal 6 Gbps Mode	Green Mode	Register
Channel mapping	Straight through A[39:0] to Y[39:0]	Straight through A[39:0] to Y[39:0]	Straight through A[39:0] to Y[39:0]	Page 00'h Range 00'h to 27'h
Receive ISE	Off	Off	Off	51'h, 52'h
Receive gain	Maximum	Maximum	Maximum	53'h
Receive bandwidth	11b	10b	00b	54'h
Output pre-emphasis	Off	Off	Off	56'h, 57'h
Output power level	1111b	1001b	0101b	58'h
Output high power	11b	10b	00b	58'h
Main core high power	11b	11b	00b	5A'h
Core output high power	11b	10b	00b	5A'h
Short column drive	11b	10b	00b	5B'h
Long column drive	11b	10b	10b	5B'h
VDD	2.625 V	2.5 V	2.5 V	

## 4.2 AC Characteristics

The following tables show the AC specifications for the VSC3340-01 device. The specifications apply for all channels.

### 4.2.1 High-Speed Data Inputs

The following table shows the AC specifications for the high-speed data input pins: A, AN, INJP[1:0], and INJN[1:0].

**Table 62. High-Speed Inputs**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Serial NRZ input data rate	DR <sub>A</sub>	0		6.5	Gbps	Minimum data rate is limited by the AC-coupling capacitor value (if AC-coupled)
Propagation delay from any A input to any Y output			750	1000	ps	
Output channel-to-channel delay skew	t <sub>SKEW</sub>	-150		150	ps	Skew = longest path delay = shortest path delay
Input LOS threshold	V <sub>THLOS</sub>	26		133	mVp-p	Default CINPLOS = 60'h = 81 mVp

### 4.2.2 High-Speed Data Outputs

The following table shows the AC specifications for the high-speed data output pins: Y, YN, SNSP[1:0], and SNSN[1:0].

**Table 63. High-Speed Outputs**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Serial NRZ output data rate	D <sub>RY</sub>	0		6.5	Gbps	Minimum data rate is limited by the AC-coupling capacitor value (if AC-coupled)
Added random jitter	t <sub>RJ_RMS</sub>			0.5	ps <sub>rms</sub>	See note <sup>(1)</sup>
Added random jitter, green mode	t <sub>RJ_RMS,Green</sub>			0.5	ps <sub>rms</sub>	See note <sup>(2)</sup>
Output deterministic jitter <sup>(3)</sup>	t <sub>DJ</sub>			25	ps <sub>p-p</sub>	See note <sup>(4)</sup>
Output deterministic jitter, green mode <sup>(3)</sup>	t <sub>DJ,Green</sub>			40	ps <sub>p-p</sub>	See note <sup>(5)</sup>
Added crosstalk jitter <sup>(3)</sup>	t <sub>XJ_RMS</sub>			1.8	ps <sub>rms</sub>	See note <sup>(6)</sup>

**Table 63. High-Speed Outputs (continued)**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Added crosstalk jitter, green mode <sup>(3)</sup>	$t_{XJ\_RMS,Green}$			2.5	ps <sub>rms</sub>	See note <sup>(7)</sup>
Output duty cycle distortion	$D_{CY}$	40	50	60	%	Applies only to 101010 input data patterns
Output rise time and fall time	$t_{R-Y}, t_{F-Y}$		50	65	ps	20% to 80% with 50 $\Omega$ to AC ground <sup>(8)</sup>
Output rise time and fall time, green mode	$t_{R-Y, Green}, t_{F-Y, Green}$		65	85	ps	20% to 80% with 50 $\Omega$ to AC ground <sup>(9)</sup>
Squelched output amplitude <sup>(10)</sup>	$V_{out-sq}$			30	mV <sub>p-p,DIFF</sub>	Output level = 15

1. Random jitter at the output with a clean input clock pattern measured after subtracting system random jitter values. Measured with default non-green mode and equalization except for ISE1 = 2.
2. Random jitter at the output with a clean input clock pattern measured after subtracting system random jitter values. Measured with default green mode and equalization settings except for ISE1 = 2.
3. Measured by bathtub curve with an Agilent JBERT, with system jitter subtracted linearly from the deterministic jitter and as square-root-difference-of-squares for random jitter.
4. Deterministic jitter at the output with a clean PRBS 2<sup>7</sup>-1 input measured after subtracting system random jitter and channel random jitter values. Measured with default non-green mode and equalization settings except for ISE1 = 2. Measured after 3" of FR-4 PCB trace.
5. Deterministic jitter at the output with a clean PRBS 2<sup>7</sup>-1 input measured after subtracting system random jitter and channel random jitter values. Measured with default green mode and equalization settings except for ISE1 = 2. Measured after 3" of FR-4 PCB trace.
6. Random jitter at the output with a clean PRBS 2<sup>7</sup>-1 input measured in the presence of asynchronous PRBS 2<sup>7</sup>-1 interferers after subtracting system and single channel random jitter values. Measured with default non-green mode and equalization settings except for ISE1 = 2.
7. Random jitter at the output with a clean PRBS 2<sup>7</sup>-1 input measured in the presence of asynchronous PRBS 2<sup>7</sup>-1 interferers after subtracting system and single channel random jitter values. Measured with default green mode and equalization settings except for ISE1 = 2, input buffer bandwidth = 01b, and main switch core bandwidth = 10b.
8. Measured at the output pin for output level = 8 with non-green mode settings except for CPE1LEVEL = 010b and CPE1DECAY = 110b.
9. Measured at the output pin for output level = 8 with green mode settings except for CPE1LEVEL = 010b and CPE1DECAY = 110b.
10. Represents the maximum signal present at the output when the output is active but squelched, either by using the CDRVCM bit or by enabling OOB signal forwarding, while in the presence of asynchronous PRBS 2<sup>7</sup>-1 interferers on adjacent channels.

## 4.2.3 Two-Wire Serial Interface

This section provides information about the two-wire serial interface parameters.

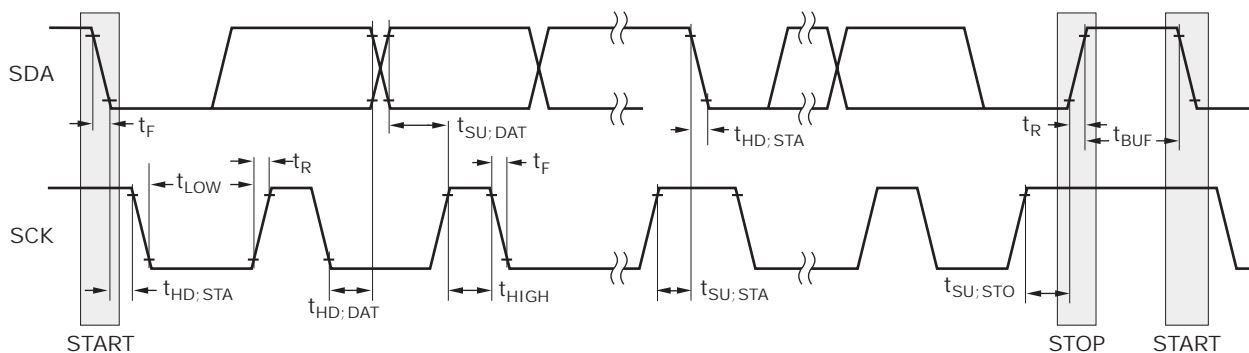
**Table 64. Two-Wire Serial Interface Timing Parameters**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Serial clock	$f_{SCK}$		400	kHz	
Serial I/O	$f_{SDA}$		400	kHz	
Hold time START condition after this period, the first CLK pulse is generated	$t_{HD;STA}$	0.6		$\mu$ s	
Low period of SCK	$t_{LOW}$	1.3		$\mu$ s	
High period of SCK	$t_{HIGH}$	0.6		$\mu$ s	

**Table 64. Two-Wire Serial Interface Timing Parameters (continued)**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Data hold time	$t_{HD;DAT}$	0.09		$\mu\text{s}$	
Data setup time	$t_{SU;DAT}$	100		ns	
Rise time of both SDA and SCK	$t_R$		300	ns	Load $\leq 3\text{nF}$
Fall time of both SDA and SCK	$t_F$		300	ns	Load $\leq 3\text{nF}$
Bus free time between STOP and START	$t_{BUF}$	1.3		$\mu\text{s}$	
Capacitive load for each bus line	$C_B$		400	pF	

**Figure 7. Two-Wire Serial Timing Diagram**



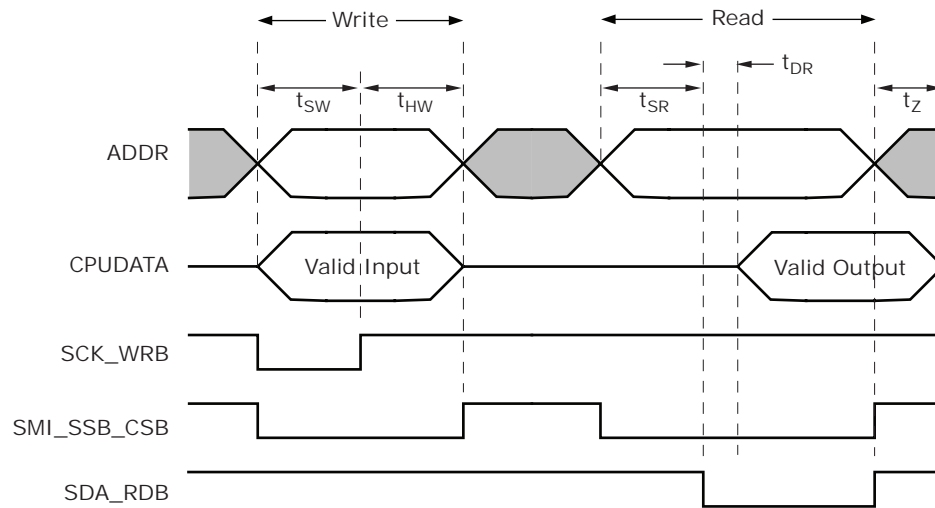
#### 4.2.4 Parallel Programming Interface

This section provides information about the parallel programming interface parameters.

**Table 65. Parallel Programming Interface Parameters**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Delay from SDA_RDB falling to valid output data on CPUDATA	$t_{DR}$		15	ns	
ADDR setup time before falling edge of SDA_RDB for a read	$t_{SR}$	5		ns	
CPUDATA/ADDR hold time after rising edge of SCK_WRB for a write	$t_{HW}$	5		ns	
CPUDATA/ADDR setup time before rising edge of SCK_WRB for a write	$t_{SW}$	5		ns	
Rise, fall time of CPUDATA as output	$t_{RDFD}$		2	ns	Load $\leq 15\text{pF}$
Rise, fall time of SCK_WRB input	$t_{RFSW}$		2	ns	Load $\leq 15\text{pF}$
Time to tri-state CPUDATA after rising edge of SDA_RDB or SMI_SSB_CSB	$t_Z$	0	1	ns	
Capacitive load for each pin	$C_B$		5	pF	

**Figure 8. Parallel Programming Timing Diagram**



#### 4.2.5 Four-Wire Serial Interface

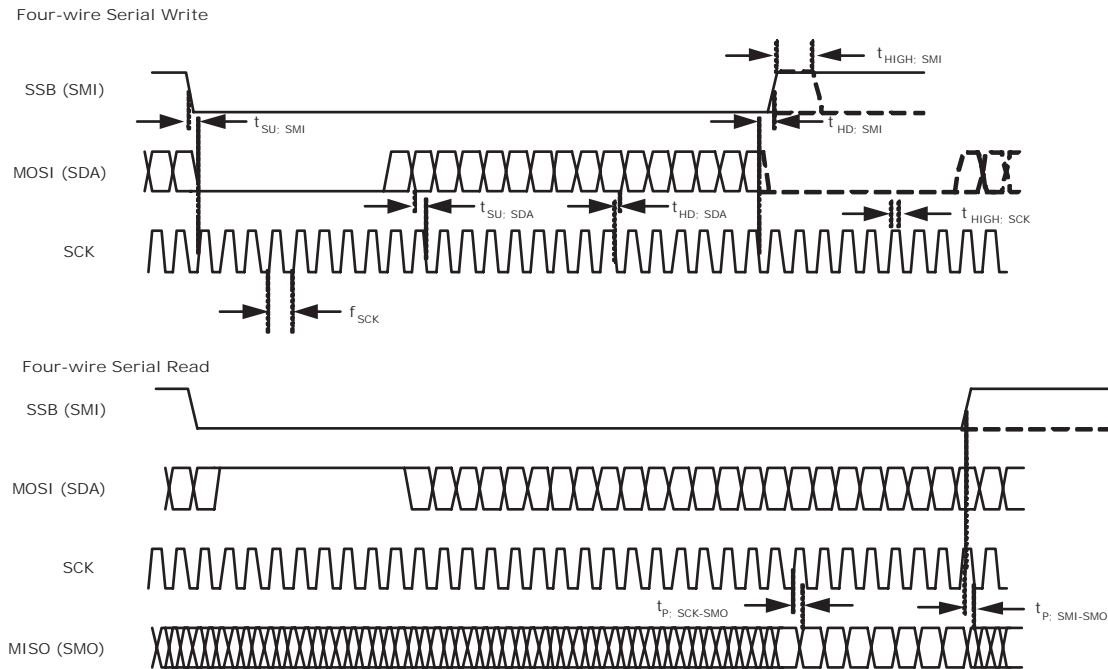
This section provides information about the four-wire serial interface parameters.

**Table 66. Four-Wire Serial Interface Parameters**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Serial clock	$f_{SCK}$		30	MHz	
Serial clock minimum pulse width	$t_{HIGH;SCK}$	5		ns	
SDA setup time to falling edge of SCK	$t_{SU;SDA}$	1		ns	
SDA hold time from falling edge of SCK	$t_{HD;SDA}$	2		ns	
SMI setup time to rising edge of SCK	$t_{SU;SMI}$	2		ns	
Falling SCK in last valid data to rising SMI	$t_{HD;SMI}$	100		ns	
SMI minimum pulse width	$t_{HIGH;SMI}$	5		ns	
Rising edge of SCK to SMO propagation delay	$t_{p;SCK-SMO}$	15		ns	
Rise time for all four-wire signals	$t_R$		3	ns	Clod $\leq$ 15pF
Fall time for all four-wire signals	$t_F$		3	ns	Clod $\leq$ 15pF



**Figure 9. Four-Wire Serial Timing Diagram**



### 4.3 Operating Conditions

The following table shows the recommended operating conditions for the VSC3340-01 device.

**Table 67. Recommended Operating Conditions**

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Core and I/O power supply	$V_{DD}$	2.375	2.5	2.625	V
Operating temperature <sup>(1)</sup>	T	-40		100	°C

1. Minimum specification is ambient temperature, and the maximum is case temperature.

### 4.4 Stress Ratings

This section contains the stress ratings for the VSC3340-01 device.

**Warning** Stresses listed in the following table may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

**Table 68. Stress Ratings**

Parameter	Symbol	Minimum	Maximum	Unit
Power supply voltage, potential to GND	$V_{DD}$	-0.5		V

**Table 68. Stress Ratings (continued)**

Parameter	Symbol	Minimum	Maximum	Unit
DC input voltage applied (TTL)		-0.5	$V_{DD} + 1.0$	V
DC input voltage applied (CML)		-0.5	$V_{DD} + 0.5$	V
Output current (LVTTTL)	$I_{OUT}$	-50	50	mA
Storage temperature	$T_S$	-40	125	°C
Electrostatic discharge voltage, charged device model	$V_{ESD\_CDM}$	-500	500	V
Electrostatic discharge voltage, human body model	$V_{ESD\_HBM}$	See note <sup>(1)</sup>		V

1. This device has completed all required testing as specified in the JEDEC standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*, and complies with a Class 2 rating. The definition of Class 2 is any part that passes an ESD pulse of 2000 V, but fails an ESD pulse of 4000 V.

**Warning** This device can be damaged by electrostatic discharge (ESD) voltage. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

## 5 Pin Descriptions

The VSC3340-01 device has 484 pins, which are described in this section.



The pin information is also provided as an attached Microsoft Excel file, so that you can copy it electronically. In Adobe Reader, double-click the attachment icon.

### 5.1 Pin Diagram

The following illustration shows the top view of the pin diagram for the VSC3340-01 device.

Figure 10. Pin Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
<b>A</b>	Y20	YN20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
<b>B</b>	Y21	YN21	AN19	AN18	AN17	AN16	AN15	AN14	AN13	AN12	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
<b>C</b>	Y22	YN22	ADDR3	ADDR2	ADDR1	ADDR0	VDD	VSS	VSS	VDD	INJPO	INJNO	VSS	VDD	VDD	VSS	CPUD ATA7	CPUD ATA6	CPUD ATA5	CPUD ATA4	YN0	Y0
<b>D</b>	Y23	YN23	ADDR4	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	CPUD ATA3	YN1	Y1
<b>E</b>	Y24	YN24	ADDR5	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	CPUD ATA2	YN2	Y2
<b>F</b>	Y25	YN25	ADDR6	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	CPUD ATA1	YN3	Y3
<b>G</b>	Y26	YN26	APAD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	CPUD ATA0	YN4	Y4
<b>H</b>	Y27	YN27	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	YN5	Y5
<b>J</b>	Y28	YN28	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	YN6	Y6
<b>K</b>	Y29	YN29	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	YN7	Y7
<b>L</b>	Y30	YN30	SNSN1	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	SNSPO	YN8	Y8
<b>M</b>	Y31	YN31	SNSP1	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	SNSNO	YN9	Y9
<b>N</b>	Y32	YN32	VREG	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	YN10	Y10
<b>P</b>	Y33	YN33	VSS	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	YN11	Y11
<b>R</b>	Y34	YN34	VSS	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	YN12	Y12
<b>T</b>	Y35	YN35	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	TWS	YN13	Y13
<b>U</b>	Y36	YN36	ADDR7	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	STAT1	YN14	Y14
<b>V</b>	Y37	YN37	ADDR8	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	STAT0	YN15	Y15
<b>W</b>	Y38	YN38	ADDR9	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD	SERP ARB	YN16	Y16
<b>Y</b>	Y39	YN39	ADDR10	RESETB	CONFIG	SCAN MODE	VSS	VDD	VDD	VSS	INJN1	INJP1	VDD	VSS	VSS	VDD	SCK_ WRB	SDA_ RDB	SMI_SS B_CSB	SMO	YN17	Y17
<b>AA</b>	AN39	AN38	AN37	AN36	AN35	AN34	AN33	AN32	AN31	AN30	AN29	AN28	AN27	AN26	AN25	AN24	AN23	AN22	AN21	AN20	YN18	Y18
<b>AB</b>	A39	A38	A37	A36	A35	A34	A33	A32	A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	YN19	Y19

## 5.2 Pins by Function

This section contains the functional pin descriptions for the VSC3340-01 device.

### 5.2.1 High-Speed Data Inputs

The following table shows the high-speed data input pins for the VSC3340-01 device.

**Table 69. High-Speed Data Input Pins**

Name	Number	I/O	Level	Description
A0	A22	I	CML	Differential input port, true
A1	A21	I	CML	Differential input port, true
A2	A20	I	CML	Differential input port, true
A3	A19	I	CML	Differential input port, true
A4	A18	I	CML	Differential input port, true
A5	A17	I	CML	Differential input port, true
A6	A16	I	CML	Differential input port, true
A7	A15	I	CML	Differential input port, true
A8	A14	I	CML	Differential input port, true
A9	A13	I	CML	Differential input port, true
A10	A12	I	CML	Differential input port, true
A11	A11	I	CML	Differential input port, true
A12	A10	I	CML	Differential input port, true
A13	A9	I	CML	Differential input port, true
A14	A8	I	CML	Differential input port, true
A15	A7	I	CML	Differential input port, true
A16	A6	I	CML	Differential input port, true
A17	A5	I	CML	Differential input port, true
A18	A4	I	CML	Differential input port, true
A19	A3	I	CML	Differential input port, true
A20	AB20	I	CML	Differential input port, true
A21	AB19	I	CML	Differential input port, true
A22	AB18	I	CML	Differential input port, true
A23	AB17	I	CML	Differential input port, true
A24	AB16	I	CML	Differential input port, true
A25	AB15	I	CML	Differential input port, true
A26	AB14	I	CML	Differential input port, true
A27	AB13	I	CML	Differential input port, true
A28	AB12	I	CML	Differential input port, true
A29	AB11	I	CML	Differential input port, true
A30	AB10	I	CML	Differential input port, true
A31	AB9	I	CML	Differential input port, true
A32	AB8	I	CML	Differential input port, true

**Table 69. High-Speed Data Input Pins (continued)**

Name	Number	I/O	Level	Description
A33	AB7	I	CML	Differential input port, true
A34	AB6	I	CML	Differential input port, true
A35	AB5	I	CML	Differential input port, true
A36	AB4	I	CML	Differential input port, true
A37	AB3	I	CML	Differential input port, true
A38	AB2	I	CML	Differential input port, true
A39	AB1	I	CML	Differential input port, true
AN0	B22	I	CML	Differential input port, complement
AN1	B21	I	CML	Differential input port, complement
AN2	B20	I	CML	Differential input port, complement
AN3	B19	I	CML	Differential input port, complement
AN4	B18	I	CML	Differential input port, complement
AN5	B17	I	CML	Differential input port, complement
AN6	B16	I	CML	Differential input port, complement
AN7	B15	I	CML	Differential input port, complement
AN8	B14	I	CML	Differential input port, complement
AN9	B13	I	CML	Differential input port, complement
AN10	B12	I	CML	Differential input port, complement
AN11	B11	I	CML	Differential input port, complement
AN12	B10	I	CML	Differential input port, complement
AN13	B9	I	CML	Differential input port, complement
AN14	B8	I	CML	Differential input port, complement
AN15	B7	I	CML	Differential input port, complement
AN16	B6	I	CML	Differential input port, complement
AN17	B5	I	CML	Differential input port, complement
AN18	B4	I	CML	Differential input port, complement
AN19	B3	I	CML	Differential input port, complement
AN20	AA20	I	CML	Differential input port, complement
AN21	AA19	I	CML	Differential input port, complement
AN22	AA18	I	CML	Differential input port, complement
AN23	AA17	I	CML	Differential input port, complement
AN24	AA16	I	CML	Differential input port, complement
AN25	AA15	I	CML	Differential input port, complement
AN26	AA14	I	CML	Differential input port, complement
AN27	AA13	I	CML	Differential input port, complement
AN28	AA12	I	CML	Differential input port, complement
AN29	AA11	I	CML	Differential input port, complement
AN30	AA10	I	CML	Differential input port, complement
AN31	AA9	I	CML	Differential input port, complement
AN32	AA8	I	CML	Differential input port, complement
AN33	AA7	I	CML	Differential input port, complement

**Table 69. High-Speed Data Input Pins (continued)**

Name	Number	I/O	Level	Description
AN34	AA6	I	CML	Differential input port, complement
AN35	AA5	I	CML	Differential input port, complement
AN36	AA4	I	CML	Differential input port, complement
AN37	AA3	I	CML	Differential input port, complement
AN38	AA2	I	CML	Differential input port, complement
AN39	AA1	I	CML	Differential input port, complement
INJP0	C11	I	CML	Differential test input port, true
INJN0	C12	I	CML	Differential test input port, complement
INJP1	Y12	I	CML	Differential test input port, true
INJN1	Y11	I	CML	Differential test input port, complement

## 5.2.2 High-Speed Data Outputs

The following table shows the high-speed data output pins for the VSC3340-01 device.

**Table 70. High-Speed Data Output Pins**

Name	Number	I/O	Level	Description
Y0	C22	O	CML	Differential output port, true
Y1	D22	O	CML	Differential output port, true
Y2	E22	O	CML	Differential output port, true
Y3	F22	O	CML	Differential output port, true
Y4	G22	O	CML	Differential output port, true
Y5	H22	O	CML	Differential output port, true
Y6	J22	O	CML	Differential output port, true
Y7	K22	O	CML	Differential output port, true
Y8	L22	O	CML	Differential output port, true
Y9	M22	O	CML	Differential output port, true
Y10	N22	O	CML	Differential output port, true
Y11	P22	O	CML	Differential output port, true
Y12	R22	O	CML	Differential output port, true
Y13	T22	O	CML	Differential output port, true
Y14	U22	O	CML	Differential output port, true
Y15	V22	O	CML	Differential output port, true
Y16	W22	O	CML	Differential output port, true
Y17	Y22	O	CML	Differential output port, true
Y18	AA22	O	CML	Differential output port, true
Y19	AB22	O	CML	Differential output port, true
Y20	A1	O	CML	Differential output port, true
Y21	B1	O	CML	Differential output port, true
Y22	C1	O	CML	Differential output port, true
Y23	D1	O	CML	Differential output port, true

**Table 70. High-Speed Data Output Pins (continued)**

Name	Number	I/O	Level	Description
Y24	E1	O	CML	Differential output port, true
Y25	F1	O	CML	Differential output port, true
Y26	G1	O	CML	Differential output port, true
Y27	H1	O	CML	Differential output port, true
Y28	J1	O	CML	Differential output port, true
Y29	K1	O	CML	Differential output port, true
Y30	L1	O	CML	Differential output port, true
Y31	M1	O	CML	Differential output port, true
Y32	N1	O	CML	Differential output port, true
Y33	P1	O	CML	Differential output port, true
Y34	R1	O	CML	Differential output port, true
Y35	T1	O	CML	Differential output port, true
Y36	U1	O	CML	Differential output port, true
Y37	V1	O	CML	Differential output port, true
Y38	W1	O	CML	Differential output port, true
Y39	Y1	O	CML	Differential output port, true
YN0	C21	O	CML	Differential output port, complement
YN1	D21	O	CML	Differential output port, complement
YN2	E21	O	CML	Differential output port, complement
YN3	F21	O	CML	Differential output port, complement
YN4	G21	O	CML	Differential output port, complement
YN5	H21	O	CML	Differential output port, complement
YN6	J21	O	CML	Differential output port, complement
YN7	K21	O	CML	Differential output port, complement
YN8	L21	O	CML	Differential output port, complement
YN9	M21	O	CML	Differential output port, complement
YN10	N21	O	CML	Differential output port, complement
YN11	P21	O	CML	Differential output port, complement
YN12	R21	O	CML	Differential output port, complement
YN13	T21	O	CML	Differential output port, complement
YN14	U21	O	CML	Differential output port, complement
YN15	V21	O	CML	Differential output port, complement
YN16	W21	O	CML	Differential output port, complement
YN17	Y21	O	CML	Differential output port, complement
YN18	AA21	O	CML	Differential output port, complement
YN19	AB21	O	CML	Differential output port, complement
YN20	A2	O	CML	Differential output port, complement
YN21	B2	O	CML	Differential output port, complement
YN22	C2	O	CML	Differential output port, complement
YN23	D2	O	CML	Differential output port, complement
YN24	E2	O	CML	Differential output port, complement

**Table 70. High-Speed Data Output Pins (continued)**

Name	Number	I/O	Level	Description
YN25	F2	O	CML	Differential output port, complement
YN26	G2	O	CML	Differential output port, complement
YN27	H2	O	CML	Differential output port, complement
YN28	J2	O	CML	Differential output port, complement
YN29	K2	O	CML	Differential output port, complement
YN30	L2	O	CML	Differential output port, complement
YN31	M2	O	CML	Differential output port, complement
YN32	N2	O	CML	Differential output port, complement
YN33	P2	O	CML	Differential output port, complement
YN34	R2	O	CML	Differential output port, complement
YN35	T2	O	CML	Differential output port, complement
YN36	U2	O	CML	Differential output port, complement
YN37	V2	O	CML	Differential output port, complement
YN38	W2	O	CML	Differential output port, complement
YN39	Y2	O	CML	Differential output port, complement
SNSP0	L20	O	CML	Differential test output port, true
SNSN0	M20	O	CML	Differential test output port, complement
SNSP1	M3	O	CML	Differential test output port, true
SNSN1	L3	O	CML	Differential test output port, complement

### 5.2.3 Control Pins

The following table shows the control pins for the VSC3340-01 device, including their pull-up (PU) or pull-down (PD) designations.

**Table 71. Control Pins**

Name	Number	I/O	Level	PU/PD	Description
ADDR0	C6	I	LVTTTL	PD	Two-wire serial address, parallel interface address.
ADDR1	C5	I	LVTTTL	PD	Two-wire serial address, parallel interface address.
ADDR2	C4	I	LVTTTL	PD	Two-wire serial address, parallel interface address.
ADDR3	C3	I	LVTTTL	PD	Two-wire serial address, parallel interface address.
ADDR4	D3	I	LVTTTL	PD	Two-wire serial address, parallel interface address.
ADDR5	E3	I	LVTTTL	PU	Two-wire serial address, parallel interface address.
ADDR6	F3	I	LVTTTL	PD	Two-wire serial address, parallel interface address.
ADDR7	U3	I	LVTTTL	PD	Two-wire serial address, parallel interface address.
ADDR8	V3	I	LVTTTL	PD	Two-wire serial address, parallel interface address.
ADDR9	W3	I	LVTTTL	PD	Two-wire serial address, parallel interface address.
ADDR10	Y3	I	LVTTTL	PD	Two-wire serial address, parallel interface address.
CPUDATA0	G20	I/O	LVTTTL	PD	Bidirectional data pin for parallel programming interface.
CPUDATA1	F20	I/O	LVTTTL	PD	Bidirectional data pin for parallel programming interface.
CPUDATA2	E20	I/O	LVTTTL	PD	Bidirectional data pin for parallel programming interface.



**Table 71. Control Pins (continued)**

Name	Number	I/O	Level	PU/PD	Description
CPUDATA3	D20	I/O	LVTTTL	PD	Bidirectional data pin for parallel programming interface.
CPUDATA4	C20	I/O	LVTTTL	PD	Bidirectional data pin for parallel programming interface.
CPUDATA5	C19	I/O	LVTTTL	PD	Bidirectional data pin for parallel programming interface.
CPUDATA6	C18	I/O	LVTTTL	PD	Bidirectional data pin for parallel programming interface.
CPUDATA7	C17	I/O	LVTTTL	PD	Bidirectional data pin for parallel programming interface.
CONFIG	Y5	I	LVTTTL	PD	Permits simultaneous configuration of multiple connection steps. Internal pull-up resistor.
RESETB	Y4	I	LVTTTL	PU	Resets device when pulled low. Internal pull-up resistor.
SCK_WRB	Y17	I/O	LVTTTL	PU	Serial clock for two-wire serial bus. Write strobe for parallel interface.
SDA_RDB	Y18	I/O	LVTTTL	PU	Serial data for two-wire serial bus. Read control for parallel interface.
SMI_SSB_CSB	Y19	I	LVTTTL	PD	Input for optional proprietary two-wire addressing scheme. Chip select for four-wire serial interface and parallel interface.
SMO	Y20	I/O	LVTTTL	PD	Output for optional proprietary two-wire addressing scheme.
STAT0	V20	O	LVTTTL	PD	Status output for LOS.
STAT1	U20	O	LVTTTL	PD	Status output for LOS.
SERPARB	W20	I	LVTTTL	PD	Control for programming interface type. Serial = 1. Parallel = 0.
SCANMODE	Y6	I	LVTTTL	PD	Puts device into scan test mode when 1.
VREG	N3	I	Analog		Internal 1.8 V regulated supply sense point. Vitesse use only.
APAD	G3	O	Analog		Analog test point output. Vitesse use only.
TWS	T20	I	LVTTTL	PD	Two-wire signaling mode when 1.

## 5.2.4 Power Supplies

The following table shows the power supply pins for the VSC3340-01 device.

**Table 72. Power Supplies**

Name	Number	Description
VDD	C7, C10, C14, C15, D4, D5, D8, D9, D12, D13, D16, D17, E4, E5, E8, E9, E12, E13, E16, E17, F6, F7, F10, F11, F14, F15, F18, F19, G6, G7, G10, G11, G14, G15, G18, G19, H4, H5, H8, H9, H12, H13, H16, H17, H20, J4, J5, J8, J9, J12, J13, J16, J17, J20, K3, K6, K7, K10, K11, K14, K15, K18, K19, L6, L7, L10, L11, L14, L15, L18, L19, M4, M5, M8, M9, M12, M13, M16, M17, N4, N5, N8, N9, N12, N13, N16, N17, N20, P6, P7, P10, P11, P14, P15, P18, P19, R6, R7, R10, R11, R14, R15, R18, R19, T4, T5, T8, T9, T12, T13, T16, T17, U4, U5, U8, U9, U12, U13, U16, U17, V6, V7, V10, V11, V14, V15, V18, V19, W6, W7, W10, W11, W14, W15, W18, W19, Y8, Y9, Y13, Y16	Power supply for switch core, high-speed inputs, outputs and control logic (2.5 V)

**Table 72. Power Supplies (continued)**

Name	Number	Description
VSS	C8, C9, C13, C16, D6, D7, D10, D11, D14, D15, D18, D19, E6, E7, E10, E11, E14, E15, E18, E19, F4, F5, F8, F9, F12, F13, F16, F17, G4, G5, G8, G9, G12, G13, G16, G17, H3, H6, H7, H10, H11, H14, H15, H18, H19, J3, J6, J7, J10, J11, J14, J15, J18, J19, K4, K5, K8, K9, K12, K13, K16, K17, K20, L4, L5, L8, L9, L12, L13, L16, L17, M6, M7, M10, M11, M14, M15, M18, M19, N6, N7, N10, N11, N14, N15, N18, N19, P3, P4, P5, P8, P9, P12, P13, P16, P17, P20, R3, R4, R5, R8, R9, R12, R13, R16, R17, R20, T3, T6, T7, T10, T11, T14, T15, T18, T19, U6, U7, U10, U11, U14, U15, U18, U19, V4, V5, V8, V9, V12, V13, V16, V17, W4, W5, W8, W9, W12, W13, W16, W17, Y7, Y10, Y14, Y15	Ground

## 5.3 Pins by Number

This section provides a numeric list of the VSC3340-01 device pins.

A1	Y20	AA22	Y18	B21	AN1
A2	YN20	AB1	A39	B22	AN0
A3	A19	AB2	A38	C1	Y22
A4	A18	AB3	A37	C2	YN22
A5	A17	AB4	A36	C3	ADDR3
A6	A16	AB5	A35	C4	ADDR2
A7	A15	AB6	A34	C5	ADDR1
A8	A14	AB7	A33	C6	ADDR0
A9	A13	AB8	A32	C7	VDD
A10	A12	AB9	A31	C8	VSS
A11	A11	AB10	A30	C9	VSS
A12	A10	AB11	A29	C10	VDD
A13	A9	AB12	A28	C11	INJP0
A14	A8	AB13	A27	C12	INJN0
A15	A7	AB14	A26	C13	VSS
A16	A6	AB15	A25	C14	VDD
A17	A5	AB16	A24	C15	VDD
A18	A4	AB17	A23	C16	VSS
A19	A3	AB18	A22	C17	CPUDATA7
A20	A2	AB19	A21	C18	CPUDATA6
A21	A1	AB20	A20	C19	CPUDATA5
A22	A0	AB21	YN19	C20	CPUDATA4
AA1	AN39	AB22	Y19	C21	YN0
AA2	AN38	B1	Y21	C22	Y0
AA3	AN37	B2	YN21	D1	Y23
AA4	AN36	B3	AN19	D2	YN23
AA5	AN35	B4	AN18	D3	ADDR4
AA6	AN34	B5	AN17	D4	VDD
AA7	AN33	B6	AN16	D5	VDD
AA8	AN32	B7	AN15	D6	VSS
AA9	AN31	B8	AN14	D7	VSS
AA10	AN30	B9	AN13	D8	VDD
AA11	AN29	B10	AN12	D9	VDD
AA12	AN28	B11	AN11	D10	VSS
AA13	AN27	B12	AN10	D11	VSS
AA14	AN26	B13	AN9	D12	VDD
AA15	AN25	B14	AN8	D13	VDD
AA16	AN24	B15	AN7	D14	VSS
AA17	AN23	B16	AN6	D15	VSS
AA18	AN22	B17	AN5	D16	VDD
AA19	AN21	B18	AN4	D17	VDD
AA20	AN20	B19	AN3	D18	VSS
AA21	YN18	B20	AN2	D19	VSS

Pins by number *(continued)*

D20	CPUDATA3	F21	YN3	H22	Y5
D21	YN1	F22	Y3	J1	Y28
D22	Y1	G1	Y26	J2	YN28
E1	Y24	G2	YN26	J3	VSS
E2	YN24	G3	APAD	J4	VDD
E3	ADDR5	G4	VSS	J5	VDD
E4	VDD	G5	VSS	J6	VSS
E5	VDD	G6	VDD	J7	VSS
E6	VSS	G7	VDD	J8	VDD
E7	VSS	G8	VSS	J9	VDD
E8	VDD	G9	VSS	J10	VSS
E9	VDD	G10	VDD	J11	VSS
E10	VSS	G11	VDD	J12	VDD
E11	VSS	G12	VSS	J13	VDD
E12	VDD	G13	VSS	J14	VSS
E13	VDD	G14	VDD	J15	VSS
E14	VSS	G15	VDD	J16	VDD
E15	VSS	G16	VSS	J17	VDD
E16	VDD	G17	VSS	J18	VSS
E17	VDD	G18	VDD	J19	VSS
E18	VSS	G19	VDD	J20	VDD
E19	VSS	G20	CPUDATA0	J21	YN6
E20	CPUDATA2	G21	YN4	J22	Y6
E21	YN2	G22	Y4	K1	Y29
E22	Y2	H1	Y27	K2	YN29
F1	Y25	H2	YN27	K3	VDD
F2	YN25	H3	VSS	K4	VSS
F3	ADDR6	H4	VDD	K5	VSS
F4	VSS	H5	VDD	K6	VDD
F5	VSS	H6	VSS	K7	VDD
F6	VDD	H7	VSS	K8	VSS
F7	VDD	H8	VDD	K9	VSS
F8	VSS	H9	VDD	K10	VDD
F9	VSS	H10	VSS	K11	VDD
F10	VDD	H11	VSS	K12	VSS
F11	VDD	H12	VDD	K13	VSS
F12	VSS	H13	VDD	K14	VDD
F13	VSS	H14	VSS	K15	VDD
F14	VDD	H15	VSS	K16	VSS
F15	VDD	H16	VDD	K17	VSS
F16	VSS	H17	VDD	K18	VDD
F17	VSS	H18	VSS	K19	VDD
F18	VDD	H19	VSS	K20	VSS
F19	VDD	H20	VDD	K21	YN7
F20	CPUDATA1	H21	YN5	K22	Y7

Pins by number *(continued)*

L1	Y30	N2	YN32	R3	VSS
L2	YN30	N3	VREG	R4	VSS
L3	SNSN1	N4	VDD	R5	VSS
L4	VSS	N5	VDD	R6	VDD
L5	VSS	N6	VSS	R7	VDD
L6	VDD	N7	VSS	R8	VSS
L7	VDD	N8	VDD	R9	VSS
L8	VSS	N9	VDD	R10	VDD
L9	VSS	N10	VSS	R11	VDD
L10	VDD	N11	VSS	R12	VSS
L11	VDD	N12	VDD	R13	VSS
L12	VSS	N13	VDD	R14	VDD
L13	VSS	N14	VSS	R15	VDD
L14	VDD	N15	VSS	R16	VSS
L15	VDD	N16	VDD	R17	VSS
L16	VSS	N17	VDD	R18	VDD
L17	VSS	N18	VSS	R19	VDD
L18	VDD	N19	VSS	R20	VSS
L19	VDD	N20	VDD	R21	YN12
L20	SNSP0	N21	YN10	R22	Y12
L21	YN8	N22	Y10	T1	Y35
L22	Y8	P1	Y33	T2	YN35
M1	Y31	P2	YN33	T3	VSS
M2	YN31	P3	VSS	T4	VDD
M3	SNSP1	P4	VSS	T5	VDD
M4	VDD	P5	VSS	T6	VSS
M5	VDD	P6	VDD	T7	VSS
M6	VSS	P7	VDD	T8	VDD
M7	VSS	P8	VSS	T9	VDD
M8	VDD	P9	VSS	T10	VSS
M9	VDD	P10	VDD	T11	VSS
M10	VSS	P11	VDD	T12	VDD
M11	VSS	P12	VSS	T13	VDD
M12	VDD	P13	VSS	T14	VSS
M13	VDD	P14	VDD	T15	VSS
M14	VSS	P15	VDD	T16	VDD
M15	VSS	P16	VSS	T17	VDD
M16	VDD	P17	VSS	T18	VSS
M17	VDD	P18	VDD	T19	VSS
M18	VSS	P19	VDD	T20	TWS
M19	VSS	P20	VSS	T21	YN13
M20	SNSN0	P21	YN11	T22	Y13
M21	YN9	P22	Y11	U1	Y36
M22	Y9	R1	Y34	U2	YN36
N1	Y32	R2	YN34	U3	ADDR7

Pins by number *(continued)*

U4	VDD	W5	VSS
U5	VDD	W6	VDD
U6	VSS	W7	VDD
U7	VSS	W8	VSS
U8	VDD	W9	VSS
U9	VDD	W10	VDD
U10	VSS	W11	VDD
U11	VSS	W12	VSS
U12	VDD	W13	VSS
U13	VDD	W14	VDD
U14	VSS	W15	VDD
U15	VSS	W16	VSS
U16	VDD	W17	VSS
U17	VDD	W18	VDD
U18	VSS	W19	VDD
U19	VSS	W20	SERPARB
U20	STAT1	W21	YN16
U21	YN14	W22	Y16
U22	Y14	Y1	Y39
V1	Y37	Y2	YN39
V2	YN37	Y3	ADDR10
V3	ADDR8	Y4	RESETB
V4	VSS	Y5	CONFIG
V5	VSS	Y6	SCANMODE
V6	VDD	Y7	VSS
V7	VDD	Y8	VDD
V8	VSS	Y9	VDD
V9	VSS	Y10	VSS
V10	VDD	Y11	INJN1
V11	VDD	Y12	INJP1
V12	VSS	Y13	VDD
V13	VSS	Y14	VSS
V14	VDD	Y15	VSS
V15	VDD	Y16	VDD
V16	VSS	Y17	SCK_WRB
V17	VSS	Y18	SDA_RDB
V18	VDD	Y19	SMI_SSB_CSB
V19	VDD	Y20	SMO
V20	STAT0	Y21	YN17
V21	YN15	Y22	Y17
V22	Y15		
W1	Y38		
W2	YN38		
W3	ADDR9		
W4	VSS		

## 5.4 Pins by Name

This section provides an alphabetical list of the VSC3340-01 device pins.

A0	A22	ADDR3	C3	AN35	AA5
A1	A21	ADDR4	D3	AN36	AA4
A2	A20	ADDR5	E3	AN37	AA3
A3	A19	ADDR6	F3	AN38	AA2
A4	A18	ADDR7	U3	AN39	AA1
A5	A17	ADDR8	V3	APAD	G3
A6	A16	ADDR9	W3	CONFIG	Y5
A7	A15	ADDR10	Y3	CPUDATA0	G20
A8	A14	ANO	B22	CPUDATA1	F20
A9	A13	AN1	B21	CPUDATA2	E20
A10	A12	AN2	B20	CPUDATA3	D20
A11	A11	AN3	B19	CPUDATA4	C20
A12	A10	AN4	B18	CPUDATA5	C19
A13	A9	AN5	B17	CPUDATA6	C18
A14	A8	AN6	B16	CPUDATA7	C17
A15	A7	AN7	B15	INJN0	C12
A16	A6	AN8	B14	INJN1	Y11
A17	A5	AN9	B13	INJP0	C11
A18	A4	AN10	B12	INJP1	Y12
A19	A3	AN11	B11	RESETB	Y4
A20	AB20	AN12	B10	SCANMODE	Y6
A21	AB19	AN13	B9	SCK_WRB	Y17
A22	AB18	AN14	B8	SDA_RDB	Y18
A23	AB17	AN15	B7	SERPARB	W20
A24	AB16	AN16	B6	SMI_SSB_CSB	Y19
A25	AB15	AN17	B5	SMO	Y20
A26	AB14	AN18	B4	SNSN0	M20
A27	AB13	AN19	B3	SNSN1	L3
A28	AB12	AN20	AA20	SNSPO	L20
A29	AB11	AN21	AA19	SNSP1	M3
A30	AB10	AN22	AA18	STAT0	V20
A31	AB9	AN23	AA17	STAT1	U20
A32	AB8	AN24	AA16	TWS	T20
A33	AB7	AN25	AA15	VDD	C7
A34	AB6	AN26	AA14	VDD	C10
A35	AB5	AN27	AA13	VDD	C14
A36	AB4	AN28	AA12	VDD	C15
A37	AB3	AN29	AA11	VDD	D4
A38	AB2	AN30	AA10	VDD	D5
A39	AB1	AN31	AA9	VDD	D8
ADDR0	C6	AN32	AA8	VDD	D9
ADDR1	C5	AN33	AA7	VDD	D12
ADDR2	C4	AN34	AA6	VDD	D13

Pins by name *(continued)*

VDD	D16	VDD	K6	VDD	R14
VDD	D17	VDD	K7	VDD	R15
VDD	E4	VDD	K10	VDD	R18
VDD	E5	VDD	K11	VDD	R19
VDD	E8	VDD	K14	VDD	T4
VDD	E9	VDD	K15	VDD	T5
VDD	E12	VDD	K18	VDD	T8
VDD	E13	VDD	K19	VDD	T9
VDD	E16	VDD	L6	VDD	T12
VDD	E17	VDD	L7	VDD	T13
VDD	F6	VDD	L10	VDD	T16
VDD	F7	VDD	L11	VDD	T17
VDD	F10	VDD	L14	VDD	U4
VDD	F11	VDD	L15	VDD	U5
VDD	F14	VDD	L18	VDD	U8
VDD	F15	VDD	L19	VDD	U9
VDD	F18	VDD	M4	VDD	U12
VDD	F19	VDD	M5	VDD	U13
VDD	G6	VDD	M8	VDD	U16
VDD	G7	VDD	M9	VDD	U17
VDD	G10	VDD	M12	VDD	V6
VDD	G11	VDD	M13	VDD	V7
VDD	G14	VDD	M16	VDD	V10
VDD	G15	VDD	M17	VDD	V11
VDD	G18	VDD	N4	VDD	V14
VDD	G19	VDD	N5	VDD	V15
VDD	H4	VDD	N8	VDD	V18
VDD	H5	VDD	N9	VDD	V19
VDD	H8	VDD	N12	VDD	W6
VDD	H9	VDD	N13	VDD	W7
VDD	H12	VDD	N16	VDD	W10
VDD	H13	VDD	N17	VDD	W11
VDD	H16	VDD	N20	VDD	W14
VDD	H17	VDD	P6	VDD	W15
VDD	H20	VDD	P7	VDD	W18
VDD	J4	VDD	P10	VDD	W19
VDD	J5	VDD	P11	VDD	Y8
VDD	J8	VDD	P14	VDD	Y9
VDD	J9	VDD	P15	VDD	Y13
VDD	J12	VDD	P18	VDD	Y16
VDD	J13	VDD	P19	VREG	N3
VDD	J16	VDD	R6	VSS	C8
VDD	J17	VDD	R7	VSS	C9
VDD	J20	VDD	R10	VSS	C13
VDD	K3	VDD	R11	VSS	C16



Pins by name *(continued)*

VSS	D6	VSS	J11	VSS	P16
VSS	D7	VSS	J14	VSS	P17
VSS	D10	VSS	J15	VSS	P20
VSS	D11	VSS	J18	VSS	R3
VSS	D14	VSS	J19	VSS	R4
VSS	D15	VSS	K4	VSS	R5
VSS	D18	VSS	K5	VSS	R8
VSS	D19	VSS	K8	VSS	R9
VSS	E6	VSS	K9	VSS	R12
VSS	E7	VSS	K12	VSS	R13
VSS	E10	VSS	K13	VSS	R16
VSS	E11	VSS	K16	VSS	R17
VSS	E14	VSS	K17	VSS	R20
VSS	E15	VSS	K20	VSS	T3
VSS	E18	VSS	L4	VSS	T6
VSS	E19	VSS	L5	VSS	T7
VSS	F4	VSS	L8	VSS	T10
VSS	F5	VSS	L9	VSS	T11
VSS	F8	VSS	L12	VSS	T14
VSS	F9	VSS	L13	VSS	T15
VSS	F12	VSS	L16	VSS	T18
VSS	F13	VSS	L17	VSS	T19
VSS	F16	VSS	M6	VSS	U6
VSS	F17	VSS	M7	VSS	U7
VSS	G4	VSS	M10	VSS	U10
VSS	G5	VSS	M11	VSS	U11
VSS	G8	VSS	M14	VSS	U14
VSS	G9	VSS	M15	VSS	U15
VSS	G12	VSS	M18	VSS	U18
VSS	G13	VSS	M19	VSS	U19
VSS	G16	VSS	N6	VSS	V4
VSS	G17	VSS	N7	VSS	V5
VSS	H3	VSS	N10	VSS	V8
VSS	H6	VSS	N11	VSS	V9
VSS	H7	VSS	N14	VSS	V12
VSS	H10	VSS	N15	VSS	V13
VSS	H11	VSS	N18	VSS	V16
VSS	H14	VSS	N19	VSS	V17
VSS	H15	VSS	P3	VSS	W4
VSS	H18	VSS	P4	VSS	W5
VSS	H19	VSS	P5	VSS	W8
VSS	J3	VSS	P8	VSS	W9
VSS	J6	VSS	P9	VSS	W12
VSS	J7	VSS	P12	VSS	W13
VSS	J10	VSS	P13	VSS	W16

Pins by name *(continued)*

VSS	W17	YN0	C21
VSS	Y10	YN1	D21
VSS	Y14	YN2	E21
VSS	Y15	YN3	F21
VSS	Y7	YN4	G21
Y0	C22	YN5	H21
Y1	D22	YN6	J21
Y2	E22	YN7	K21
Y3	F22	YN8	L21
Y4	G22	YN9	M21
Y5	H22	YN10	N21
Y6	J22	YN11	P21
Y7	K22	YN12	R21
Y8	L22	YN13	T21
Y9	M22	YN14	U21
Y10	N22	YN15	V21
Y11	P22	YN16	W21
Y12	R22	YN17	Y21
Y13	T22	YN18	AA21
Y14	U22	YN19	AB21
Y15	V22	YN20	A2
Y16	W22	YN21	B2
Y17	Y22	YN22	C2
Y18	AA22	YN23	D2
Y19	AB22	YN24	E2
Y20	A1	YN25	F2
Y21	B1	YN26	G2
Y22	C1	YN27	H2
Y23	D1	YN28	J2
Y24	E1	YN29	K2
Y25	F1	YN30	L2
Y26	G1	YN31	M2
Y27	H1	YN32	N2
Y28	J1	YN33	P2
Y29	K1	YN34	R2
Y30	L1	YN35	T2
Y31	M1	YN36	U2
Y32	N1	YN37	V2
Y33	P1	YN38	W2
Y34	R1	YN39	Y2
Y35	T1		
Y36	U1		
Y37	V1		
Y38	W1		
Y39	Y1		

## 6 Package Information

The VSC3340-01 device is available in two package types. VSC3340JJ-01 is a 484-pin, flip chip ball grid array (FCBGA) with a 23 mm × 23 mm body size, 1 mm pin pitch, and 3.16 mm maximum height. The device is also available in a lead(Pb)-free (second-level interconnect only) package, VSC3340XJJ-01.

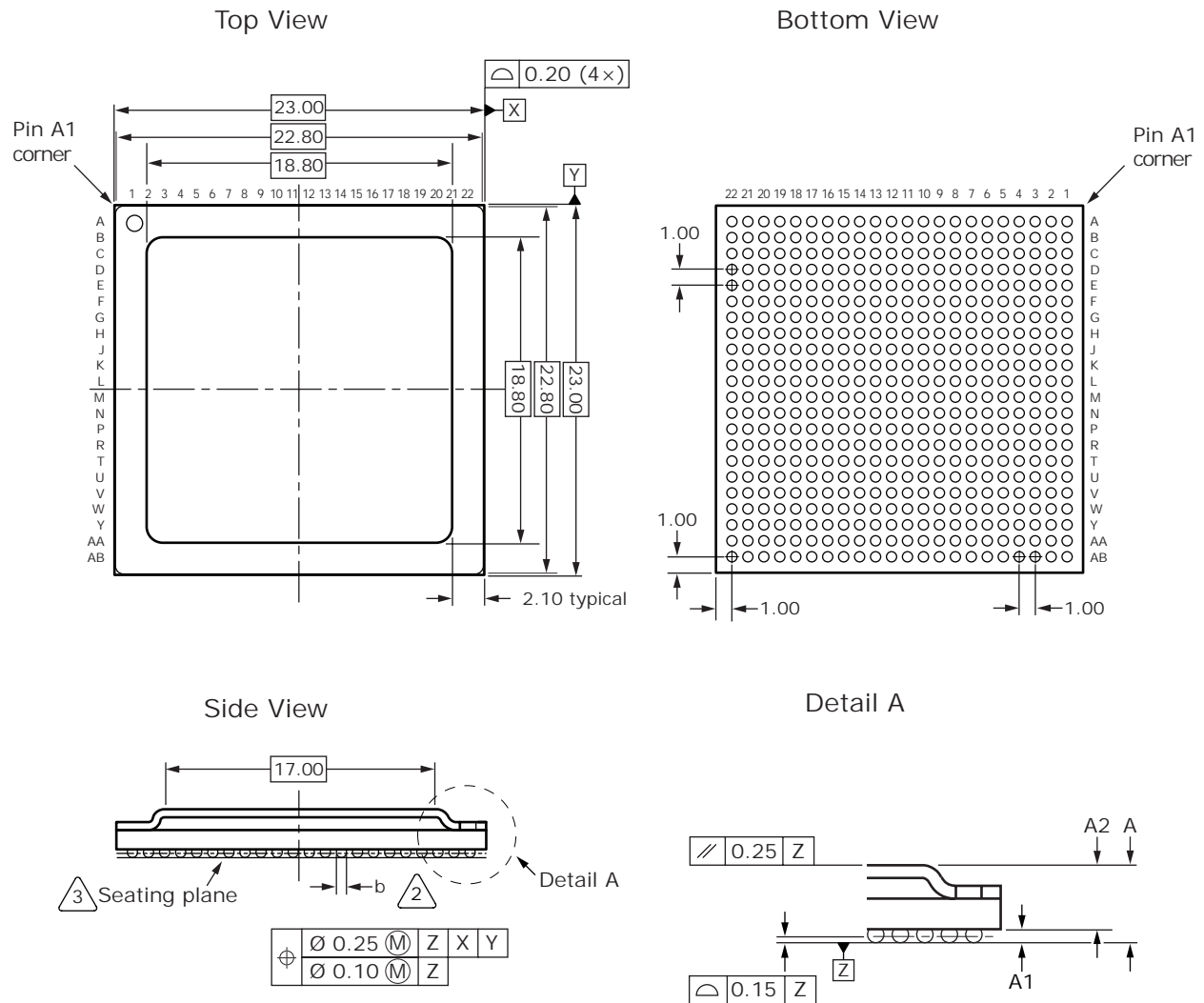
Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

This section provides the package drawing, thermal specifications, and moisture sensitivity rating for the VSC3340-01 device.

### 6.1 Package Drawing

The following illustration shows the package drawing for the VSC3340-01 device. The drawing contains the top view, bottom view, side view, detail view, dimensions, tolerances, and notes.

Figure 11. Package Drawing



Notes

- All dimensions and tolerances are in millimeters (mm).
- Dimension is measured at the maximum solder ball diameter, parallel to primary datum Z.
- Primary datum Z and seating plane are defined by the spherical crowns of the solder balls.
- Package corners are R0.5 mm.
- Heatspreader corners are R0.5 – 1.25 mm.
- Radial true position is represented by typical values.

## 6.2 Thermal Specifications

Thermal specifications for this device are based on the JEDEC JESD51 family of documents. These documents are available on the JEDEC Web site at [www.jedec.org](http://www.jedec.org). The thermal specifications are modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information about the thermal measurement method used for this device, see the JESD51-1 standard.

**Table 73. Thermal Resistances**

Symbol	°C/W	Parameter
$\theta_{JCTop}$	1.9	Die junction to package case top
$\theta_{JB}$	9.65	Die junction to printed circuit board
$\theta_{JA}$	15.6	Die junction to ambient
$\theta_{JMA}$ at 1 m/s	12.95	Die junction to moving air measured at an air speed of 1 m/s
$\theta_{JMA}$ at 2 m/s	11	Die junction to moving air measured at an air speed of 2 m/s

To achieve results similar to the modeled thermal measurements, the guidelines for board design described in the JESD51 family of publications must be applied. For information about applications using FCBGA packages, see the following:

- JESD51-2A, *Integrated Circuits Thermal Test Method Environmental Conditions, Natural Convection (Still Air)*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions, Forced Convection (Moving Air)*
- JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions, Junction-to-Board*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

## 6.3 Moisture Sensitivity

This device is rated moisture sensitivity level 4 as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

## 7 Ordering Information

The VSC3340-01 device is available in two package types. VSC3340JJ-01 is a 484-pin, flip chip ball grid array (FCBGA) with a 23 mm × 23 mm body size, 1 mm pin pitch, and 3.16 mm maximum height. The device is also available in a lead(Pb)-free (second-level interconnect only) package, VSC3340XJJ-01.

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table shows the ordering information for the VSC3340-01 device.

**Table 74. Ordering Information**

Part Order Number	Description
VSC3340JJ-01	484-pin FCBGA with a 23 mm × 23 mm body size, 1 mm pin pitch, and 3.16 mm maximum height
VSC3340XJJ-01	Lead(Pb)-free (second-level interconnect only), 484-pin FCBGA with a 23 mm × 23 mm body size, 1 mm pin pitch, and 3.16 mm maximum height