SPECTRUM DIGITAL INCORPORATED

Davinci-DM644x Evaluation Module

Technical Reference

2006 ***DSP Development Systems***

DaVinci-DM644x Evaluation Module Technical Reference

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Contents

About This Manual

This document describes the board level operations of the DM644x Evaluation Module (EVM). The EVM is based on the Texas Instruments DM644x Processor.

The DM644x Evaluation Module is a table top card that allows engineers and software developers to evaluate certain characteristics of the DM644x processor to determine if the processor meets the designers application requirements. Evaluators can create software to execute on board or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The DM644x Evaluation Module will sometimes be referred to as the DM644x EVM or EVM.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents, Application Notes and User Guides

Information regarding DaVinci™ technology can be found at the following Texas Instruments website:

http://www.ti.com/corp/docs/landing/davinci/index.html

Table 1: Manual History

Revision	History
A	Production Release
B	Corrected I^2C address of TVP5146
C	Corrected Pin 70, Table 30, DC1 connector

Table 2: Board History

Revision	History
C	Production Release

Chapter 1

Introduction to the DM644x EVM

Chapter One provides a description of the DM644x EVM along with the key features and a block diagram of the circuit board.

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1.1 Key Features

The DM644x EVM is a standalone development platform that enables users to evaluate and develop applications for the TI DaVinci processor family. Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.

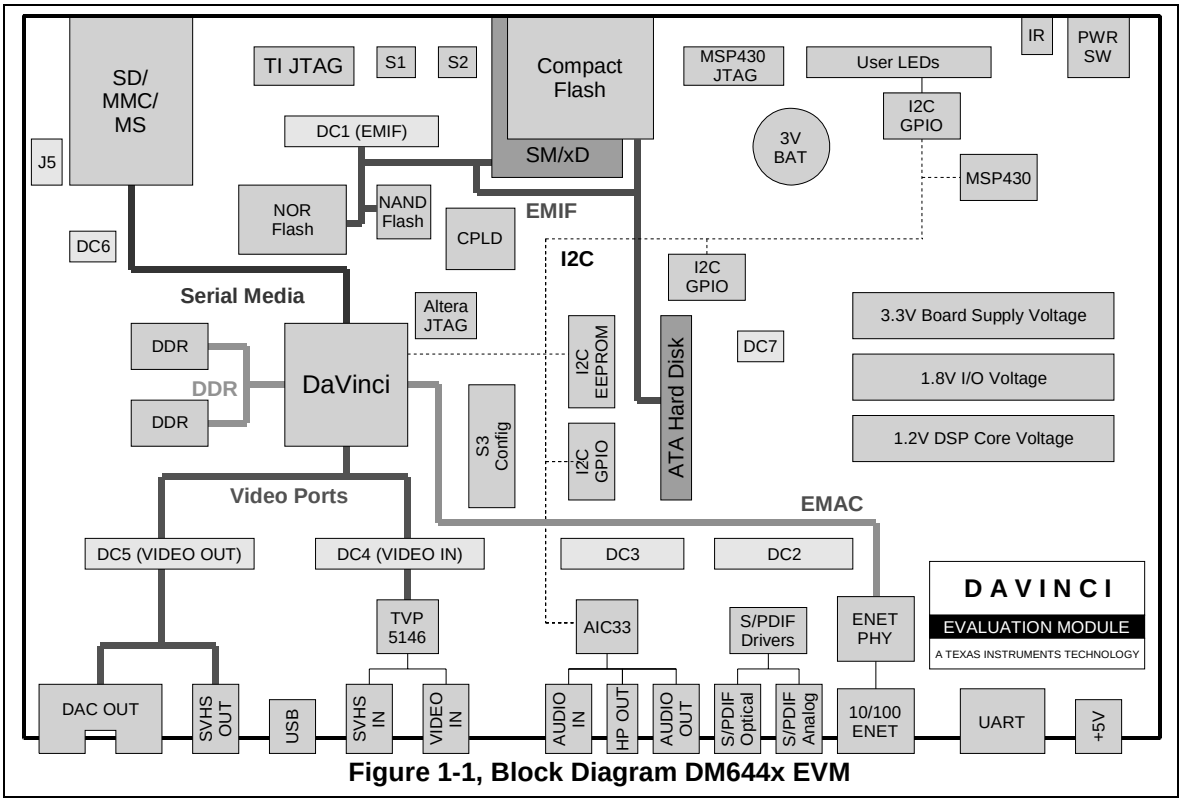

Figure 1-1, Block Diagram DM644x EVM

The EVM comes with a full complement of on board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments DM644x processor with an ARM processor operating up to 300 Mhz. and a C64xx DSP operating up to 600 Mhz.
- 1 video input port, supports composite or S video
- 4 video DAC outputs - component, RGB, composite
- 256 Mbytes of DDR2 DRAM
- UART, Media Card interface (SD card, xD card, SM card, MS card, MMC)
- 16 Mbytes of non-volatile Flash memory, 64 Mbytes NAND Flash, 4 Mbytes SRAM
- AIC33 stereo codec

- USB2 Interface
- 10/100 MBS Ethernet Interface
- IR Remote Interface, real time clock, via MSP430
- Configurable boot load options
- JTAG emulation interface
- 8 user LEDs
- Single voltage power supply (+5V)
- Expansion connectors for daughter card use
- ATA Interface, Vlynq Interface
- SPDIF Interface, analog, and optical

1.2 Functional Overview of the DM644x EVM

The DM644x on the DaVinci EVM interfaces to on-board peripherals through the 16-bit wide EMIF peripheral interface pins. The DDR2 memory is connected to its own dedicated 32 bit wide bus. The EMIF bus is also connected to the Flash, SRAM, NAND, and daughter card expansion connectors which are used for add-in boards.

On board video decoder and on chip encoders interface video streams to the DM644x processor. One decoder and 4 on chip DAC channels are standard on the EVM. On screen display functions are implemented in software on the DM644x processor.

An on-board AIC33 codec allows the DSP to transmit and receive analog audio signals. The I^2C bus is used for the codec control interface, while the McBSP controls the audio stream. Signal interfacing is done through 3.5mm audio jacks that correspond to microphone input, line input, and line output. The codec can select the line input as the active input.

The EVM includes 8 LEDs, IR interface, and Real time clock which can be used to provide the user with interactive feedback. These interfaces are implemented via software on a MSP430 and are accessed by reading and writing to the I^2C registers.

Media cards, ATA interface, VLYNQ, and ethernet MAC interfaces are integrated peripheral on the DM644x processor exploiting its system on a chip architecture.

An included 5V external power supply is used to power the board. On-board switching voltage regulators provide the +1.2V CPU core voltage and +3.3V for peripherals and +1.8V memory and DM644x I/O. The board is held in reset until these supplies are within operating specifications.

Code Composer communicates with the EVM through an external emulator via the 20 pin external JTAG connector.

1.3 Basic Operation

The EVM is designed to work with TI's Code Composer Studio development, or standard GDB tool environments. Code Composer communicates with the board through an external JTAG emulator. To start, follow the instructions in the Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

Detailed information about the EVM including examples and reference material is available on the EVM's CD-ROM.

1.4 Memory Map

The DaVinci family of processors have a large byte addressable address space, some limitations to byte addressing are determined by peripheral interconnection to the Davinci device. Program code and data can be placed anywhere in the unified address space. Addresses are multiple sizes depending on hardware implementation. Refer to the appropriate device data sheets for more details.

The memory map shows the address space of a generic DaVinci processor on the left with specific details of how each region is used on the right. By default, the internal memory sits at the beginning of the address space. Portions of memory can be remapped in software as L2 cache rather than fixed RAM.

The part incorporates a dual EMIF interface. One dedicated EMIF directly interfaces to the DDR2 memory. The other EMIF has 4 separate addressable regions called chip enable spaces (CS2-CS5). The Flash, NAND Flash, or SRAM are mapped into CE2 space and selectable via J4. Daughter cards use CE2 and CE3. When CE2 is used for daughter card interfacing J4 must be set appropriately. CS4 and CS5 are reserved for the VLYNQ interface on the EVM.

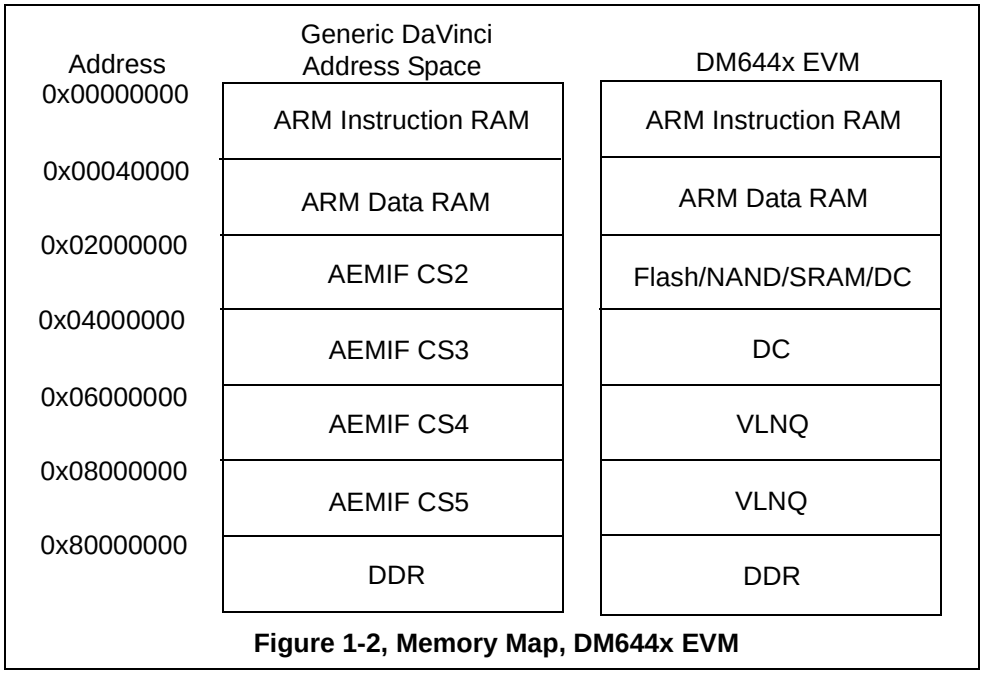

Figure 1-2, Memory Map, DM644x EVM

1.5 Configuration Switch Settings

The EVM has a single 10 position configuration switch that allow users to control the operational state of the processor when it is released from reset. The configuration switch is labeled S3 on the EVM board.

Switch S3 configures the boot mode that will be used when the DSP starts executing. By default the switches are configured to EMIF boot (out of 8-bit Flash) in little endian mode. The table below shows the settings for switch S3.

Table 1: Configuration Switch S3 Settings

Position	Name	Function	Boot Mode
1	COUT0	Boot Mode 0	00 - Boot from ROM NAND 01 - Boot from AEMIF 10 - Boot from ROM HPI 11 - Boot from ROM UART
2	COUT1	Boot Mode 1	
3	COUT2	Bus width: 0=8 bit, 1=16 bit	
4	COUT3	0=ARM boots DSP, 1=C64xx self boots	
5	YOUT4		
6	YOUT3		
7	YOUT2		
8	YOUT1		
9	YOUT0		
10	USER	For Demos	

1.6 Power Supply

The EVM operates from a single +5V external power supply connected to the main power input (J14), a 2.5 MM. barrel-type plug. Internally, the +5V input is converted into +1.2V, +1.8V and +3.3V using Texas Instruments swift voltage regulators. The +1.2V supply is used for the DSP core while the +3.3V supply is used for the DSP's I/O buffers and other chips on the board. The +1.8 volt supply is used for DM644x I/O, low voltage memory, and peripherals, and DDR2 memory.

There are four power test points on the EVM; TP14, TP25, TP26, and TP43. These test points provide a convenient mechanism to check the EVM's multiple power supplies. The table below shows the voltages for each test point and what the supply is used for.

Table 2: Power Test Points

Test Point	Voltage	Voltage Use
TP43	+1.2 V	DM644x Core
TP25	+1.2 V	DM644x Core/Power Down
TP26	+1.8 V	DDR2 Memory, DSP I/O, and logic
TP14	+3.3V	DSP I/O and logic

Chapter 2

Board Components

This chapter describes the operation of the major board components on the DM644x EVM.

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2.1 EMIF Interfaces

A separate 16 bit EMIF with four chip enables divide up the address space and allow for asynchronous accesses on the EVM. CE4 and CE5 are reserved for VLYNQ use allowing the EVM two dedicated chip enables. CE2 is used for Flash, NAND Flash, SRAM, and xD and SM Media cards. Both CE2 and/or CE3 can be routed to the daughter card interface connectors.

Table 1: EMIF Interfaces

Chip Select	Function
CE2	NOR Flash, NAND Flash, SRAM (see JP4 definition)
CE2	Daughter Card Interface (see JP4 definition)
CE3	Daughter Card Interface

2.1.1 DDR2 Memory Interface

The DM644x device incorporates a dedicated 32 bit wide DDR2 memory bus. The EVM uses two gigabit 16 bit wide memories on this bus, for a total of 256 megabytes of memory for program, data, and video storage. The internal DDR controller uses a PLL to control the DDR memory timing. The interface supports rates up to 166 Mhz., and is clocked on differential edges for optimal performance. Memory refresh for DDR2 is handled automatically by the DM644x internal DDR controller.

2.1.2 Flash, NAND Flash, SRAM Memory Interface

The DM644x has 16 megabytes of NOR Flash, or 64 megabytes of NAND Flash, or 4 megabytes of SRAM memory mapped into the CE2 space. This NOR Flash memory, and NAND Flash memory are used primarily for boot loading. SRAM is used for debugging application code. The CE2 space is configured as 16 bits wide on the DM644x EVM for NOR Flash and SRAM usage, and 8 bit wide for NAND flash usage.

2.1.3 ATA Interface

The DM644x integrates a standard ATA interface on chip. This interface is multiplexed with the EMIF interface at +1.8 volt levels. The EVM incorporates a standard Lap drive Hard Disk Drive connector, JP1. Level translators are used to translate the data to +3.3 volt interface levels and a CPLD is used to translate the control interface to +3.3V levels. Buffer control is implemented via the CPLD. The drive is selected via I^2C I/O expander U35 bit P6. When the hard drive is in use other peripherals such as the compact Flash interface and the xD/SM media cards on the EM bus are not accessible without reconfiguring the EMIF or I^2C select lines.

2.1.4 Compact Flash Interface

The EVM incorporates a PIO type Compact Flash interface. The Compact Flash is selected via I^2C expander U35 bit P5. The interface is multiplexed on the EMIF interface. When the Compact Flash interface is in use other interfaces such as the ATA or xD/SM card on the EMIF cannot be used without reconfiguring the EMIF or interface selects.

2.1.5 Memory Card Interface

The EVM supports a number of media card interfaces. On the EMIF the EVM supports xD/SM interfaces. These are selected via U35 I^2C I/O expander. On the peripheral interface the EVM supports MMC/MS/MSPro/SD.

When the xD/SM interface is used other interfaces such as the ATA or CF interface on the EMIF cannot be used without reconfiguring the EMIF or interface selects.

2.1.6 VLYNQ Interface

The DM644x brings its internal VLYNQ interface out to a mini PCI connector J16. The VLYNQ interface is multiplexed on the EM bus and this bus must be reconfigured after boot up to support VLYNQ. A multiplexer is used to minimize board layout stubs and allow as direct as possible interface for the VLYNQ signals.

2.1.7 UART Interface

The internal UART0 on the DM644x device is driven to connector J6. The UART's interface is level shifted and routed to the RS-232 line drivers prior to being brought out to a DB-9 connector, J6.

2.1.8 EMIF Buffer/Decoder Control CPLD

The EMIF buffer and decode functions are implemented with a CPLD. The EVM board incorporates an Altera MAX II EPM240TCG100 device. The device has 2 banks of I/O. One bank is used for +1.8 volt signals. The other bank is for+3.3 volt signals. This allows the device to do level shifting.

The CPLD incorporates the ATA control interface, CF control interface, xD/SM control interface along with a divide by 8 counter for video synchronization. The CPLD also incorporates various logic functions for buffer control and glue logic.

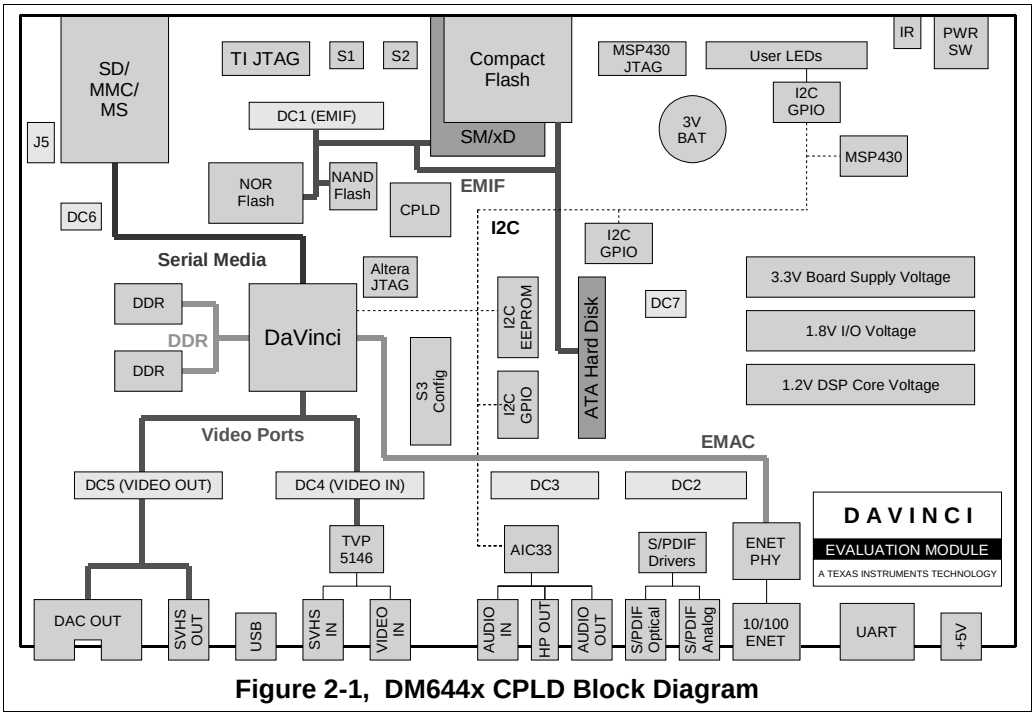

Figure 2-1, DM644x CPLD Block Diagram

2.2 Input Video Port Interfaces

The DM644x EVM supports video capture via the devices internal video ports. A Texas Instruments TVP5146 is used to decode composite video or S-video inputs into the device after being level shifted. J11 is used for the S-video inputs and J12 for the composite inputs on the EVM.

User inputs can be driven via daughter card connector DC4 when the on board level translator is tristate via driving control Capture Enable signal high on DC4.

2.2.1 On Chip Video Output DACs

The DM644x incorporates 4 output DACs to interface to various output standards. The DACs are buffered via opamps and driven to a quad RCA jack, J8. The outputs of the DACs are programmable to support composite video, component video, or RGB.

2.2.2 AIC33 Interface

The EVM uses a Texas Instruments TLV320AIC33 stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line output so the user can hear the output.

The codec communicates using two serial channels, one to control the codec's internal configuration registers and one to send and receive digital audio samples. The I^2C bus is used as the unidirectional control channel. The control channel is generally only used when configuring the codec, it is typically idle when audio data is being transmitted,

The McBSP is used as the bi-directional data channel. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The EVM examples generally use a 16-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the DSP side.

The codec has a programmable clock from a PLL1705 PLL device. The default system clock is 18.432 Mhz. The internal sample rate generate subdivides the 18.432 MHz clock to generate common frequencies such as 48KHz and 8KHz. The sample rate is set by a codec register. The figure below shows the codec interface on the DM644x EVM.

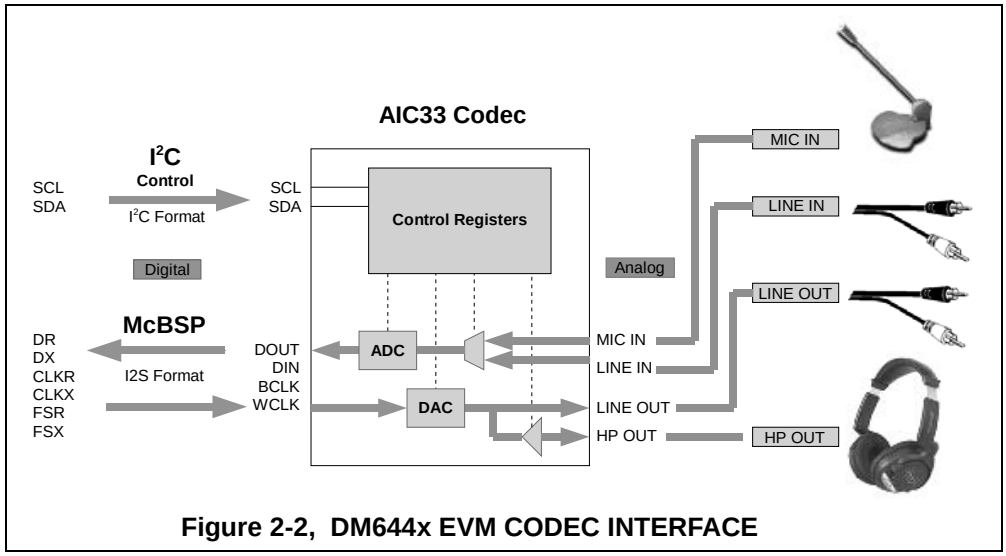

Figure 2-2, DM644x EVM CODEC INTERFACE

2.2.3 Audio PLL/VCXO Circuit/PLL1705 Clock Generator

The DM644x EVM implements a multiple PLL clock generator for creating the Audio clocks for the board.

In streaming video applications the audio and video sequences can lose synchronization. The DM644x uses a VCXO interpolation circuit to incrementally speed up or slow down the STCLK input to allow for this synchronization to remain locked.

The PWM0 and timer inputs on DM644x are used to control this feature. The PWM0 pin drives a PICX100-27W Voltage Controlled Oscillator which is divided by 8 in the CPLD and fed back into the timer input pin.

The STCLK is also a source clock for the PLL1705 programmable PLL device. This device creates the clocks for the AIC33 Codec, daughter card VIDCLK an AUDIOCLK.

The PLL1705 is programmable via an I^2C and Expander U18. Software sequencing on the I/O expander is required to interface correctly to the PLL1708's programmable inputs.

The diagram below is a simplified diagram of this clocking scheme.

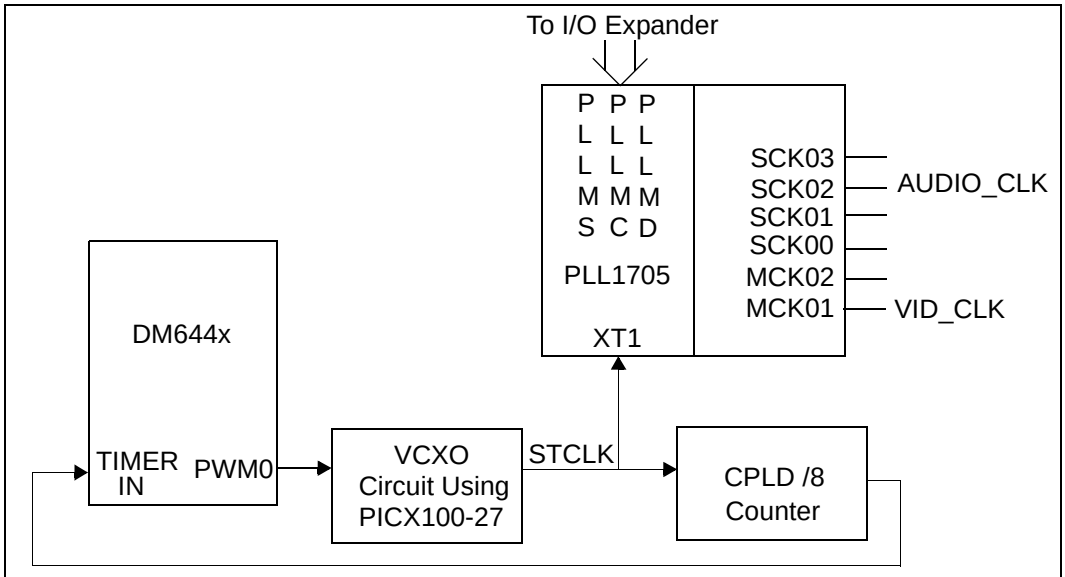

Figure 2-3, Audio PLL/VCXO Circuit/PLL1705 Clock Generator

2.3 Ethernet Interface

The DM644x integrates an ethernet MAC on chip. This interface is routed to the PHY via CBT switches. The EVM uses an Intel LXT971 PHY. The 10/100 Mbit interface is isolated and brought out to a RJ-45 standard ethernet connector, P2. The PHY directly interfaces to the DM644x. The ethernet address is stored in the I^2C serial ROM during manufacturing.

The RJ-45 has 2 LEDs integrated into its connector. The LEDs are green and yellow and indicate the status of the ethernet link. The green LED, when on, indicates link and when blinking indicates link activity. The yellow LED, when illuminated, indicates full duplex mode.

When configuring the PHY use the high drive option in the PHY register 26 to compensate for the routing length and extra capacitance of the CBT switches.

2.4 I^2C Interface

The I^2C bus on the DM644x is ideal for interfacing to the control registers of many devices. On the DM644x EVM the I^2C bus is used to configure the video decoder, stereo Codec, I/O expanders, and communicate with the MSP430. An I^2C ROM is also interfaced via the serial bus. The format of the bus is shown in the figure below.

Start	Slave Address	W	ACK	Sub Address	ACK-S	Data	ACK-S	Stop

Write Sequence

Start	Slave Address	R	Data	STOP

Read Sequence

Figure 2-4, I^2C Bus Format

The addresses of the on board peripherals are shown in the table below.

Table 2: I^2C Memory Map

Device	Address	R/W	Function
TVP5146	0x5D	R/W	Capture 1 Decoder
PCF 8574A	0x38	R/W	LEDs
PCF 8574A	0x39	R/W	PLL/User Switch
PCF 8574A	0x3A	R/W	Peripheral Selects
TLV320AIC33	0x1B	R/W	CODEC
24WC256	0x50	R/W	I^2C EEPROM
MSP430	0x23	R/W	LEDs, IR, RTC

2.4.1 I/O Expanders

The DM644x EVM uses three I^2C expanders to handle various bit I/O functions. Each of these is an bit I/O expander, a PCF8574A. At Power Up Reset the expanders are initialized to 0xFF, all ones. The functions for each of the I/O expanders are shown in the tables below.

Table 3: U2 I/O Expander

Pin Number	Function	States
P0	User LED DS8	0 = Turns LED On, 1 = Turns LED Off
P1	User LED DS7	0 = Turns LED On, 1 = Turns LED Off
P2	User LED DS6	0 = Turns LED On, 1 = Turns LED Off
P3	User LED DS5	0 = Turns LED On, 1 = Turns LED Off
P4	User LED DS4	0 = Turns LED On, 1 = Turns LED Off
P5	User LED DS3	0 = Turns LED On, 1 = Turns LED Off
P6	User LED DS2	0 = Turns LED On, 1 = Turns LED Off
P7	User LED DS1	0 = Turns LED On, 1 = Turns LED Off

Table 4: U18 I/O Expander

Pin Number	Function
P0	PLL Program Interface, PLL CSEL Pin
P1	PLL Program Interface, PLL SR Pin
P2	PLL Program Interface, PLL FS1 Pin
P3	PLL Program Interface, PLL FS2 Pin
P4	Spare IO1
P5	Spare IO2
P6	Spare IO3
P7	User DIP Switch *****

* - useful as input only
High Input - Switch in “ON” Position
Low Input - Switch in “OFF” Position

Table 5: U35 I/O Expander

Pin Number	Function	State
P0	USB Bus Drive	0 = Enable USB Bus Drive
P1	VDD IMX Enable	0 = Disables VDDIMX supply
P2	VLYNQ	0 = Turns on VLYNQ Mux U11
P3	Compact Flash Reset	Drives Reset Low to CF Adapter
P4	Not Used	
P5	WLAN Reset	0 = Removes Reset from WLAN
P6	ATA Select *	0 = Enables ATA Interface
P7	Compact Flash Select *	0 = Enables CF Interface

***** Only one interface, ATA or CF, can be enabled at a time

2.4.2 MSP430

The DM644x EVM incorporates infrared remote, real time clock, and some bit I/O in a MSP430 microcontroller. The I^2C interface is used on the DM644x processor to communicate to the MSP430. The MSP430 acts as a slave device on the I^2C bus.

2.5 SPDIF Analog, and Optical Interfaces

The McBSP's DX pin on the DM644x can be configured to operate as a SPDIF transmitter. The DM644x EVM supports a single SPDIF output with both analog and optical interfaces. The analog SPDIF output pin is routed to a level translator then to a driver and filter circuit before being output on J13. The same level translator is used for another driver which then drives the optical transmitter U65. When the SPDIF interface is enabled the TLV320AIC33 codec is disabled.

2.6 Daughter Card Interfaces

The EVM provides expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their EVM platform to extend its capabilities and provide customer and application specific I/O. The expansion connectors are for all major interfaces including memory, peripherals, and video expansion.

The pin outs for this interface are documented in Section 3.

The memory connector provides access to the DSP's EMIF signals to interface with memories and memory mapped devices.

The video capture port is brought out to the daughter card interface. Four signals are used to disable the on board video peripherals so that they can be used by the expansion connector. The table below indicates the operation of these signals.

Table 6: Daughter Card Video Enable

Signal	State To Enable Daughter Card Use	DM644x Signals Enables
CAPTURE_EN	1	DC4 YI0-YI7 PCLK,VD,HD
McBSP_EN	1	DC3 McBSP
ENET_ENABLE	1	DC2 GIOV33 pins

Other than the buffering, most daughter card signals are not modified on the board.

2.7 DM644x Core CPU Clock

The DM644x EVM uses a 27 Megahertz crystal to generate the input clock. The DM644x has an internal PLL which can multiply the input clock to generate the internal clock. The PLL multiplier is set via software on the DM644x device.

2.8 USB Clock

The DM644x EVM uses a 24 Mhz crystal for the USB II clock generator. The USB controller is completely integrated in the DM644x device.

2.9 Battery

The DM644x EVM incorporates a battery holder to provide backup power to the MSP430's real time clock when the power is not applied to the board. The optional battery should be +3 volt 20 millimeter coin type Lithium single cell.

Some common part numbers for batteries which should operate in the EVM are shown in the table below.

Table 7: Battery Part Numbers

Part Numbers
CR2032
DL2032
BR2032
CR2025
BR2025
CR2016
BR2016
DL2016

These batteries are available from Duracell, Eveready, Panasonic, Ray-O-Vac, Sanyo, Sony, Sieko, Toshiba, Varta, and other battery manufacturers.

Chapter 3

Physical Description

This chapter describes the physical layout of the DM644x EVM and its interfaces.

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3.1 Board Layout

The DM644x EVM is a 8.75 x 4.5 inch (210 x 115 mm.) ten (10) layer printed circuit board which is powered by an external +5 volt only power supply. Figure 3-1 shows the layout of the DM644x EVM.

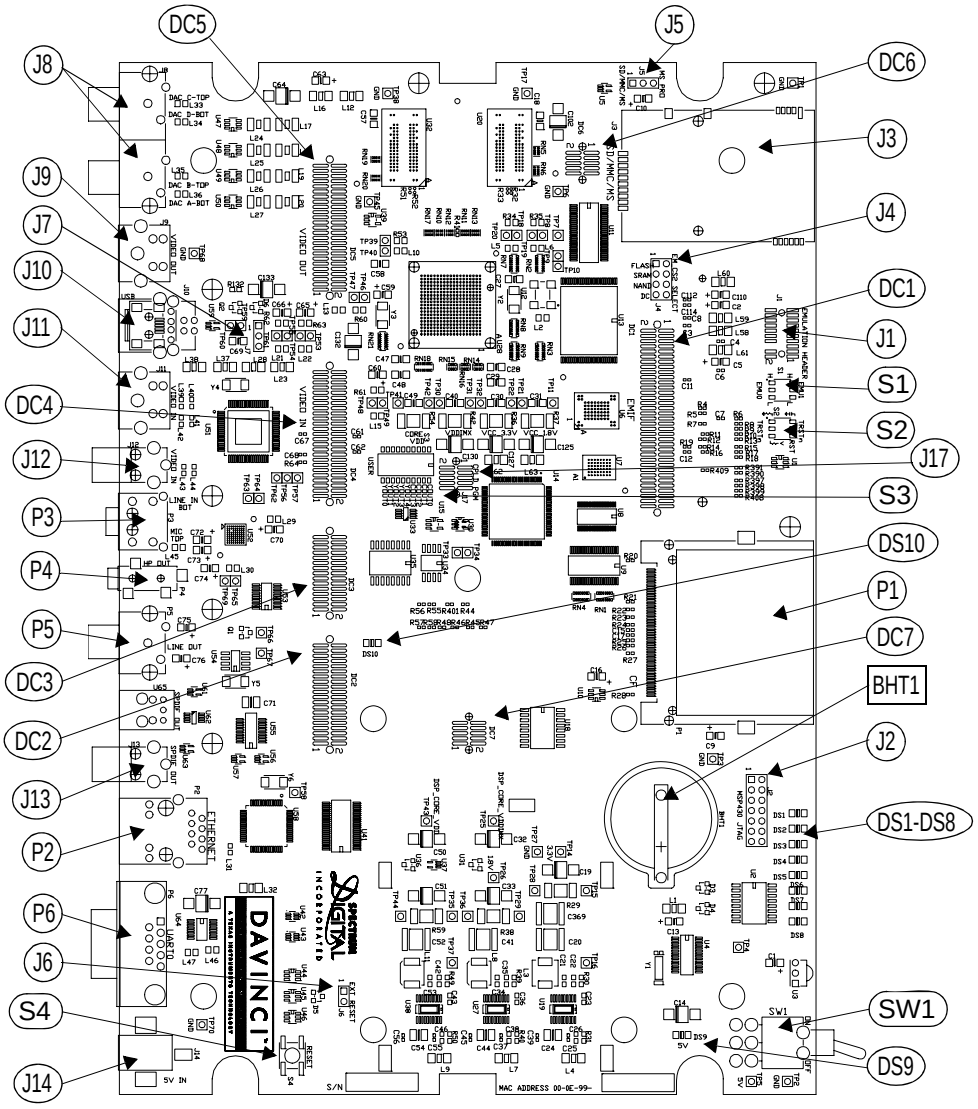

Figure 3-1, DM644x EVM, Interfaces Top Side

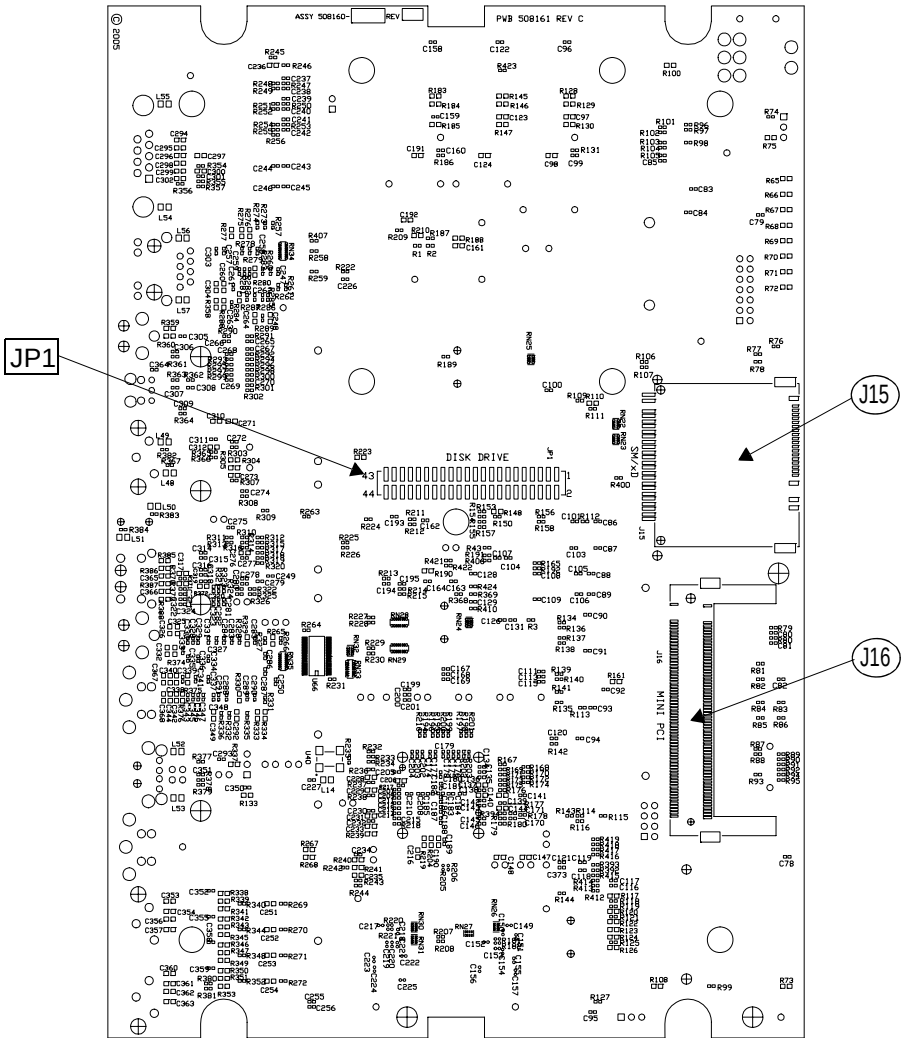

Figure 3-2, DM644x EVM, Interfaces, Bottom Side

3.2 Connectors

The EVM has seventeen (17) connectors providing interfaces to various peripherals. These connectors are described in the following sections.

Table 1: Connectors

Connector	Size	Function	Board Side
J1	20	Emulation Header	Top
J2	2x7	MSP430 JTAG	Top
J3	24	SD/MMC/MS	Top
J4	8	CS2 Select	Top
J5	3	SD/MMC/DC Termination Select	Top
J6	2	External RESET Interface	Top
J7	2	USB Host/Client Termination	Top
J8	8	DAC Connector	Top
J9	4	Video Out	Top
J10	2	USB	Top
J11	4	Video In	Top
J12	2	Video In	Top
J13	2	SPDIF Out	Top
J14	2	+5V In	Top
J15	46	SM/xD	Bottom
J16	2x62	Mini PCI for VLYNQ	Bottom
J17	2x5	CPLD Programming Header (Factory Use)	Top

3.2.1 J1, Emulation Header

The J1 Emulation Header is located on the top side of the board and is used to provide an interface to JTAG emulators. The connections for this connector is shown on page 33 of the schematics in appendix A. The pinout for the J1 connector is shown in the table below.

Table 2: J1, Emulation Header

Pin #	Signal	Pin #	Signal
1	DSP_TMS	2	TRSTn
3	DSP_TDI	4	TDIS
5	VCC_1.8V	6	Key-clipped
7	DSP_TDO	8	GND
9	DSP_RTCK	10	GND
11	CTI_TCK	12	GND
13	CTI_EMU0	14	CTI_EMU1
15	EMULATOR_RSTn	16	GND
17	NC	18	NC
19	NC	20	GND

3.2.2 J2, MSP430 JTAG Header

The J2 MSP430 JTAG Header is located on the top side of the board and is used to provide a programming interface to the MSP430 microcontroller. The connections for this connector are shown on page 28 of the schematics in appendix A. The pinout for the J2 connector is shown in the table below.

Table 3: J21, MSP430 JTAG Header

Pin #	**Signal**	**Pin #**	**Signal**
1	430_TDO	2	NC
3	430_TDI	4	MSP430_3V3
5	430_TMS	6	NC
7	430_TCK	8	430_TEST/VPP
9	GND	10	
11	NC	12	NC
13	NC	14	NC

3.2.3 J3, SD/MMC/MS Connector

The J3 SD/MMC/MS connector is located on the top side of the board and is used to provide an interface to a SD/MMC/MD card. The connections for this connector is shown on page 16 of the schematics in appendix A. The pinout for the J3 connector is shown in the table below.

Table 4: J3, SD/MMC/MS Connector

Pin #	Signal	Pin #	Signal
1	SD_DATA3	2	SD_CMD
3	GND	4	VCC_3.3V
5	SD_CLK	6	GND
7	SD_DATA0	8	SD_DATA1
9	SD_DATA2	10	GND
11	MS.CMD.BS	12	MS.DATA1
13	MS.DATA0	14	MS.DATA2
15	MS.INS/ VCC_3.3V	16	MS.DATA3
17	MS.CLK	18	VCC_3.3V
19	GND	20	VCC_3.3V
21	SD/MMC.INS/ VCC_3.3V	22	GND
23	GND	24	

3.2.4 J4, CS2 Select

The J4 connector is actually a 8 position jumper located on the top side of the board and is used to select the type of memory that the CS2 signal is routed to. The CS2 can be routed to the four signals shown in the figure below. Only one (1) device can be selected at a time. To reconfigure this signal, power down the EVM, change the jumper, and then power the board back up. Do **NOT** change this jumper with the power on. The connections for this connector is shown on page 10 of the schematics in appendix A.

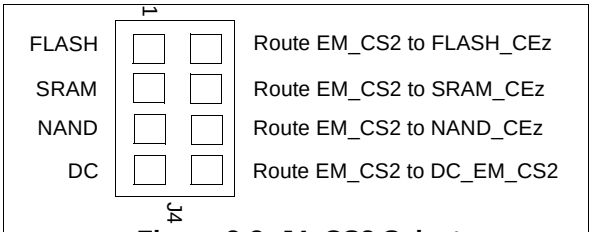

Figure 3-3, J4, CS2 Select

3.2.5 J5, SD/MMC/MS Termination Select

The J5 connector is a 3 position jumper located on the top side of the board and is used to select the termination (ground or VCC_3.3V)for the SD/MMC/MS connector (J3). Either the +3.3V (1-2 position) or Ground (2-3 position) must be selected. To reconfigure this termination, power down the EVM, change the jumper, and then power the board back up. Do **NOT** change this jumper with the power on. The connections for this connector are shown on page 16 of the schematics in appendix A.

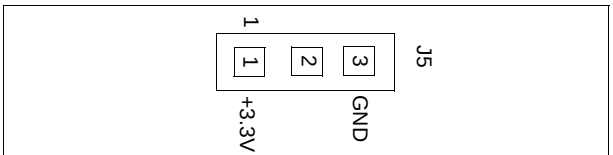

Figure 3-4, J5, SD/MMC/MS Termination Select

Table 5: J5, SD/MMC/MS Termination Select

Media Type	Position
SD	1-2
MMC	1-2
MS	1-2
MS PRO	2-3

3.2.6 J6, External RESET Interface

The J6 connector is a 2 position jumper located on the top side of the board and is used to externally reset the board. This connector is unpopulated as shipped from the factory. This circuitry parallels the RESET switch, S4. The connections for this connector are shown on page 34 of the schematics in appendix A.

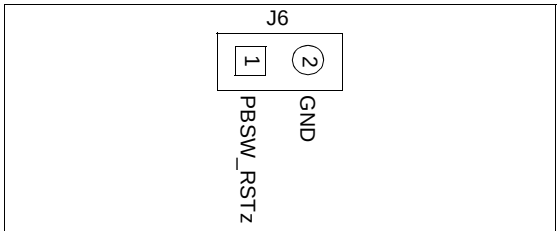

Figure 3-5, J6, External RESET Interface

3.2.7 J7, USB Host/Client Termination

The J7 connector is a 3 position jumper located on the top side of the board and is used to select the termination for the USB host/client configuration on USB connector J10. Either the +3.3V (1-2 position) or Ground (2-3 position) must be selected. This signal **must** be terminated. To reconfigure this termination, power down the EVM, change the jumper, and then power the board back up. Do **NOT** change this jumper with the power on. The connections for this connector are shown on page 21 of the schematics in appendix A.

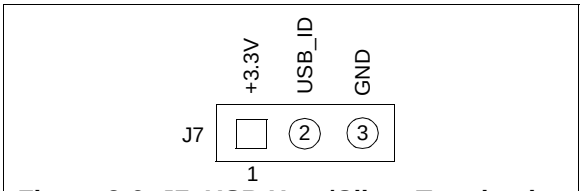

Figure 3-6, J7, USB Host/Client Termination

3.2.8 J8, Dual RCA Jack

The J8 connector is a dual RCA jack providing 4 DAC outputs. Do **NOT** plug into these connectors with the power on. The figure below shows this connector as viewed from the card edge. The position of each DAC output is identified. The connections for this connector are shown on page 25 of the schematics in appendix A.

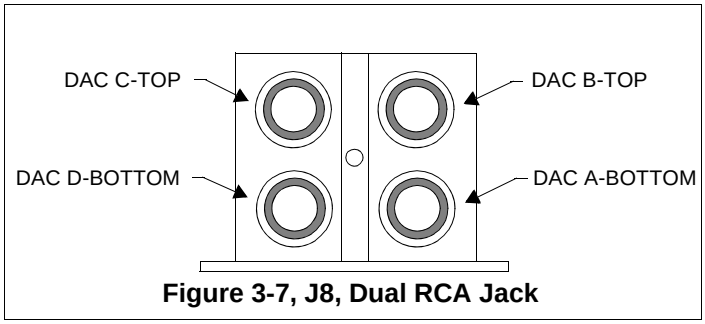

Figure 3-7, J8, Dual RCA Jack

3.2.9 J9, Video Out

Connector J9 is a four pin mini din connector which interfaces to an output display device. This connector brings out the DAC B (DAC B-TOP from J8) and DAC C (DAC C-TOP from J8). Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge. The connections for this connector are shown on page 25 of the schematics in appendix A.

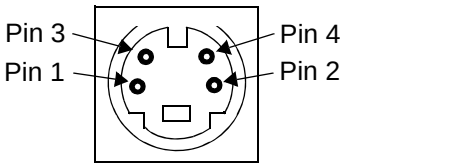

Figure 3-8, J9, Front View, Mini Din Connector

Table 6: J9, Video Out, Mini Din Connector

Pin #	Signal Name
1	Ground
2	Ground
3	DAC_IOUTB
4	DAC_IOUTC

3.2.10 J10, USB Connector

Connector J10 is a USB connector. Three different connectors can be mounted at location J10. The default connector is USB host. The three tables below show the signals on each possible connector. The connections for this connector are shown on page 21 of the schematics in appendix A.

Table 7: J10B, USB Peripheral Connector

Pins	Signal
1A	USB_VBUS
2B	USB_DM
3B	USB_DP
4B	GND
1,2	USB_SHIELD

Table 8: J10B, Mini A-B USB On The Go Connector

Pins	Signal
1AB	USB_VBUS
2AB	USB_DM
3AB	USB_DP
4AB	USB_ID
5AB	GND
5,6,7,8	USB_SHIELD

Table 9: J10C, USB Host Connector

Pins	Signal
1A	USB_VBUS
2A	USB_DM
3A	USB_DP
4A	GND
3,4	USB_SHIELD

3.2.11 J11, Video In

Connector J11 is a four pin mini din connector which interfaces to the TVP5146 encoder. This connector brings in a video signal (LUMA) to pin 9 on the TVP5146. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge. The connections for this connector are shown on page 24 of the schematics in appendix A.

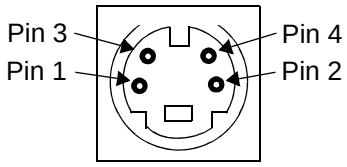

Figure 3-9, J11,Front View, Mini Din Connector

Table 10: J11, Video In, Mini Din Connector

Pin #	Signal Name
1	GND
2	GND
3	LUMA
4	Chroma

3.2.12 J12, Video In

J12 is an RCA jack used as a video input to the TVP5146 encoder. This connector brings in a video signal to pin 8 on the TVP5146. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge. The connections for this connector are shown on page 24 of the schematics in appendix A.

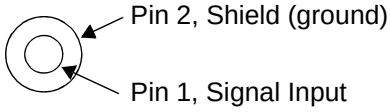

Figure 3-10, J12, Video In RCA Jack

Table 11: J12, Video In, RCA Jack

Pin #	Signal Name
1	Pin 8, TVP5146
2	GND

3.2.13 J13, SPDIF Out

J12 is an RCA jack used as an output from the DX signal on the DM644x. This connector brings out the SPDIF signal. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge. The connections for this connector are shown on page 27 of the schematics in appendix A.

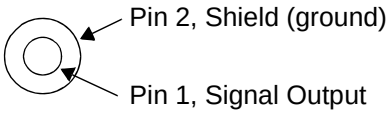

Figure 3-11, J13, SPDIF Out, RCA Jack

Table 12: J13, SPDIF, RCA Jack

Pin #	Signal Name
1	SPDIF Analog output
2	GND

3.2.14 J14, +5V Input

Connector J14 is the input power connector. This connector bring in +5 volts to the EVM. This is 2.5mm. jack. Inside of the jack is tied to On/Off power switch SW1. The other side is tied to ground and LED DS9. The figure below shows this connector as viewed from the card edge. The connections for this connector are shown on page 34 of the schematics in appendix A.

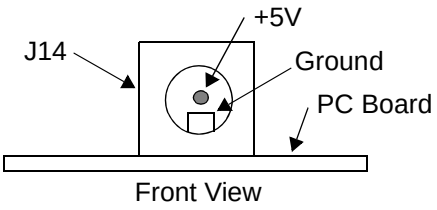

Figure 3-12, J14, +5 Volt Input Connector

3.2.15 J15, SM/xD Interface

Connector J14 provides an interface to SM/xD memory cards. This connector is located on the bottom side of the board. Do **NOT** plug into this connector with the power on. The table below shows the signals on this connector. The connections for this connector are shown on page 34 of the schematics in appendix A.

Table 13: J15, SM/xD Interface

Connector Pin Name	EVM Signal	Connector Pin Name	EVM Signal
SM.I/01	3V3.EM.D0	SM.LVD	NC
SM.I/02	3V3.EM.D1	SM.VCC1	VCC_3.3V
SM.I/03	3V3.EM.D2	SM.VCC2	VCC_3.3V
SM.I/04	3V3.EM.D3	SM.VSS1	GND
SM.I/05	3V3.EM.D4	SM.VSS2	GND
SM.I/06	3V3.EM.D5	xD.VSS2	GND
SM.I/07	3V3.EM.D6	xD.CD	xD.CD/VCC_3.3V
SM.I/08	3V3.EM.D7	xD.R/B	3V3.WAIT/BUSY
SM.CLE	3V3.CLE_EM_A2	xD.$\overline{RE}$	3V3.READ_OE
SM.ALE	3V3.ALE_EM_A1	xD.$\overline{CE}$	3V3.SM_CEz
SM.$\overline{WE}$	3V3.WRITE_WE	xD.CLE	3V3.CLE_EM_A2
SM.$\overline{WP}$	GND	xD.ALE	3V3.ALE_EM_A1
SM.R/B	3V3.WAIT/BUSY	xD.$\overline{WE}$	3V3.WRITE_WE
SM.$\overline{RE}$	3V3.READ.OE	xD.$\overline{WP}$	SM.Xd.wp
SM.$\overline{CE}$	3V3.SM_CEz	xD.VSS1	GND
SM.CD	SM.CD/ VCC_3.3V	xD.I/O0	3V3.EM_D0
SM.OPTION	GND	xD.I/O1	3V3.EM_D1
SM.26	GND	xD.I/O2	3V3.EM_D2
SM.25	GND	xD.I/O3	3V3.EM_D3
SM.SENS.1	GND	xD.I/O4	3V3.EM_D4
SM.SENS.2	GND	xD.I/O5	3V3.EM_D5
xD.VCC1	VCC_3.3V	xD.I/O6	3V3.EM_D6
xD.VCC2	VCC_3.3V	xD.I/O7	3V3.EM_D7

3.2.16 J16, Mini PCI VLYNQ Interface

Connector J16 provides an interface to TI supported VNLYNQ cards. This mini-PCI connector is located on the bottom side of the board. Do **NOT** plug into this connector with the power on. The table below shows the signals on this connector. The connections for this connector are shown on page 32 of the schematics in appendix A.

Table 14: J16, VLYNQ Card Interface

Pin #	Signal
1,2,7-9,11-14,17, 18,EMC1,EMC2, EMC3,EMC4,93,98, 100,112,121, 104-110,113, 115-120,122-124	NC
15,20,23,25,26,27 32,33,34,35,37,41, 42,45-49,50-62, 64-69,71-87, 90-92,94-96, 99,101,102,114	GND
10,111	VCC_1.8V
19,28,31,40,63,70, 88,89,97,103	VCC_3.3V
3	SLP_CLK_EN
4	SLP_REG/WAKEUP
5	PM_EN
6	WLAN_INTR
16	SD_CLK/VLYNQ_CLK
21	SD_CMD/VLYNQ_RXD0
22	SD_DATA3/VLYQ_RXD1
24	VLYNQ_SCRUN/SD_DATA0
26	1V8.WLAN_RESET
29	VLYNQ_RXD2
30	VLYNQ_RXD3
36	SD_DATA2/VLYNQ_TXD0
38	VLYNQ_TXD2
39	VLYNQ_TXD3
43	SD_DATA1/VLYNQ_TXD1

3.2.17 J17, FPGA Programming Header

Connector J17 is a 10 pin header that provides a programming interface to the FPGA, U14. This connector is located on the top side of the board. Do **NOT** plug into this connector with the power on. The table below shows the signals on this connector. This connector is for factory use only. Reprogramming this CPLD affects the functionality of your EVM.

Table 15: J17, FPGA Programming Header

Pin #	Signal	Pin #	Signal
1	ISR_TCK	2	GND
3	ISR_TDO	4	VCC_1.8V
5	ISR_TMS	6	NC
7	NC	8	NC
9	ISR_TDI	10	GND

3.3 Peripheral Connectors

Table 16: Peripheral Connectors

Connector	Pins	Signal	Board Side
P1	50	Compact Flash	Top
P2	8	Ethernet	Top
P3	4	Line In/Mic	Top
P4	2	HP Out	Top
P5	4	Line Out	Top
P6	8	UART0	Top

3.3.1 P1, Compact Flash Connector

The P1 connector is located on the top side of the board and is used to provide an interface to a Compact Flash memory card. This is a 2 x 25 pin male connector. The connections for this connector is shown on page 19 of the schematics in appendix A. The pinout for the P1 connector is shown in the table below.

Table 17: P1, Compact Flash Connector

Pin #	Signal	Pin #	Signal
1	GND	2	3V3.EM_D3
3	3V3.EM_D4	4	3V3.EM_D5
5	3V3.EM_D6	6	3V3.EM_D7
7	3V3.CF.ATA_CS0	8	GND
9	GND	10	GND
11	GND	12	GND
13	Pin 3, U10	14	GND
15	GND	16	GND
17	GND	18	3V3.CF.ATA2_EM_A0
19	3V3.CF.ATA1_EM_BA1	20	3V3.CF.ATA0_EM_BA0
21	3V3.EM_D0	22	3V3.EM_D1
23	3V3.EM_D2	24	
25	VCC_3.V/3V3.CF_CD2	26	VCC_3.V/3V3.CF_CD1
27	3V3.EM_D11	28	3V3.EM_D12
29	3V3.EM_D13	30	3V3.EM_D14
31	3V3.EM_D15	32	3V3.CF.ATA_CS1
33	NC	34	3V3.CF.READ_OE
35	3V3.CF.WRITE_WE	36	VCC_3.3V
37	3V3.CF.INTRQ_EM_RNW	38	Pin 3, U10
39	GND	40	NC
41	3V3.CF_RESETz	42	3V3.CF.WAIT/BUSY
43	NC	44	VCC_3.3V
45	NC	46	NC
47	3V3.EM_D8	48	3V3.EM_D9
49	3V3.EM_D10	50	GND

3.3.2 P2, Ethernet Interface

The P2 connector is located on the top side of the board and is used to provide an Ethernet interface. This is a standard RJ-45 connector. The connections for this connector is shown on page 22 of the schematics in appendix A. The pinout for the P2 connector is shown in the table below.

Table 18: P2, Ethernet Interface

Pin #	Signal	Pin #	Signal
1	LXT_TDP	2	LXT_TDM
3	LXT_RDP	4	LXT_TDCT
5	NC	6	LXT_RDM
7	NC	8	GND
9	VCC_3.3V	10	LED1-
11	VCC_3.3V	12	LINKLED-

3.3.3 P3, Line In/Mic Interface

The P2 connector is provides a stereo input (lower) and microphone input (upper) to the TVL320AIC33 on the EVM. This connector is located on the top side of the board. A view of the connector from the card edge is shown in the figure below. The signals present on this connector are defined in the following table. The connections for this connector is shown on page 26 of the schematics in appendix A.

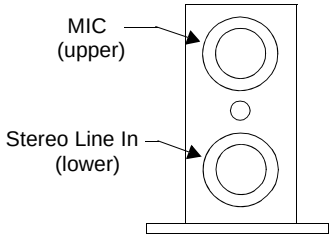

Figure 3-13, P3, Line In/Mic Interface

Table 19: P3, Line In/Mic Interface

Pin #	Signal	Input
1	Isolated Ground	Mic
2	MIC3L/MIC3R	Mic
3	MIC3L/MIC3R	Mic
4	Isolated Ground	Line In
5	LINE1R+/LINE2R+	Line In
6	LINE1L+/LINE2L+	Line In

3.3.4 P4, Headphone Out

The P4 connector is a stereo headphone output from the TVL320AIC33 on the EVM. This connector is located on the top side of the board. A view of the connector from the card edge is shown in the figure below. The signals present on this connector are defined in the following table. The connections for this connector is shown on page 26 of the schematics in appendix A.

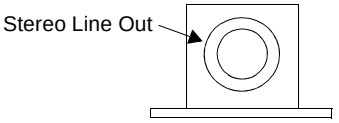

Figure 3-14, P4, Headphone Out Interface

Table 20: P4, Headphone Out Interface

Pin #	Signal
1	Isolated Ground
2	HPLOUT
3	HPROUT
4	NC

3.3.5 P5, Dual Output RCA Jack

The P5 connector is a dual output RCA jack bringing audio from the TVL320AIC33 on the EVM. This connector is located on the top side of the board. A view of the connector from the card edge is shown in the figure below. The signals present on this connector are defined in the following table. The connections for this connector is shown on page 26 of the schematics in appendix A.

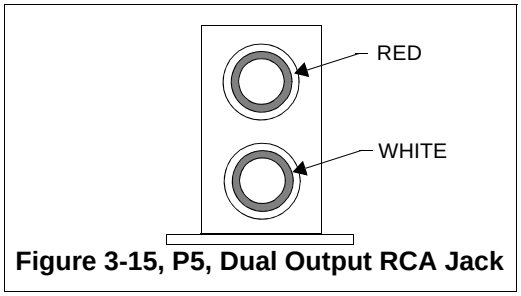

Figure 3-15, P5, Dual Output RCA Jack

Table 21: P5, Dual Output RCA Jack

Pin #	Signal
1	Isolated Ground
2	LEFT_LO+
3	RIGHT_LO+

3.3.6 P6, UART0

The P6 connector is a 9 pin make D-connector which provides a UART interface to the EVM. This connector interfaces to the MAX 3221 RS-232 line driver (U64) and is located on the top side of the board. A view of the connector from the card edge is shown in the figure below. The signals present on this connector are defined in the following table. The connections for this connector is shown on page 20 of the schematics in appendix A.

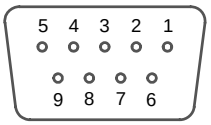

Figure 3-16, P6, DB9 Male Connector

The pin numbers and their corresponding signals are shown in the table below. This corresponds to a standard dual row to DB-9 connector interface used on personal computers.

Table 22: P6, UART0 Pinout

Pin #	Signal Name	Direction
1	NC	N/A
2	S_A_RXD	In
3	S_A_TXD	Out
4	NC	N/A
5	GND	N/A
6	NC	N/A
7	S_A_TXD	Out
8	S_A_TXD	Out
9	NC	N/A
10,11	Earth Ground	N/A

3.4 JP1, ATA Interface Connector

The JP1 connector is located on the bottom side of the board and is used to provide an ATA interface to a hard disk drive. This is a 2 x 22 pin male connector. The connections for this connector is shown on page 18 of the schematics in appendix A. The pinout for the JP1 connector is shown in the table below.

Table 23: JP1, ATA Interface

Pin #	Signal	Pin #	Signal
1	ATA RESETn	2	GND
3	ATA.DD7	4	ATA.DD8
5	ATA.DD6	6	ATA.DD9
7	ATA.DD5	8	ATA.DD10
9	ATA.DD4	10	ATA.DD11
11	ATA.DD3	12	ATA.DD12
13	ATA.DD2	14	ATA.DD13
15	ATA.DD1	16	ATA.DD14
17	ATA.DD0	18	ATA.DD15
19	GND	20	NC
21	ATA.DMARQ	22	GND
23	ATA.DIOW	24	GND
25	ATA.DIOR	26	GND
27	ATA.IORDY	28	ATA_CSEL, TP34
29	ATA.DMACK	30	GND
31	ATA.INTRQ	32	GND
33	ATA.DA1	34	TP33
35	ATA.DA0	36	ATA.DA2
37	ATA.CS0	38	ATA.CS1
39	ATA.DASPn	40	GND
41	VCC_5V	42	VCC_5V
43	GND	44	NC

3.5 LEDs

The EVM has ten (10) LEDs which are located on the top side of the board. Eight of these LEDs (DS1-8) are under user control and addressed over the I^2C bus. One LED (DS9) indicates the presence of +5 volts on the board. The remaining LED (DS10) indicates a hard disk drive is plugged into the EVM. Additional information regarding the LEDs are shown in the table below.

Table 24: LEDs

LED #	Use	Color	Schematic Page
DS1	User Defined	Green	27
DS2	User Defined	Green	27
DS3	User Defined	Green	27
DS4	User Defined	Green	27
DS5	User Defined	Green	27
DS6	User Defined	Green	27
DS7	User Defined	Green	27
DS8	User Defined	Green	27
DS9	+5V	Green	34
DS10	+3.3V	Red	18

3.6 Switches

The EVM has five (5) switches. The function of these switches are shown in the table below.

Table 25: Switches

Switch	Function	Type	Board Side	Schematic Page
S1	EMU0/1 Selection	DIP	Top	33
S2	TRSTn Select	DIP	Top	33
S3	Boot Configuration Options	DIP	Top	10
S4	RESET	Push button	Top	34
SW1	Power On/Off	Toggle	Top	34

3.6.1 S1, EMU0/1 Select Switch

S1 is a 2 position DIP switch providing 4 options in selecting the state of the EMU0 and EMU1 pins on the processor. The connections for this switch are shown on page 33 of the schematics in appendix A. A view of the switch is shown in the figure below. The selection options with this switch are in the table below.

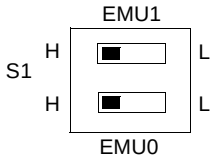

Figure 3-17, S1, EMU0/1 Select Switch

Table 26: S1, EMU0/1 Select

State at Reset EMU0	State at Reset EMU1	Function
L	L	Emulation Debug ARM JTAG Enabled
L	H	Not Defined
H	L	Not Defined
H	H	Emulation Debug * Both ARM & DSP JTAG Enabled

* is the factory shipped configuration

3.6.2 S2, TRSTn Select Switch

S2 is a 2 position DIP switch providing 4 options in selecting the state of the TRST signal for JTAG emulation. The connections for this switch are shown on page 33 of the schematics in appendix A. A view of the switch is shown in the figure below. The selection options with this switch are in the table below.

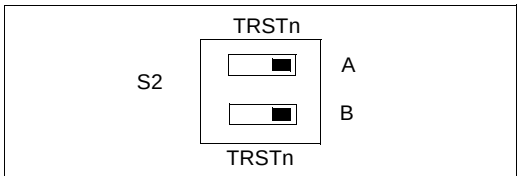

Figure 3-18, S2, TRST Select

Table 27: S2, TRST Select

Switch	Position	Function
A	Right	TRST Pull up
A	Left	TRST Pull down *
B	Right	TRST low on power up Reset
B	Left	Delay via capacitor (capacitor not populated) *

* is the factory shipped configuration

3.6.3 S3, Processor Configuration/Boot Load Options

S2 is a 10 position DIP switch providing 9 options in selecting the processor configuration and boot load modes. when a switch is in the "**ON**" position the specific function is selected. The connections for this switch are shown on page 10 of the schematics in appendix A. A view of the switch is shown in the figure below. The selection options with this switch are in the table below.

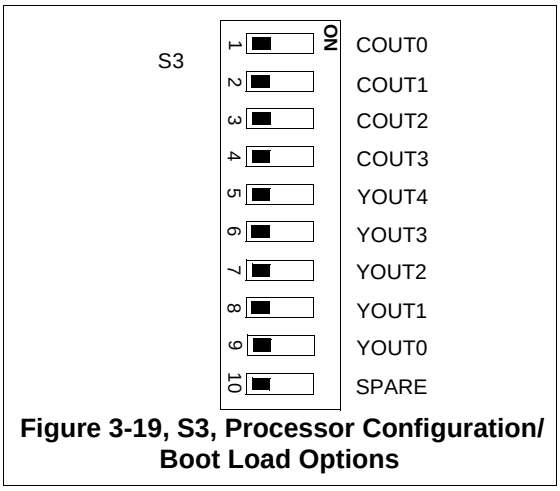

Figure 3-19, S3, Processor Configuration/ Boot Load Options

Table 28: S3, Processor Configuration/Boot Load Options

Position	Name	Function
1	COUT0	Bootmode 0
2	COUT1	Bootmode 1
3	COUT2	Bus width: 0=8 bit, 1=16 bit
4	COUT3	0=ARM boots DSP, 1=C64xx self boots
5	YOUT4	
6	YOUT3	
7	YOUT2	
8	YOUT1	
9	YOUT0	
10	USER	For Demos

3.6.4 S4, RESET

Switch S4 is a push button rest switch that will RESET the processor. This switch is in parallel with J6. The connections for this switch are shown on page 34 of the schematics in appendix A.

3.6.5 SW1, Power On/Off

Switch S1 is a toggle switch that provides power to the EVM. The connections for this switch are shown on page 34 of the schematics in appendix A.

3.7 Daughter Card Connectors

The EVM has seven connectors that are available for daughter card connections. These connectors make many of the signals on the EVM available to be used by external logic. The signals on each of the connectors are described in the following tables. The table below lists the connectors.

Table 29: Daughter Card Connectors

Connector	Size	Function	Board Side	Schematic Page
DC1	2x35	EMIF	Top	29
DC2	2x20	GIOV33/Ethernet	Top	31
DC3	2x15	SPI, McBSP, I^2C	Top	31
DC4	2x20	Video In	Top	30
DC5	2x25	Video Out	Top	30
DC6	2x5	SD Interface	Top	31
DC7	2x5	Power	Top	35

3.7.1 DC1, EMIF Expansion Connector

Table 30: DC1, EMIF Expansion Connector

Pin #	Signal	Pin #	Signal
1	B.EM_A21	2	B.EM_A20
3	B.EM_A19	4	B.EM_A18
5	B.EM_A17	6	B.EM_A16
7	B.EM_A15	8	B.EM_A14
9	GND	10	GND
11	B.EM_A13	12	B.EM_A12
13	B.EM_A11	14	B.EM_A10
15	B.EM_A9	16	B.EM_A8
17	B.EM_A7	18	B.EM_A6
19	GND	20	GND
21	B.EM_A5	22	B.EM_A4
23	B.EM_A3	24	CLE_EM_A4
25	B.EM_A1	26	ATA2_EM_A0
27	GND	28	GND
29	ATA_CS1	30	ATA_CS0
31	ATA1_EM_BA1	32	ATA0_EM_BA0
33	WRITE_WE	34	READ_OE
35	WAIT/BUSY	36	INTRQ_EM_RNW
37	GND	38	GND
39	EM_D15	40	EM_D14
41	EM_D13	42	EM_D12
43	EM_D11	44	EM_D10
45	GND	46	GND
47	EM_D9	48	EM_D8
49	EM_D7	50	EM_D6
51	EM_D5	52	EM_D4
53	GND	54	GND
55	EM_D3	56	EM_D2
57	EM_D1	58	EM_D0
59	EM_CS3	60	DC_EM_CS2
61	1.8V.SYS_RESETz	62	CLKOUT0
63	GND	64	GND
65	VCC_3.3V	66	VCC_3.3V
67	GND	68	GND
69	VCC_5V	70	VCC_1.8V

3.7.2 DC2, GIOV33/Ethernet Connector

Table 31: DC2, GIOV33/Ethernet Connector

Pin #	Signal	Pin #	Signal
1	GND	2	GND
3	GIOV33_0	4	GIOV33_1
5	GIOV33_2	6	GIOV33_3
7	GIOV33_4	8	GIOV33_5
9	GND	10	GND
11	GIOV33_6	12	GIOV33_7
13	GIOV33_8	14	GIOV33_9
15	GIOV33_10	16	GIOV33_11
17	GND	18	GND
19	GIOV33_12	20	GIOV33_13
21	GIOV33_14	22	GIOV33_15
23	GIOV33_16	24	GND
25	GND	26	3V3.SYS_RESETz
27	ENET_ENABLEz	28	GND
29	VCC_1.8V	30	3V3.UART_RXD1
31	VCC_1.8V	32	3V3.UART_TXD1
33	GND	34	GND
35	VCC_3.3V	36	VCC_3.3V
37	VCC_5V	38	VCC_5V
39	GND	40	GND

3.7.3 DC3, SPI, McBSP, I²C Connector

Table 32: DC3, SPI, McBSP, I²C Connector

Pin #	Signal	Pin #	Signal
1	SPI_EN1	2	SPI_EN0
3	SPI_DI	4	SPI_DO
5	SPI_CLK	6	TIMER_IN_DC3
7	GND	8	GND
9	DR	10	DX
11	CLKR	12	CLKX
13	FSR	14	FSX
15	GND	16	GND
17	1.8V.SYS_RESETz	18	1.8V.I2C_CLK
19	McBSP_EN	20	1.8V.I2C_DATA
21	AUDIO_CLK	22	GND
23	GND	24	1.8V_DC3_PCLK
25	VCC_3.3V	26	VCC_3.3V
27	GND	28	GND
29	VCC_5V	30	VCC_1.8V

3.7.4 DC4, Video Input Connector

Table 33: DC4, Video Input Connector

Pin #	Signal	Pin #	Signal
1	1.8V.SYS_RESETz	2	CAPTURE_EN
3	GND	4	GND
5	GIO1	6	GIO4
7	GND	8	GND
9	PWM1	10	PWM2
11	GND	12	GND
13	Y10	14	Y11
15	Y12	16	Y13
17	Y14	18	Y15
19	Y16	20	Y15
21	GND	22	GND
23	GND	24	HD
25	PCLK/1V8.DC_PCLK	26	VD
27	GND	28	GND
29	CI0	30	CI1
31	CI2	32	CI3
33	CI4	34	CI5
35	CI6	36	CI7
37	GND	38	GND
39	1V8.I2C_CLK	40	1V8.I2C_DATA
41	VCC_1.8V	42	VCC_1.8V
43	GND	44	GND
45	VCC_3.3V	46	VCC_3.3V
47	GND	48	GND
49	VCC_5V	50	VCC_5V

3.7.5 DC5, Video Output Connector

Table 34: DC5, Video Output Connector

Pin #	Signal	Pin #	Signal
1	GIO0	2	GIO2
3	GIO3	4	GIO5
5	GIO6	6	GIO38
7	GND	8	GND
9	COUT0	10	COUT1
11	COUT2	12	COUT3
13	COUT4	14	COUT5
15	COUT6	16	COUT7
17	GND	18	GND
19	VPBECLK/VID_CLK	20	HSYNC
21	GND	22	GND
23	VCLK	24	VSYNC
25	GND	26	GND
27	YOUT0	28	YOUT1
29	YOUT2	30	YOUT3
31	YOUT4	32	YOUT5
33	YOUT6	34	YOUT7
35	GND	36	GND
37	1.8V.I2C_CLK	38	1.8V.SYS_RESETz
39	1.8V.I2C_DATA	40	GND
41	VCC_1.8V	42	VCC_1.8V
43	GND	44	GND
45	VCC_3.3V	46	VCC_3.3V
47	GND	48	GND
49	VCC_5V	50	VCC_5V

3.7.6 DC6, SD Interface Connector

Table 35: DC6, SD Interface Connector

Pin #	Signal	Pin #	Signal
1	SD_CLK	2	SD_CMD
3	GND	4	GND
5	SD_DATA0	6	SD_DATA1
7	SD_DATA2	8	SD_DATA3
9	GND	10	GND

3.7.7 DC7, Power Connector

Table 36: DC7, Power Connector

Pin #	Signal	Pin #	Signal
1	VDDIMX_EN	2	GND
3	DSP_CORE_SUPPLY	4	DSP_CORE_SUPPLY
5	GND	6	GND
7	VCC_1.8V	8	VCC_1.8V
9	GND	10	GND

3.8 Test Points

The EVM has 63 test points. All test points appear on the top of the board. The following figure identifies the position of each test point. the next table list each test point and the signal appearing on that test point.

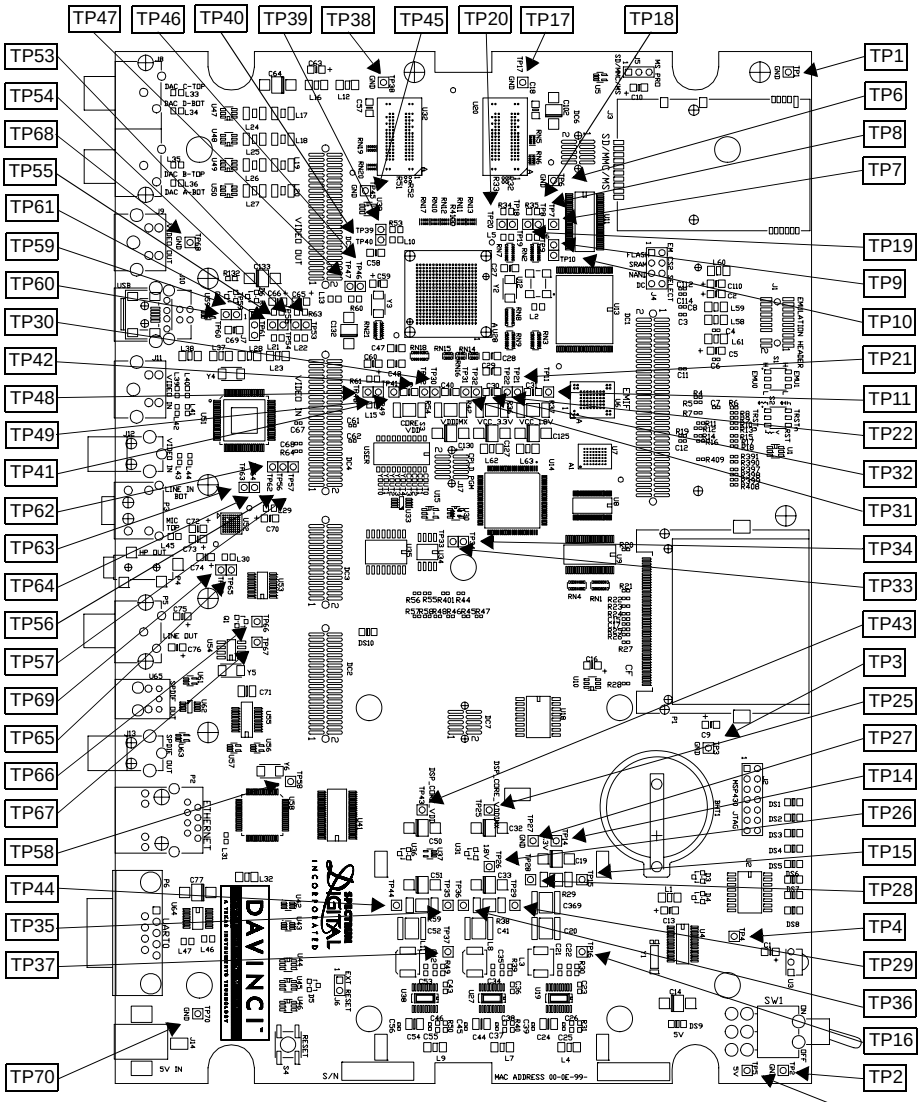

Figure 3-20, DM644x EVM, Test Points

Table 37: DM644x EVM Test Points

Test Point #	Signal	Schematic Page	Test Point #	Signal	Schematic Page
TP1	GND	4,34	TP36		
TP2	GND	34	TP37	U27,U38,PIN 4,VCC_3.3V	35
TP3	GND	34	TP38	GND	4
TP4	U4,P24,P1.3/TA2	28	TP39	U28A,DDR_VSS.DLLVCC_1.8V	4
TP5	VCC_5V	34	TP40	VCC_1.8V	4
TP6	GND	4	TP41	DSP_CORE_VDD	9
TP7	U28A,DDR_AMUX.DLL		TP42	U28D,VDD.10 DSP_CORE_VDD	9
TP8	U28E,PLLPWR18 VCC_1.8V	8	TP43	DSP_CORE_VDD	35
TP9	GND	8	TP44		
TP10	U28E,AMUX	8	TP45	GND	
TP11	U28D,VDDS1.14 VCC_1.8V	9	TP46	U28H, USB_VDDA1P8PHY VCC_1.8V	7
TP14	+3.3V	34	TP47	VCC_1.8V	7
TP15			TP48	VCC_3.3V	7
TP16	3V3_PWR_OK	34	TP49	U28H, USB_VDDA3P3PHY VCC_3.3V	7
TP17	GND	4	TP53	VCC_1.8V	5
TP18	U28E,APLLREFV DSP_CORE_VDD	8	TP54	U28G,VDDA18V VCC_1.8V	5
TP19	VCC_1.8V	8	TP55	U28G,VDDA11 DSP_CORE_VDD	5
TP20	DSP_CORE_VDD	8	TP56	U51,Pin 36	24
TP21	VCC_1.8V	9	TP57	U51,Pin 37	24
TP22	U28D,VDDSHV.4 VCC_3.3V	9	TP58	U58,PIN 64,MDINT	22
TP25	DSP_CORE_VDDIMX	35	TP59		
TP26	VCC_1.8V	35	TP60		
TP27	GND	34	TP61	DSP_CORE_VDD	5
TP28	JP1,Pin 28, ATA_CSEL	18	TP62	U51,Pin 30	24
TP29			TP63	U52,A8,MPF2	26
TP30	U28D,VDDIMX.11 DSP_CORE_VDDIMX	9	TP64	U52,A9,MPF3	26
TP31	DSP_CORE_VDDIMX	9	TP65	U52,C8,SCL	26
TP32	VCC_3.3V	9	TP66	U28I,GIO45/PWM0 VCC_1.8V	5
TP33	JP1, Pin 34	18	TP67	VIN, U54,PIN 3	5
TP34			TP68	GND	34
TP35			TP69	U52,J9,GPIO1	26
			TP70	GND	34

Appendix A

Schematics

This appendix contains the schematics for the DaVinci EVM.

NOTES, UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES IN OHMS.

2. CAPACITANCE VALUES IN MICROFARADS.

3. REFERENCE DESIGNATORS USED:

4. ALL 0.1 uF AND 0.01uF CAPACITORS ARE DECOUPLING CAPS UNLESS OTHERWISE NOTED. THEY ARE SHOWN ON THE PAGE WITH THE INTEGRATED CIRCUITS THEY SHOULD BE PLACED NEAR.

5. OBSERVE THE FOLLOWING LAYOUT NOTES:

6. BOARD PROPERTIES

A. ROUTE TO WITHIN 10% OF MANHATTAN DISTANCE
B1. General layers 50 +/- 5 OHM MATCHED IMPEDANCE
B2. USB layer 90 ohm differential

C. OUTER LAYERS 0.5 OZ CU /W 0.5 OZ AU PLATING
D. INNER LAYERS 1.0 OZ CU
E. FR4 BOARD MATERIAL
F. MINIMUM TRACE WIDTH/SPACING 4 MILS
G. MINIMUM VIA SIZE 10/19 MIL
H. LAYER STACKUP:

1. TOP - SIGNAL ROUTING
2. GROUND PLANE
3. INNER1 - SIGNAL ROUTING
4. VCC3 PLANE (3.3V BOARD)
5. INNER2 - SIGNAL ROUTING
6. INNER3 - SIGNAL ROUTING
7. VCC PLANE 2
8. INNER4 - SIGNAL ROUTING
9. GROUND PLANE
10. BOTTOM - SIGNAL ROUTING

REV	DESCRIPTION	DATE	APPROVED
A	Initial schematic ready for layout - Alpha Release	02/17/05	RRP
B	Beta Release	09/27/05	RRP
C	Gamma Release	10/28/05	RRP
D	Production Release	02/18/06	RRP

SCHEMATIC CONTENTS

BASE	I2C ADDRESS TABLE	SHEET
0x50	I2C ROM	6
0x1B	AIC33	26
0x5D	TVP5146	24
0x38	IO EXPANDER 0 (LED)	28
0x39	IO EXPANDER 1 (PLL/USER_SW)	28
0x3A	IO EXPANDER 2 (USB/CD_RESET)	28
0x23	MSP430	28

REVISION STATUS OF SHEETS

	A	A	D	A	D						
	31	32	33	34	35						
REV	B	B	A	A	A	A	A	A	A	A	
SH	21	22	23	24	25	26	27	28	29	30	
REV	A	A	A	D	B	A	B	B	B	A	
SH	11	12	13	14	15	16	17	18	19	20	
REV	D	A	B	A	B	A	B	B	A	A	NEXT ASSY USED ON
SH	1	2	3	4	5	6	7	8	9	10	APPLICATION

DWN	R.R.P.	DATE 02/17/2005
CHK	T.W.K.	DATE 02/17/2005
ENGR	R.R.P.	DATE 02/17/2005
ENGR-MGR	R.R.P.	DATE 02/17/2005
QA	C.M.D.	DATE 03/01/2004
MFG	R.R.P.	DATE 02/17/2005
RLSE	R.R.P.	DATE 02/17/2005

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Title: DAVINCI EVALUATION MODULE

Page Contents: Title Block

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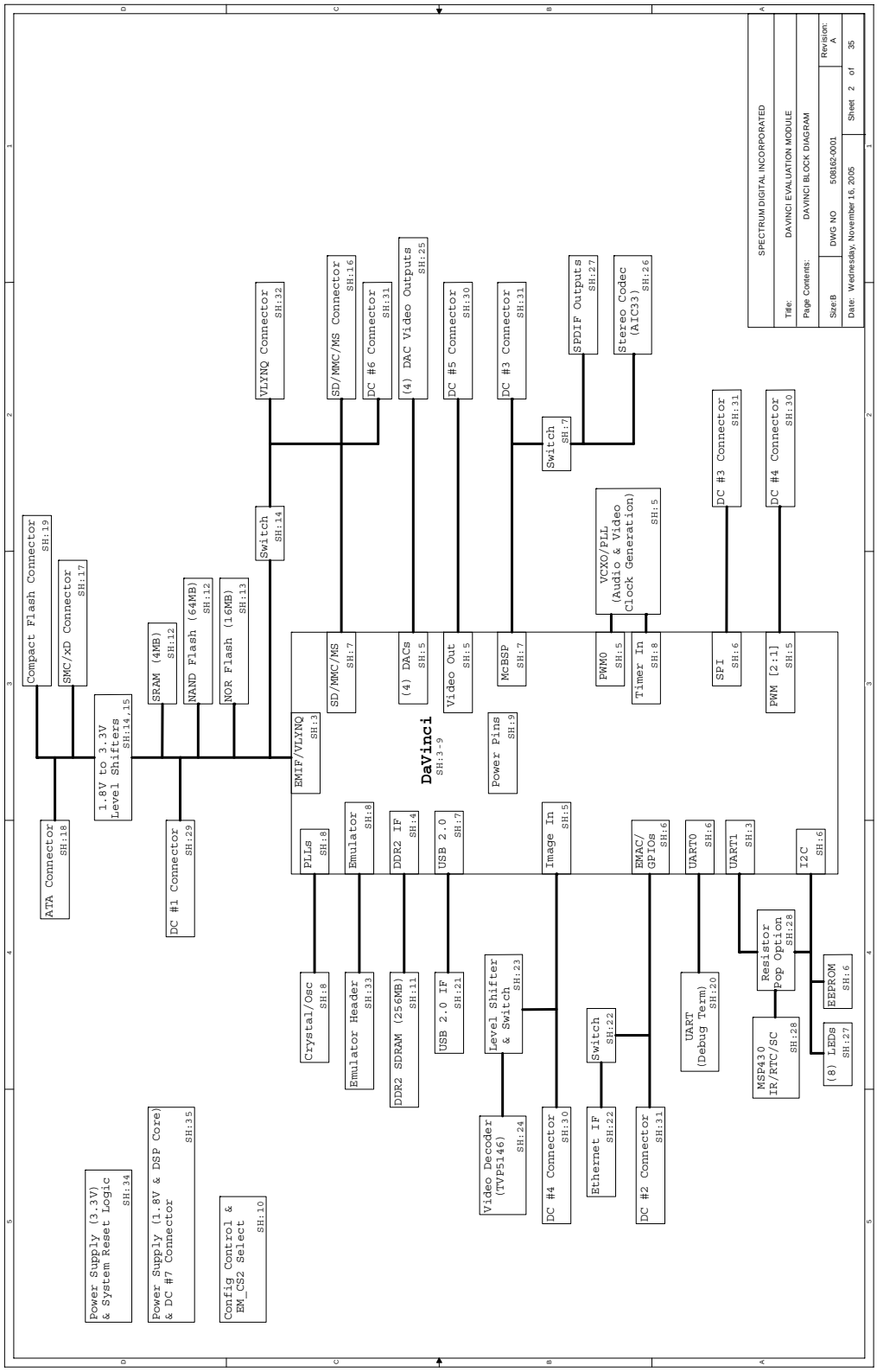
DaVinci
SH:3-9
EMIF/VLYNQ SH:3
PLLs SH:8
Emulator SH:8
DDR2 IF SH:4
USB 2.0 SH:7
Image In SH:5
EMAC/ GPIOs SH:6
UART0 SH:6
UART1 SH:3
I2C SH:6
SD/MMC/MS SH:7
(4) DACs SH:5
Video Out SH:5
McBSP SH:7
Power Pins SH:9
PWM0 SH:5
Timer In SH:8
VCXO/PLL (Audio & Video Clock Generation) SH:5
SPI SH:6
PWM [2:1] SH:5
Compact Flash Connector SH:19
SMC/xD Connector SH:17
1.8V to 3.3V Level Shifters SH:14,15
SRAM (4MB) SH:12
NAND Flash (64MB) SH:12
NOR Flash (16MB) SH:13
Switch SH:14
VLYNQ Connector SH:32
SD/MMC/MS Connector SH:16
DC #6 Connector SH:31
(4) DAC Video Outputs SH:25
DC #5 Connector SH:30
DC #3 Connector SH:31
Switch SH:7
SPDIF Outputs SH:27
Stereo Codec (AIC33) SH:26
DC #3 Connector SH:31
DC #4 Connector SH:30
ATA Connector SH:18
DC #1 Connector SH:29
Crystal/Osc SH:8
Emulator Header SH:33
DDR2 SDRAM (256MB) SH:11
USB 2.0 IF SH:21
Level Shifter & Switch SH:23
Video Decoder (TVP5146) SH:24
DC #4 Connector SH:30
Switch SH:22
Ethernet IF SH:22
DC #2 Connector SH:31
UART (Debug Term) SH:20
Resistor Pop Option SH:28
MSP430 IR/RTC/SC SH:28
EEPROM SH:6
(8) LEDs SH:27
Power Supply (3.3V) & System Reset Logic SH:34
Power Supply (1.8V & DSP Core) & DC #7 Connector SH:35
Config Control & EM_CS2 Select SH:10
SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: DAVINCI BLOCK DIAGRAM
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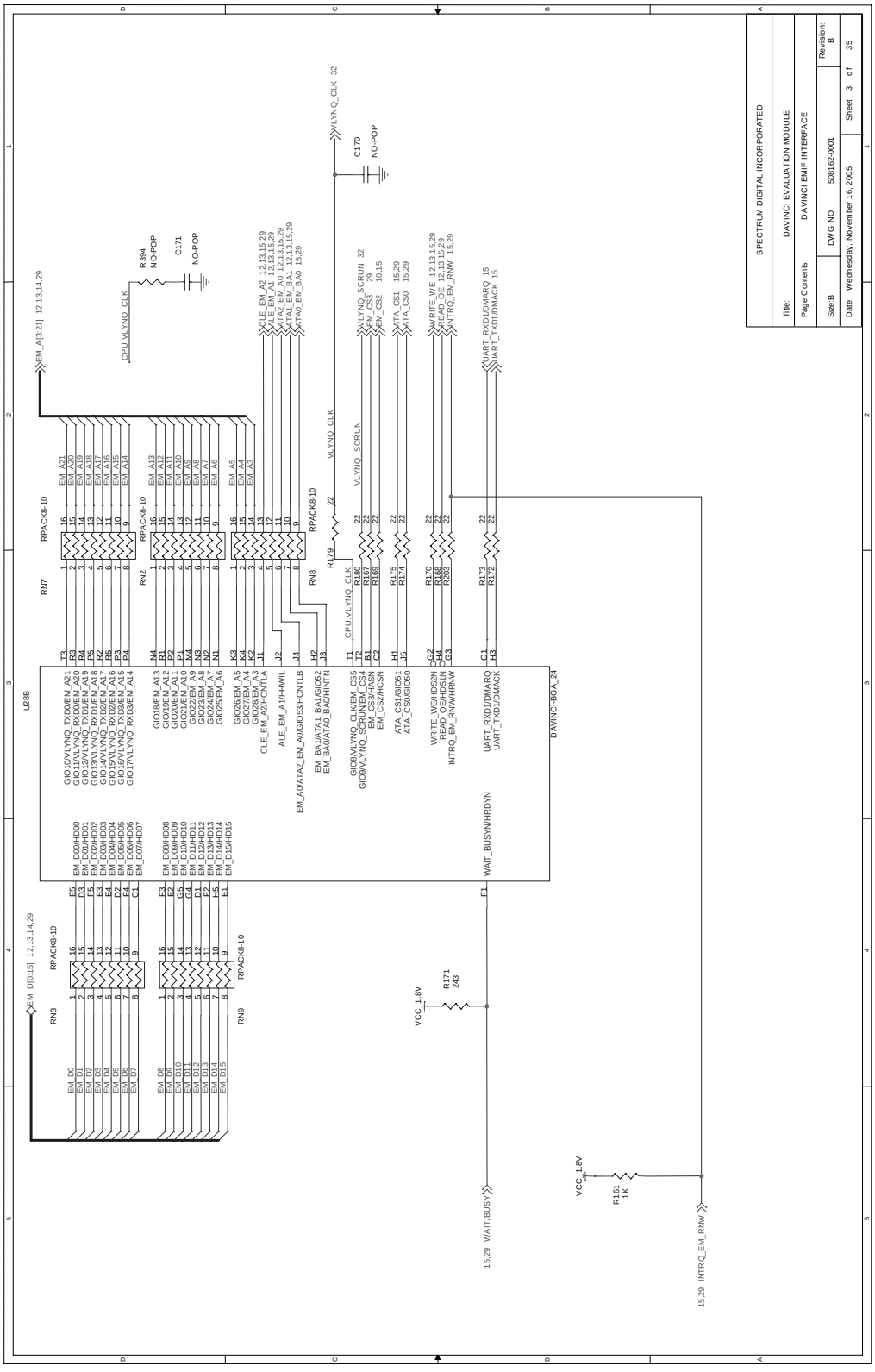
SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: DAVINCI EMIF INTERFACE
Size: B
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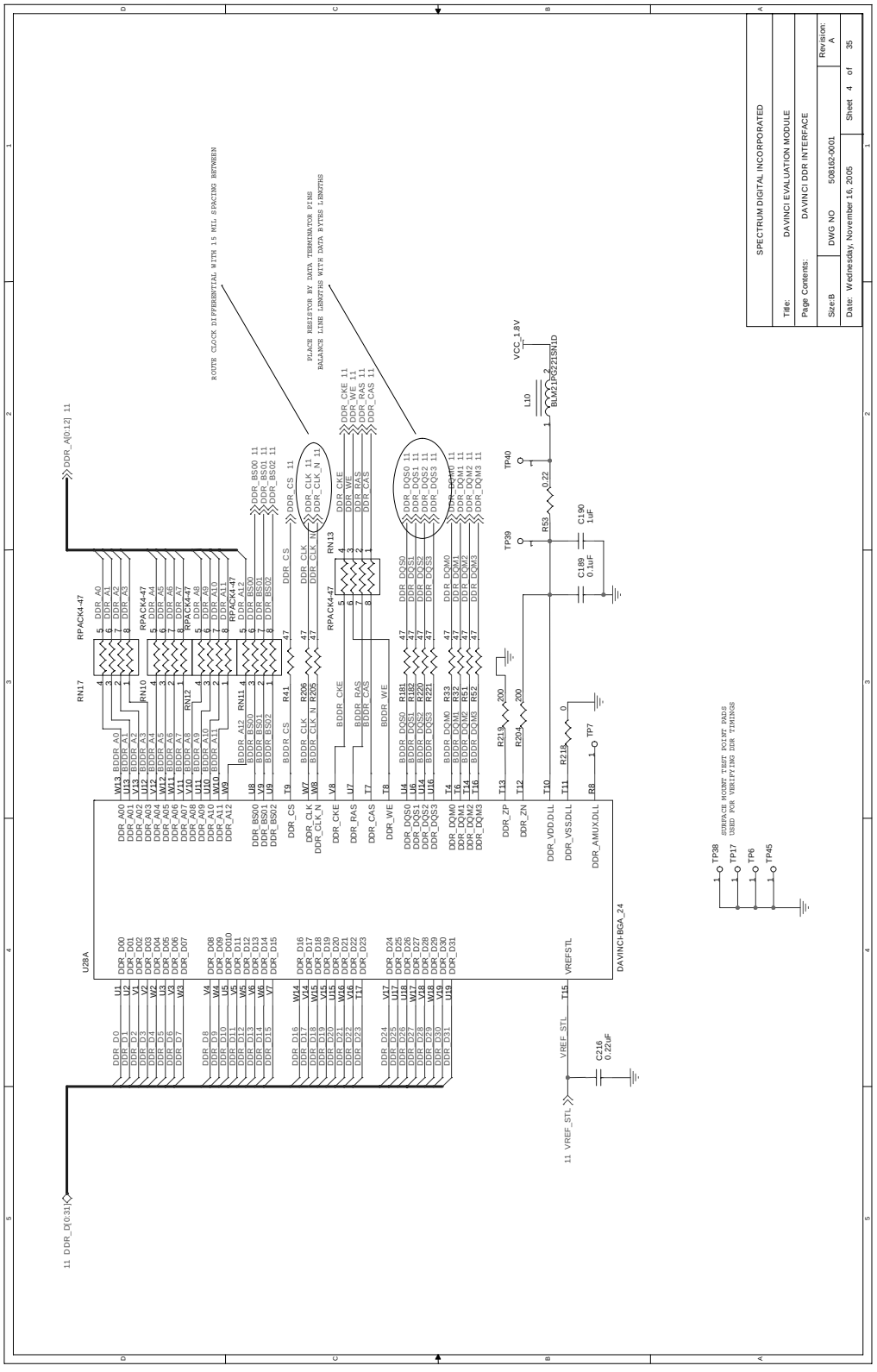
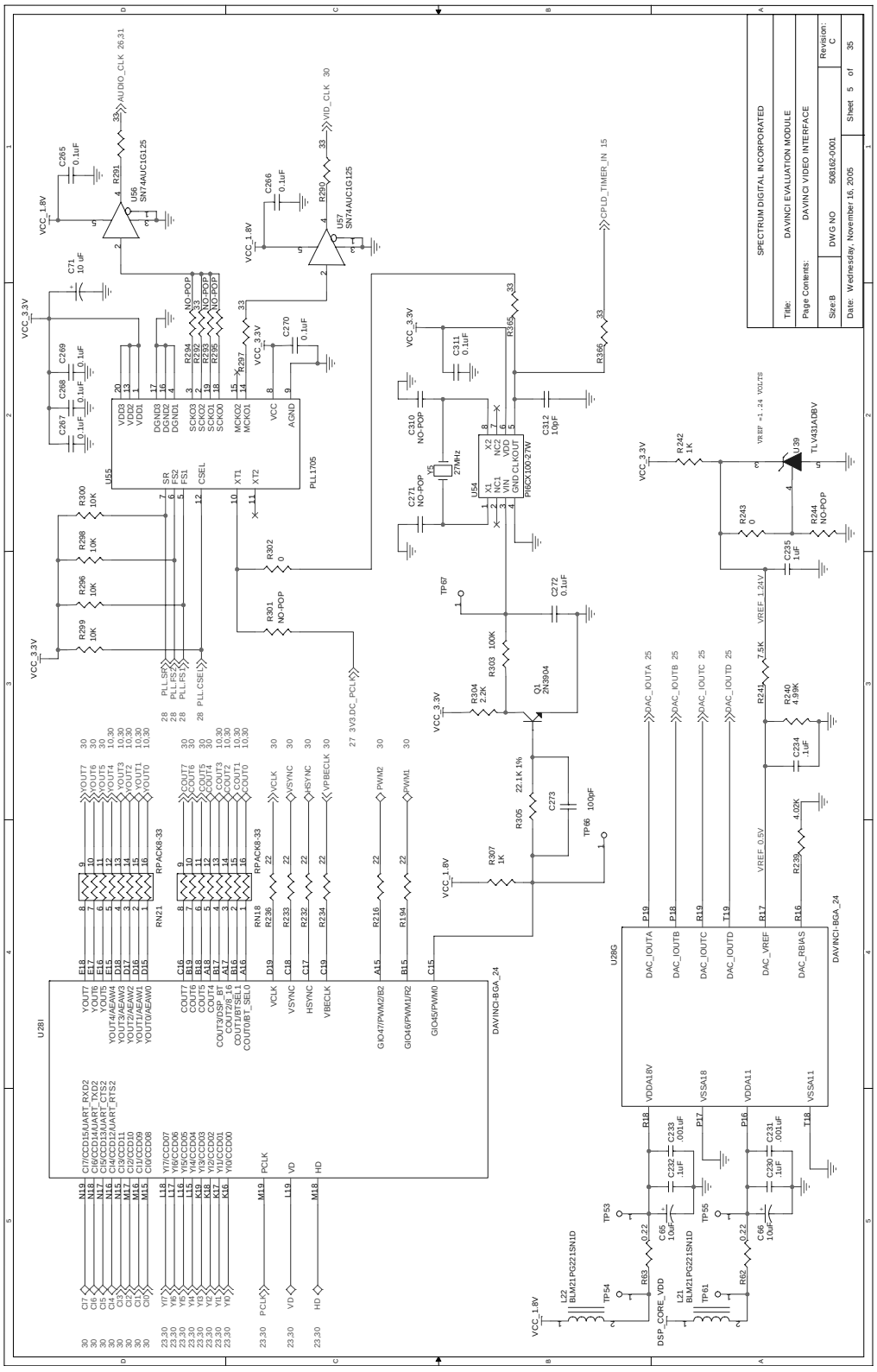
U28B
DAVINCI-BGA_24
RN3
RN7
RN2
RN8
RN9
RPACK8-10
EM_A[3:21] 12,13,14,29
EM_D[0:15] 12,13,14,29
CPU.VLYNQ_CLK
VLYNQ_CLK 32
VLYNQ_SCRUN
C170
C171
R394
NO-POP
R179
22
R171
243
R161
1K
VCC_1.8V
WAIT_BUSY/NHRDYN
UART_RXD1/DMARQ
UART_TXD1/DMACK
WRITE_WE/HDSIN
READ_OE/HDSIN
INTRQ_EM_RNW/HRNW
ATA_CS1/GIO51
ATA_CS0/GIO50
CLE_EM_A2/HCNTLA
ALE_EM_A1/HHWIL
EM_A0/ATA2_EM_A0/GIO53/HCNTLB
EM_BA1/ATA1_BA1/GIO52
EM_BA0/ATA0_BA0/HINTN
GIO8/VLYNQ_CLK/EM_CS5
GIO9/VLYNQ_SCRUN/EM_CS4
EM_CS3/HCSN
EM_CS2/HCSN
15,29 WAIT/BUSY
15,29 INTRQ_EM_RNW


SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: DAVINCI DDR INTERFACE
Size:B DWG NO 508162-0001 Revision: A
Date: Wednesday, November 16, 2005 Sheet 4 of 35
DDR_A[0:12] 11
DDR_D[0:31] 11
11 VREF_STL
RPACK4-47
RN17
RN10
RN12
RN11
RN13
DAVINCI-BGA_24
U28A
DDR_A0
DDR_A1
DDR_A2
DDR_A3
DDR_A4
DDR_A5
DDR_A6
DDR_A7
DDR_A8
DDR_A9
DDR_A10
DDR_A11
DDR_A12
DDR_BS0
DDR_BS1
DDR_BS2
DDR_CS
DDR_CLK
DDR_CLK_N
DDR_CKE
DDR_RAS
DDR_CAS
DDR_WE
DDR_DQS0
DDR_DQS1
DDR_DQS2
DDR_DQS3
DDR_DQM0
DDR_DQM1
DDR_DQM2
DDR_DQM3
DDR_ZP
DDR_ZN
DDR_VDD.DLL
DDR_VSS.DLL
DDR_AMUX.DLL
VREFSTL
R41
R206
R205
R181
R182
R220
R221
R53
R213
R204
R218
R219
R32
R51
R52
R33
C189 0.1uF
C190 1uF
C216 0.22uF
L10
VCC_1.8V
TP39
TP40
TP7
TP38
TP17
TP6
TP45
ROUTE CLOCK DIFFERENTIAL WITH 15 MIL SPACING BETWEEN
PLACE RESISTOR BY DATA TERMINATOR PINS
BALANCE LINE LENGTHS WITH DATA BYTES LENGTHS
STRIP8-CE MOUNT TEST POINT PADS
USED FOR VERIFYING DDR TIMINGS


SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
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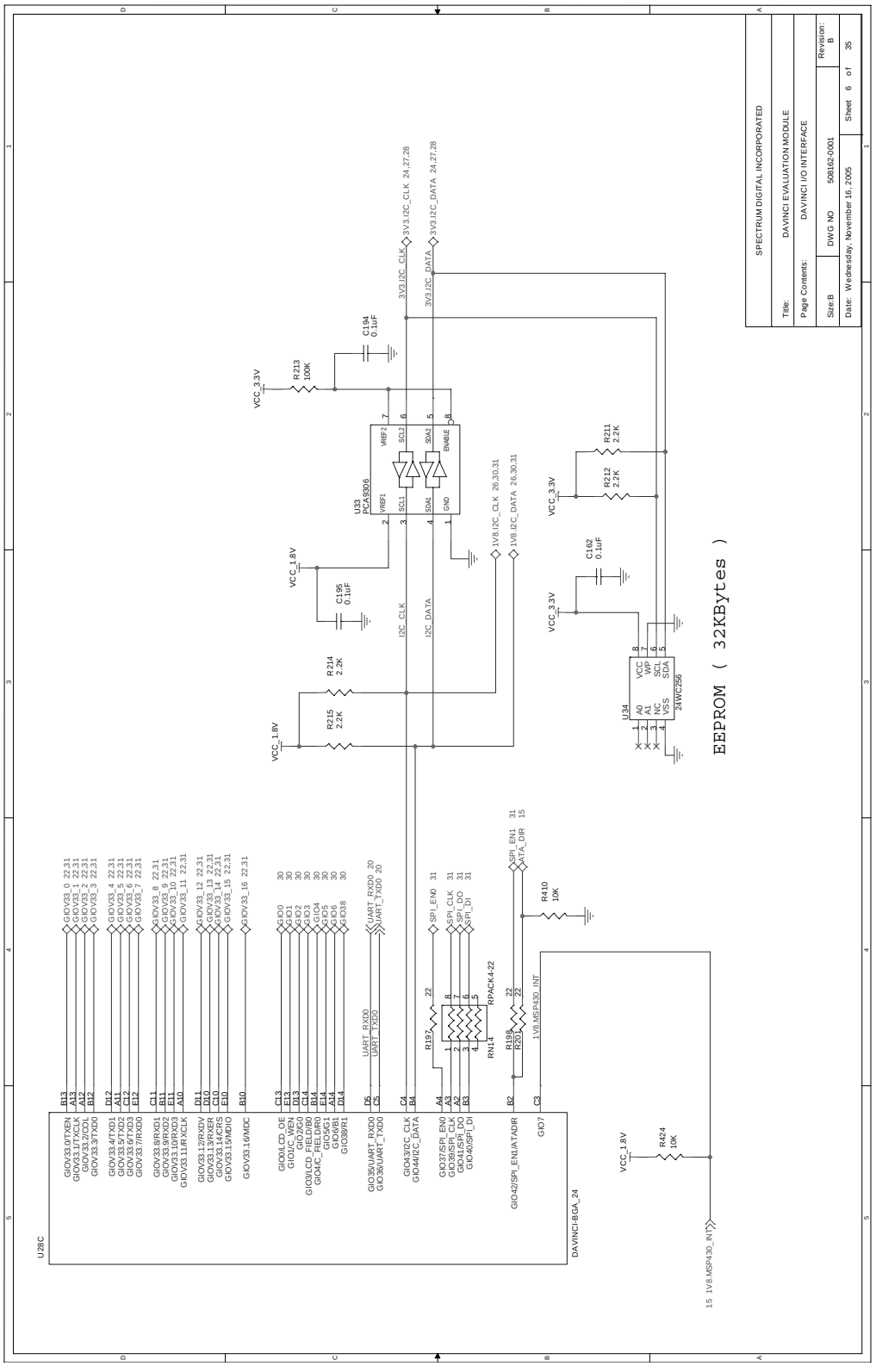
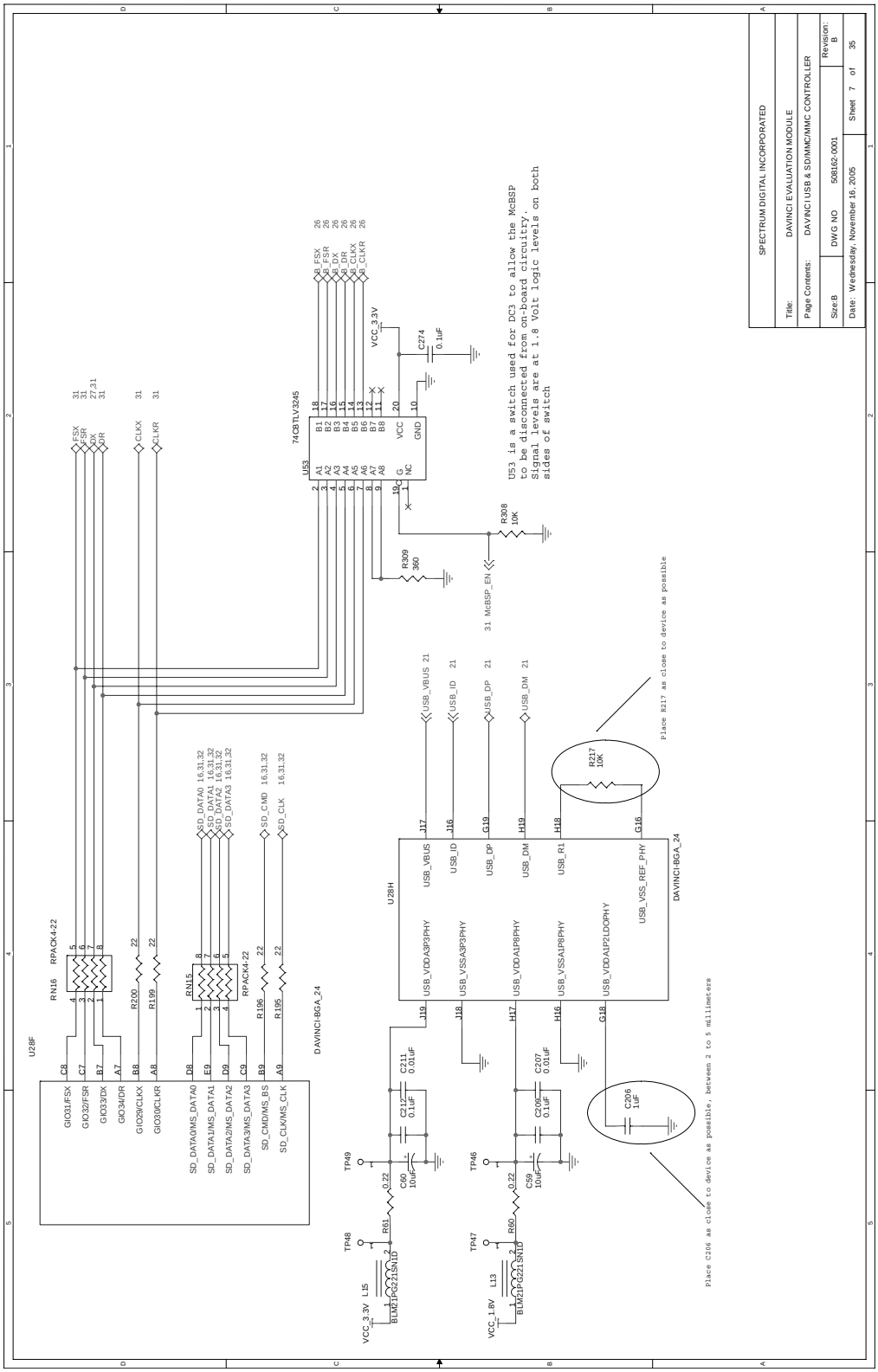
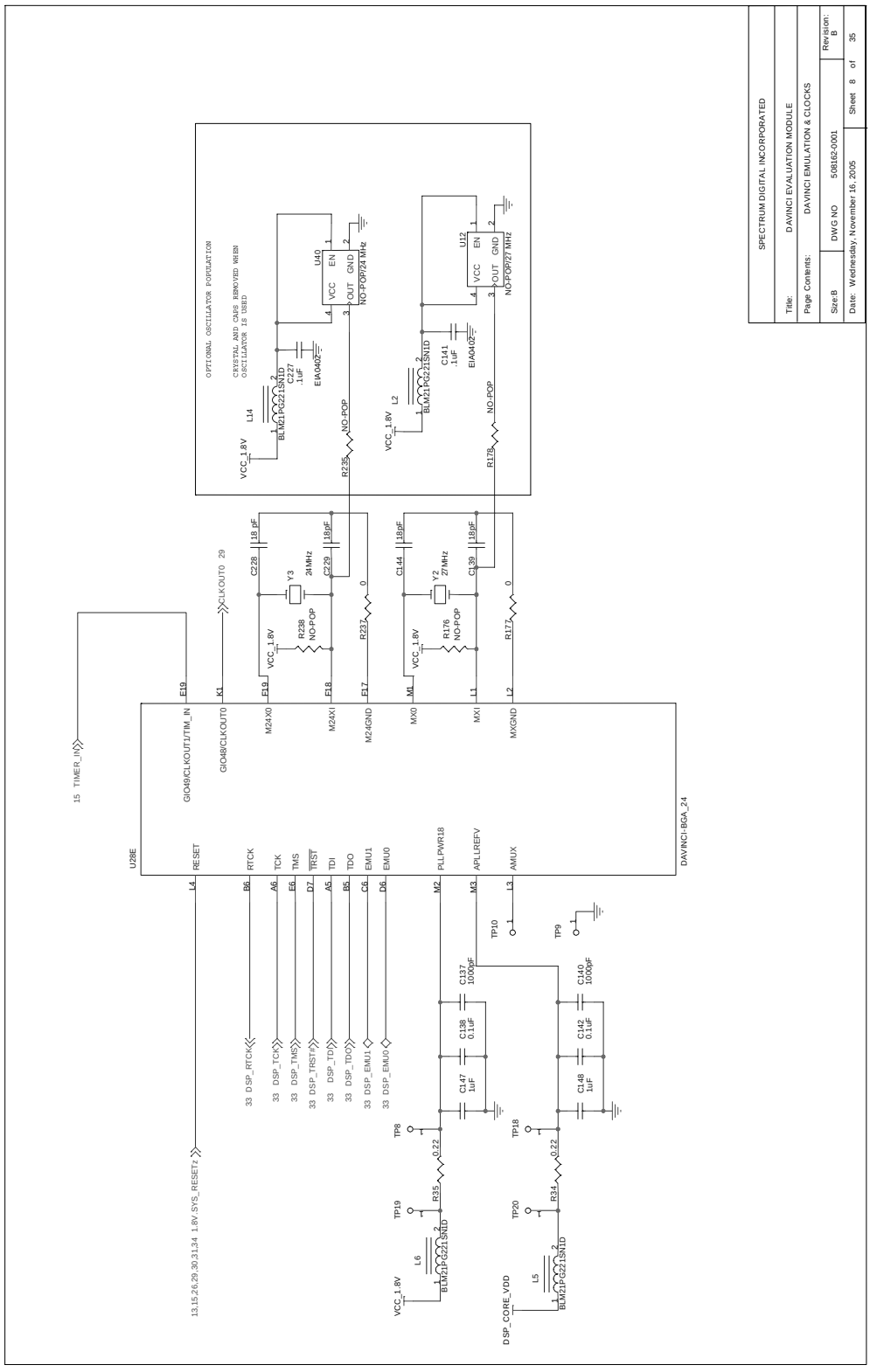
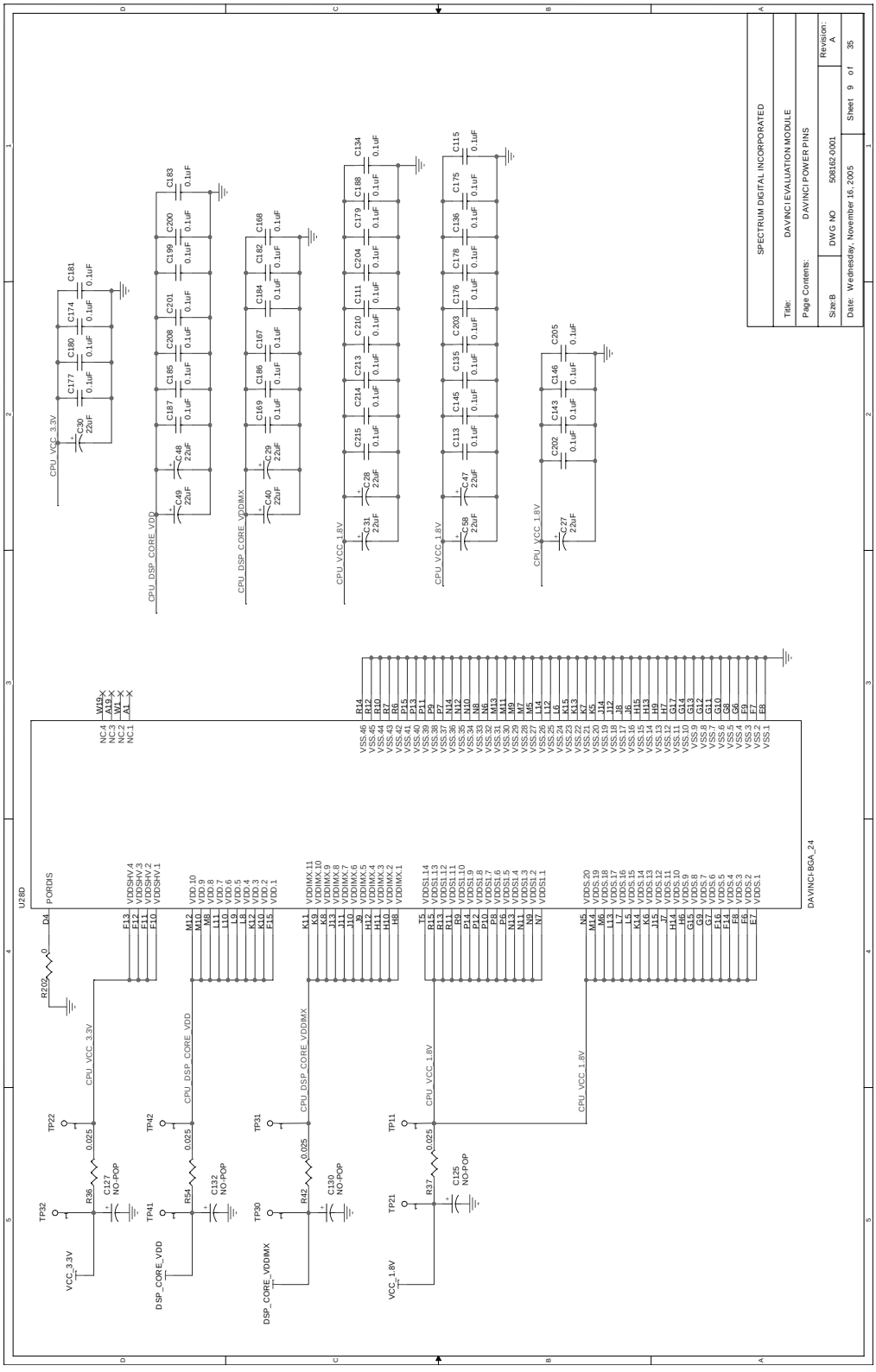
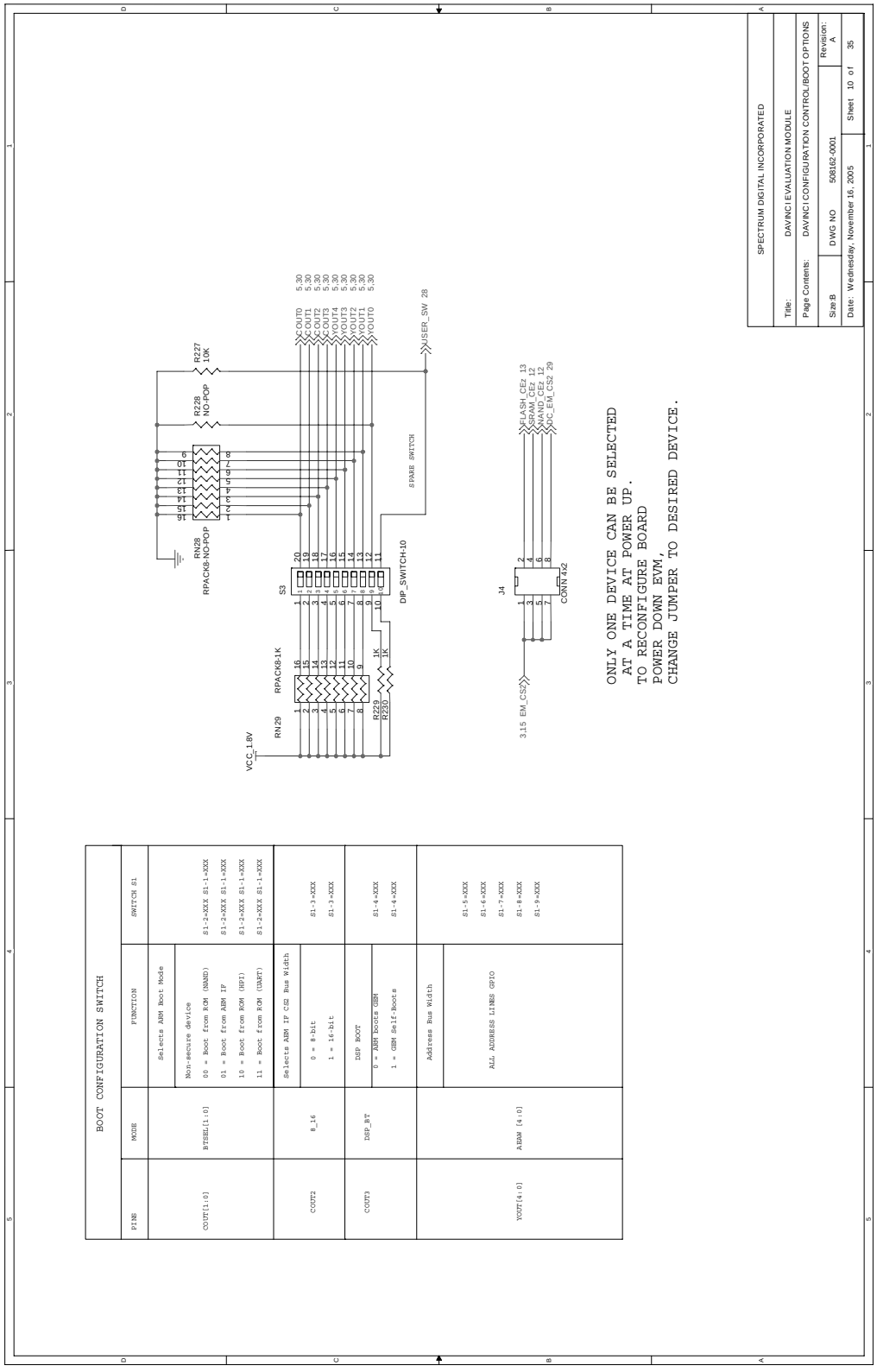
U28I
DAVINCI-BGA_24
U28G
DAVINCI-BGA_24
U55
PLL1705
U54
PBSCA100-27W
U56
SN74AUC1G125
U57
SN74AUC1G125
U39
TLV431ADBV
RN21
RPACK8-33
RN18
RPACK8-33
Q1
2N3904
L22
BLM21PG221SN1D
L21
BLM21PG221SN1D
VCC_3.3V
VCC_1.8V
DSP_CORE_VDD
AUDIO_CLK 28,31
VID_CLK 30
CPLD_TIMER_IN 15
PLL_SR
PLL_FS2
PLL_FS1
PLL_CSEL
3V3_DC_PCLK
VCLK
VSYNC
HSYNC
VBECLK
PCLK
VD
HD
PWM2
PWM1
VREF_1.24V
VREF_0.5V
DAC_IOUTA 25
DAC_IOUTB 25
DAC_IOUTC 25
DAC_IOUTD 25

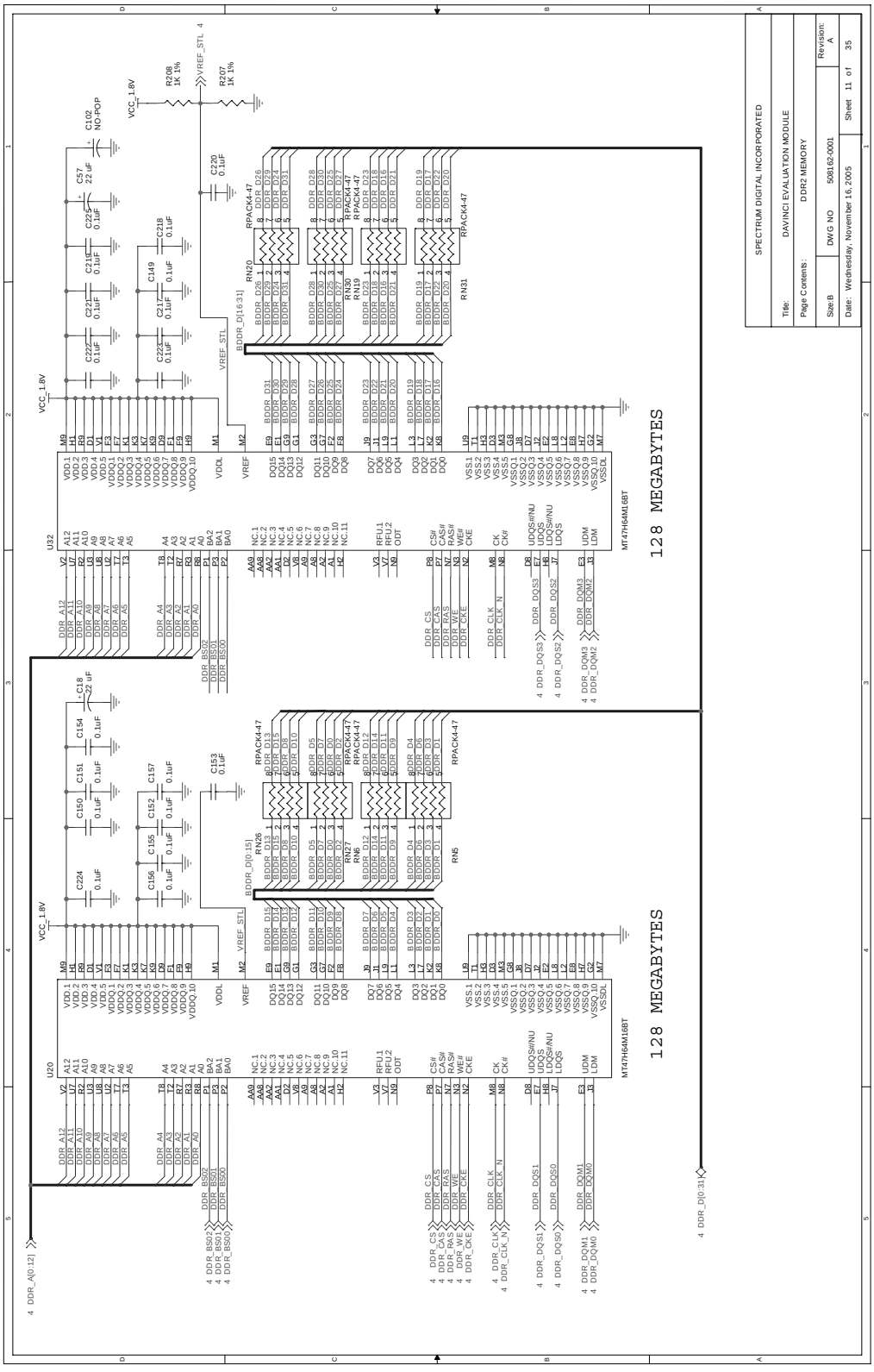

SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: DAVINCI I/O INTERFACE
Size:B DWG NO 508162-0001 Revision: B
Date: Wednesday, November 16, 2005 Sheet 6 of 35
EEPROM (32KBytes)
U28C
DAVINCI-BGA_24
U33 PCA9306
U34 24WC256
VCC_3.3V
VCC_1.8V
R213 100K
R214 2.2K
R215 2.2K
R211 2.2K
R212 2.2K
R410 10K
R424 10K
C194 0.1uF
C195 0.1uF
C162 0.1uF
RPACK4-22
RN14
R197 22
R198 22
R200 22
3V3.I2C_CLK 24,27,28
3V3.I2C_DATA 24,27,28
1V8.I2C_CLK 26,30,31
1V8.I2C_DATA 26,30,31
I2C_CLK
I2C_DATA
UART_RXD0
UART_TXD0
SPI_EN0
SPI_CLK
SPI_DO
SPI_DI
SPI_EN1
ATA_DIR
1V8.MSP430_INT
1.5 1V8.MSP430_INT

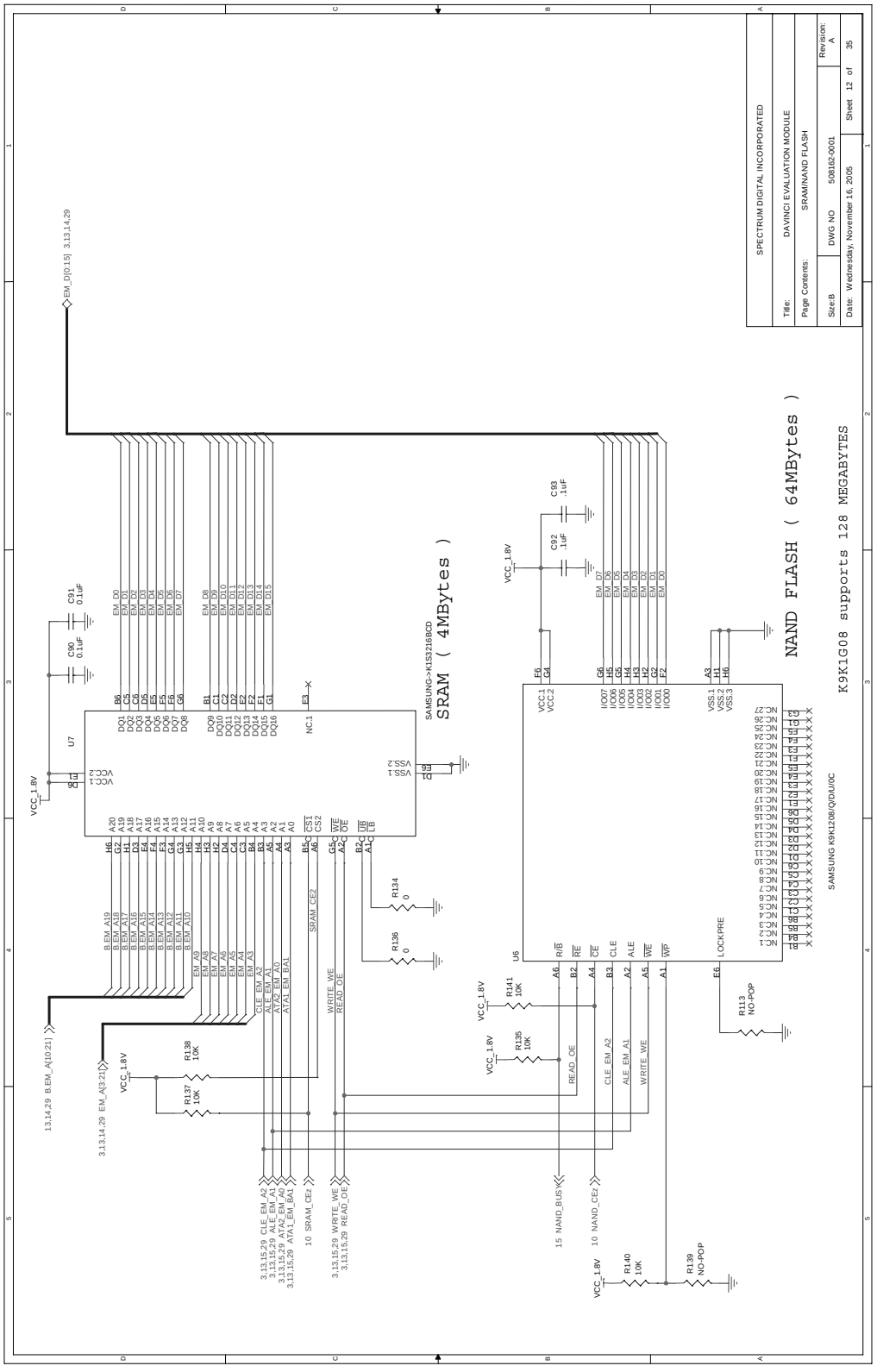

SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: DAVINCI USB & SD/MMC/NMC CONTROLLER
Size:B
DWG NO 508102-0001
Revision: B
Date: Wednesday, November 16, 2005
Sheet 7 of 35
U53 is a switch used for DC3 to allow the McBSP to be disconnected from on-board circuitry. Signal levels are at 1.8 Volt logic levels on both sides of switch
74CBTLV3245
U28F
U28H
DAVINCI-BGA_24
RPACK4-22
RN16
RN15
R200
R199
R196
R195
R308 10K
R309 360
R217 10K
C274 0.1uF
C211 0.01uF
C212 0.1uF
C60 10uF
C207 0.01uF
C208 0.1uF
C59 10uF
C206 1uF
R61 0.22
R60 0.22
L15 BLM21PG221SN1D
L13 BLM21PG221SN1D
TP49
TP48
TP46
TP47
VCC_3.3V
VCC_1.8V
Place R217 as close to device as possible
Place C206 as close to device as possible, between 2 to 5 millimeters

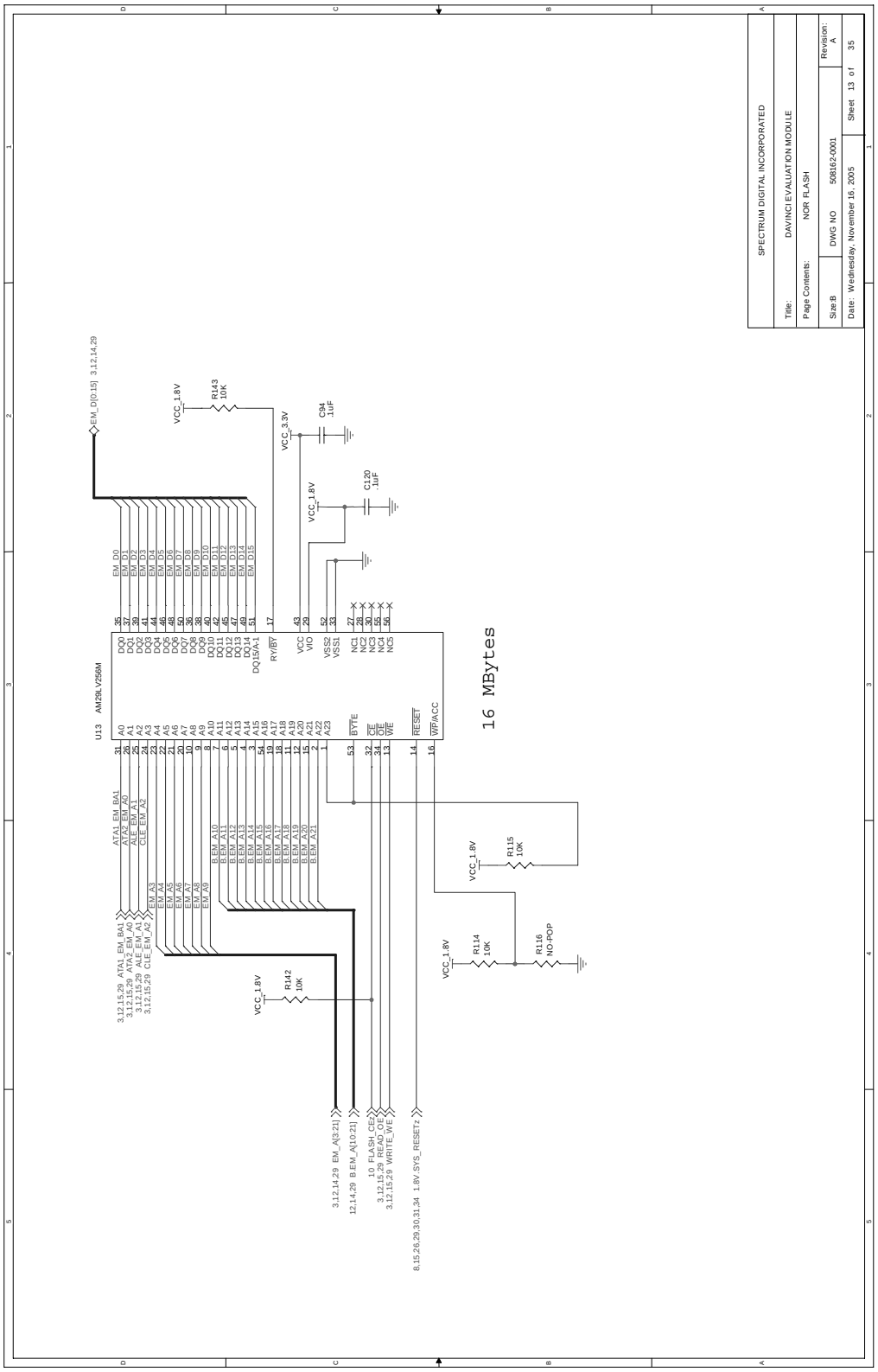

SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: DAVINCI EMULATION & CLOCKS
Size:B DWG NO 508162-0001 Revision: B
Date: Wednesday, November 16, 2005 Sheet 8 of 35
OPTIONAL OSCILLATOR POPULATION
CRYSTAL AND CASE REMOVED WHEN OSCILLATOR IS USED
U28E
DAVINCI-BGA_24
GIO49/CLKOUT1/TIM_IN
GIO48/CLKOUT0
RESET
RTCK
TCK
TMS
TRST
TDI
TDO
EMU1
EMU0
PLLPWR18
APLLREFV
AMUX
M24X0
M24XI
M24GND
MX0
MXI
MXGND
CLKOUT0 29
15 TIMER_IN
13,15,26,29,30,31,34 1.8V_SYS_RESETz
33 DSP_RTCK
33 DSP_TCK
33 DSP_TMS
33 DSP_TRSTz
33 DSP_TDI
33 DSP_TDO
33 DSP_EMU1
33 DSP_EMU0
C228 18 pF
C229 18pF
Y3 24MHz
R238 NO-POP
R237 0
C144 18pF
C139 18pF
Y2 27MHz
R176 NO-POP
R177 0
L14 BLM21PG221SN1D
C227 .1uF EIA0402
U40 VCC EN GND OUT NO-POP/24 MHz
R235 NO-POP
L2 BLM21PG221SN1D
C141 .1uF EIA0402
U12 VCC EN GND OUT NO-POP/27 MHz
R178 NO-POP
VCC_1.8V
C137 1000pF
C138 0.1uF
C147 1uF
C140 1000pF
C142 0.1uF
C148 1uF
TP8
TP9
TP10
TP18
TP19
TP20
R35 0.22
R34 0.22
L6 BLM21PG221SN1D
L5 BLM21PG221SN1D
DSP_CORE_VDD

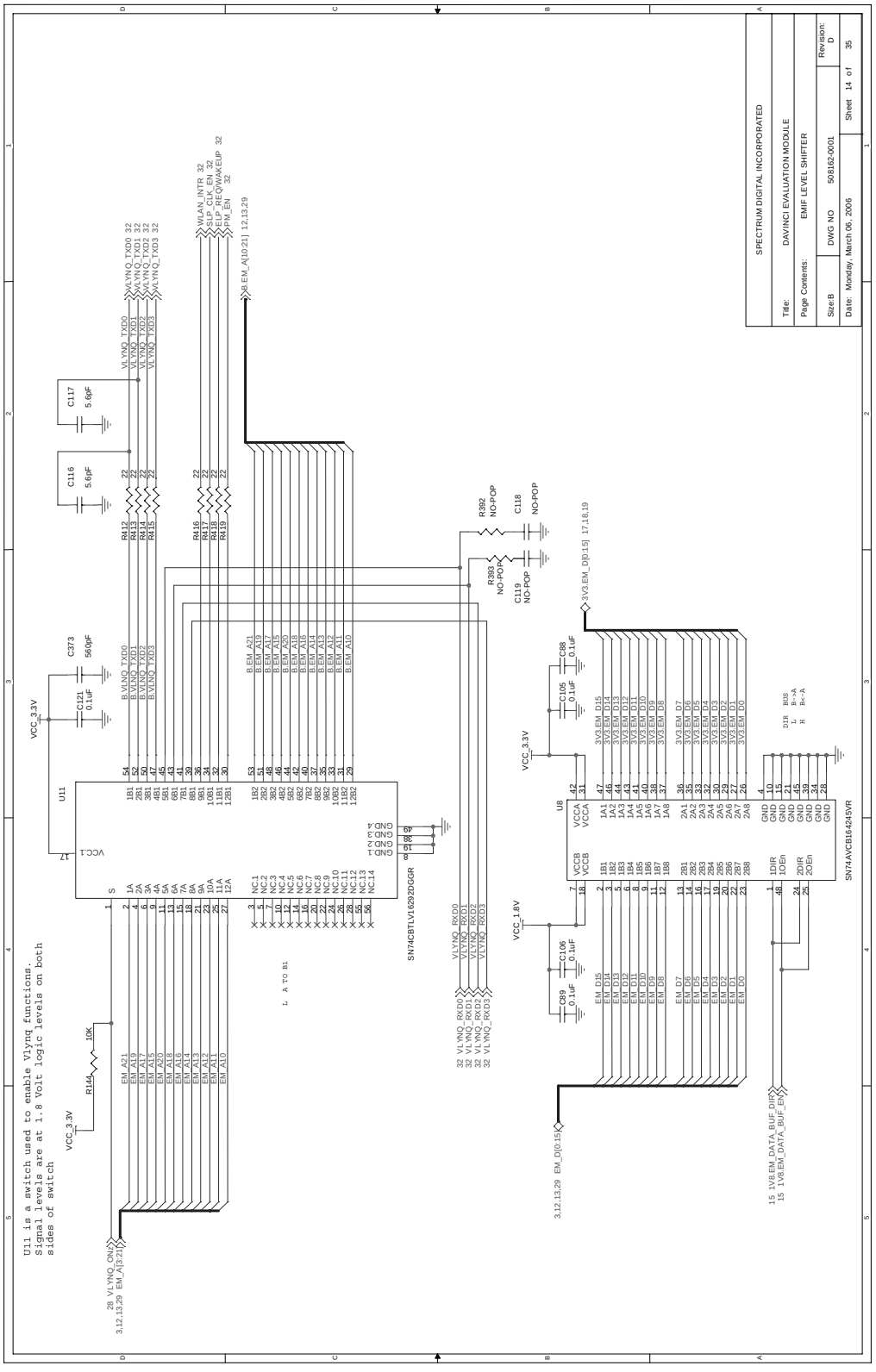

SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: DAVINCI POWER PINS
Size: B
DWG NO 508162-0001
Revision: A
Date: Wednesday, November 16, 2005
Sheet 9 of 35
U28D
DAVINCI-BGA_24
CPU_VCC_3.3V
CPU_DSP_CORE_VDD
CPU_DSP_CORE_VDDMX
CPU_VCC_1.8V
VCC_3.3V
DSP_CORE_VDD
DSP_CORE_VDDMX
VCC_1.8V

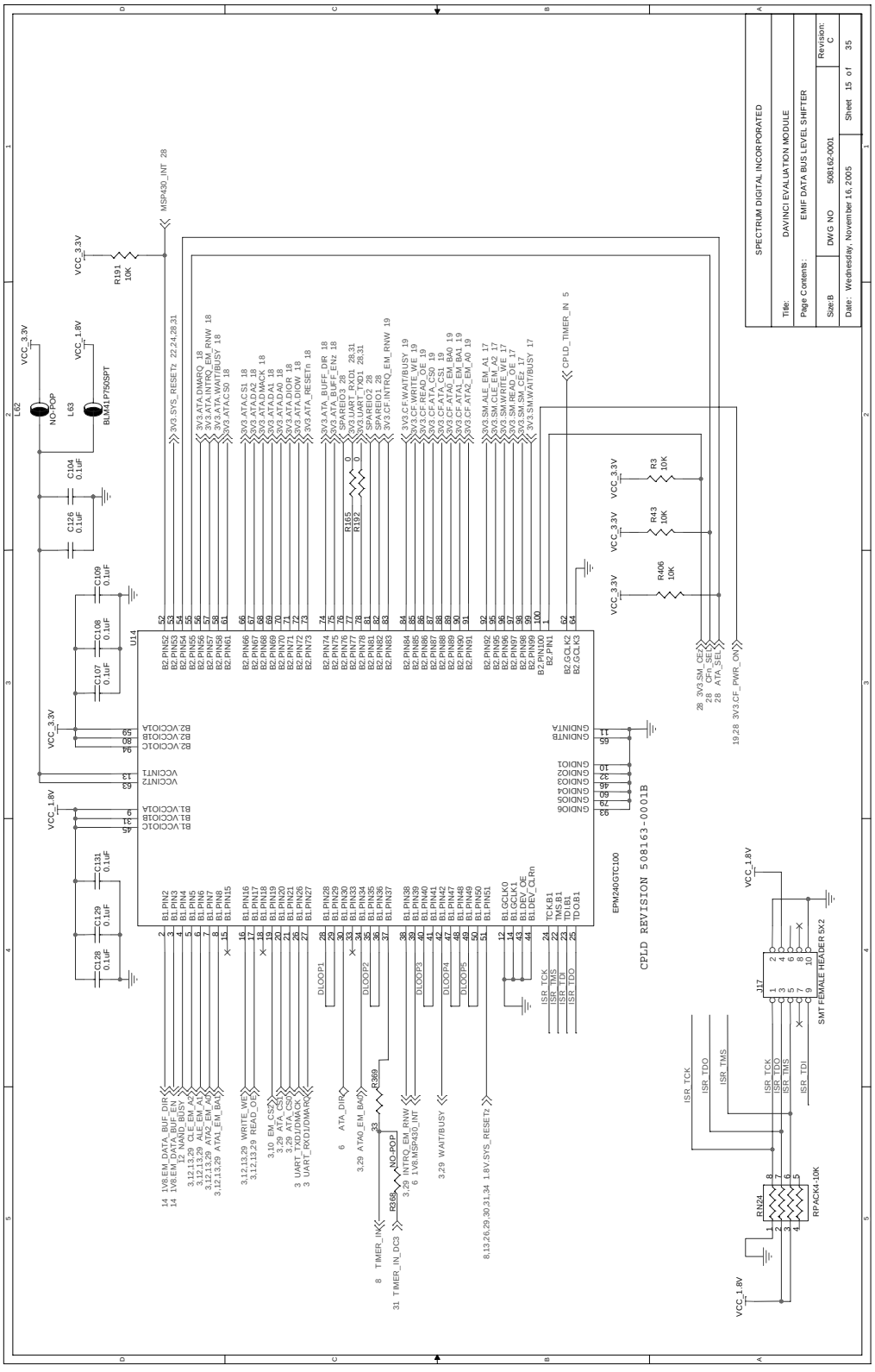

BOOT CONFIGURATION SWITCH
PINS
MODE
FUNCTION
SWITCH S1
COUT[1:0]
BTSEL[1:0]
Selects ARM Boot Mode
Non-secure device
00 = Boot from ROM (NAND)
01 = Boot from ARM IP
10 = Boot from ROM (HPI)
11 = Boot from ROM (UART)
S1-2=XXX S1-1=XXX
COUT2
8_16
Selects ARM IP CS2 Bus Width
0 = 8-bit
1 = 16-bit
S1-3=XXX
COUT3
DSP_BT
DSP BOOT
0 = ARM boots GBM
1 = GBM Self-Boots
S1-4=XXX
YOUT[4:0]
AEAW [4:0]
Addresss Bus Width
ALL ADDRESS LINES GPIO
S1-5=XXX
S1-6=XXX
S1-7=XXX
S1-8=XXX
S1-9=XXX
ONLY ONE DEVICE CAN BE SELECTED
AT A TIME AT POWER UP.
TO RECONFIGURE BOARD
POWER DOWN EVM,
CHANGE JUMPER TO DESIRED DEVICE.
SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: DAVINCI CONFIGURATION CONTROL/BOOT OPTIONS
Size:B
DWG NO 508162-0001
Revision: A
Date: Wednesday, November 16, 2005
Sheet 10 of 35

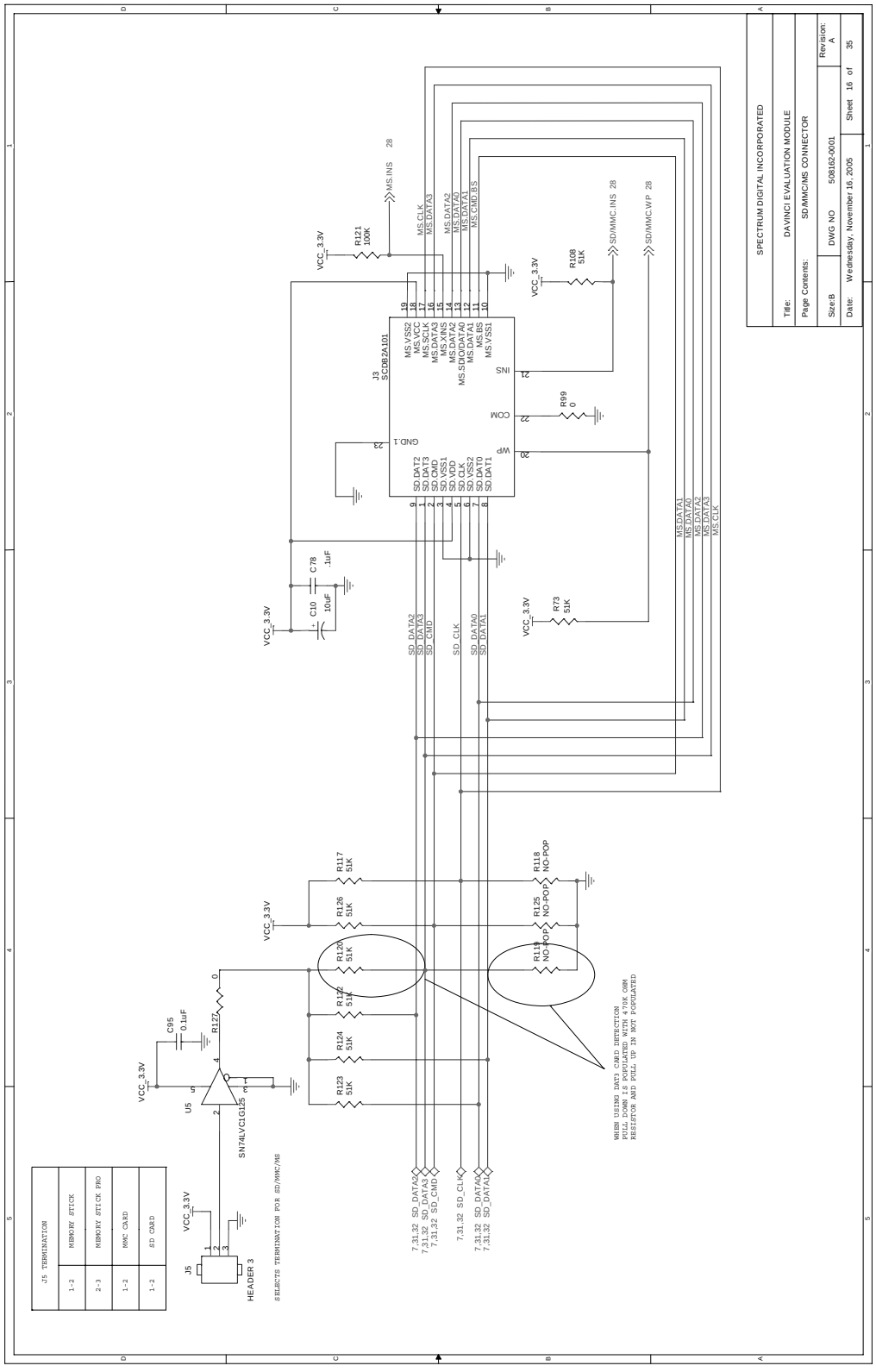

SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: DDR2 MEMORY
Size: B
DWG NO 5081620001
Revision: A
Date: Wednesday, November 16, 2005
Sheet 11 of 35
128 MEGABYTES
128 MEGABYTES
MT47H64M16BT
MT47H64M16BT
U20
U32
VCC_1.8V
VREF_STL
R208 1K 1%
R207 1K 1%
C102 NO-POP
C57 22 uF
C220 0.1uF
C218 0.1uF
C149 0.1uF
C225 0.1uF
C219 0.1uF
C21 0.1uF
C217 0.1uF
C223 0.1uF
C222 0.1uF
C224 0.1uF
C150 0.1uF
C151 0.1uF
C154 0.1uF
C18 22 uF
C153 0.1uF
C156 0.1uF
C155 0.1uF
C152 0.1uF
C157 0.1uF
RN20
RN19
RN31
RN27
RN6
RN26
RN5
RPACK4-47
BDDR_D[16-31]
BDDR_D[0-15]
4 DDR_A[0:12]
4 DDR_BS[0:2]
4 DDR_CAS
4 DDR_RAS
4 DDR_WE
4 DDR_CKE
4 DDR_CLK
4 DDR_CLK_N
4 DDR_DQS[0:3]
4 DDR_DQM[0:3]
4 DDR_D[0:31]

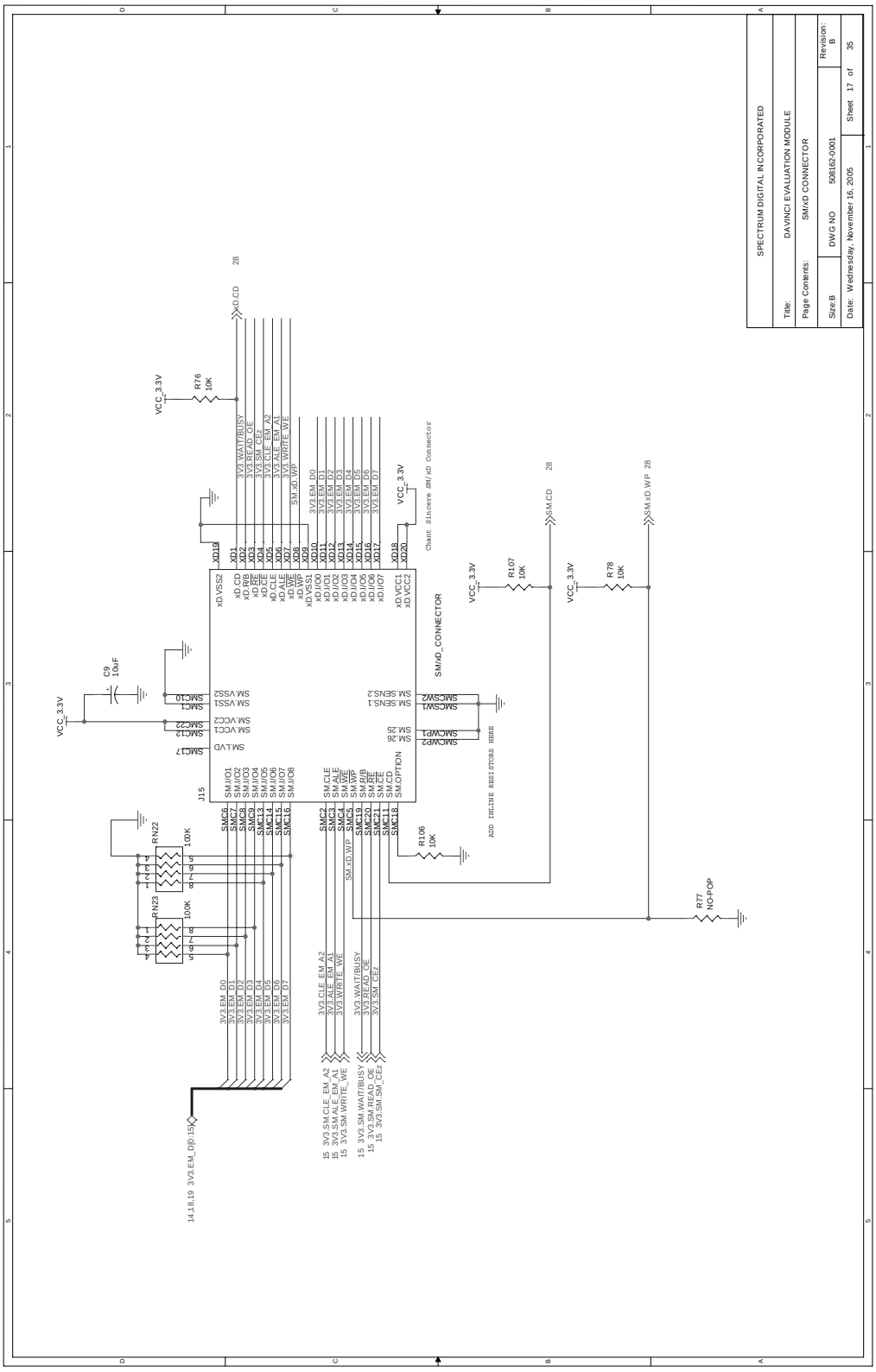

SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: SRAM/NAND FLASH
Size:B DWG NO 508162-0001 Revision: A
Date: Wednesday, November 16, 2005 Sheet 12 of 35
SRAM (4MBytes)
SAMSUNG->K1S32168CD
NAND FLASH (64MBytes)
K9K1G08 supports 128 MEGABYTES
SAMSUNG K9K1208/Q/D/U/0C
U7
U6
VCC_1.8V
EM_D[0:15] 3,13,14,29
B.EM_A[10:21] 13,14,29
EM_A[3:21] 3,13,14,29
SRAM_CE2 10
NAND_CE# 10
NAND_BUS 15
WRITE_WE 3,13,15,29
READ_OE 3,13,15,29
CLE_EM_A2 3,13,15,29
ALE_EM_A1 3,13,15,29
A17A2_EM_A0 3,13,15,29
A18A1_EM_BA1 3,13,15,29
C90 0.1uF
C91 0.1uF
C92 1uF
C93 .1uF
R134 0
R136 0
R137 10K
R138 10K
R135 10K
R141 10K
R140 10K
R113 NO-POP
R139 NO-POP
LOCKPRE

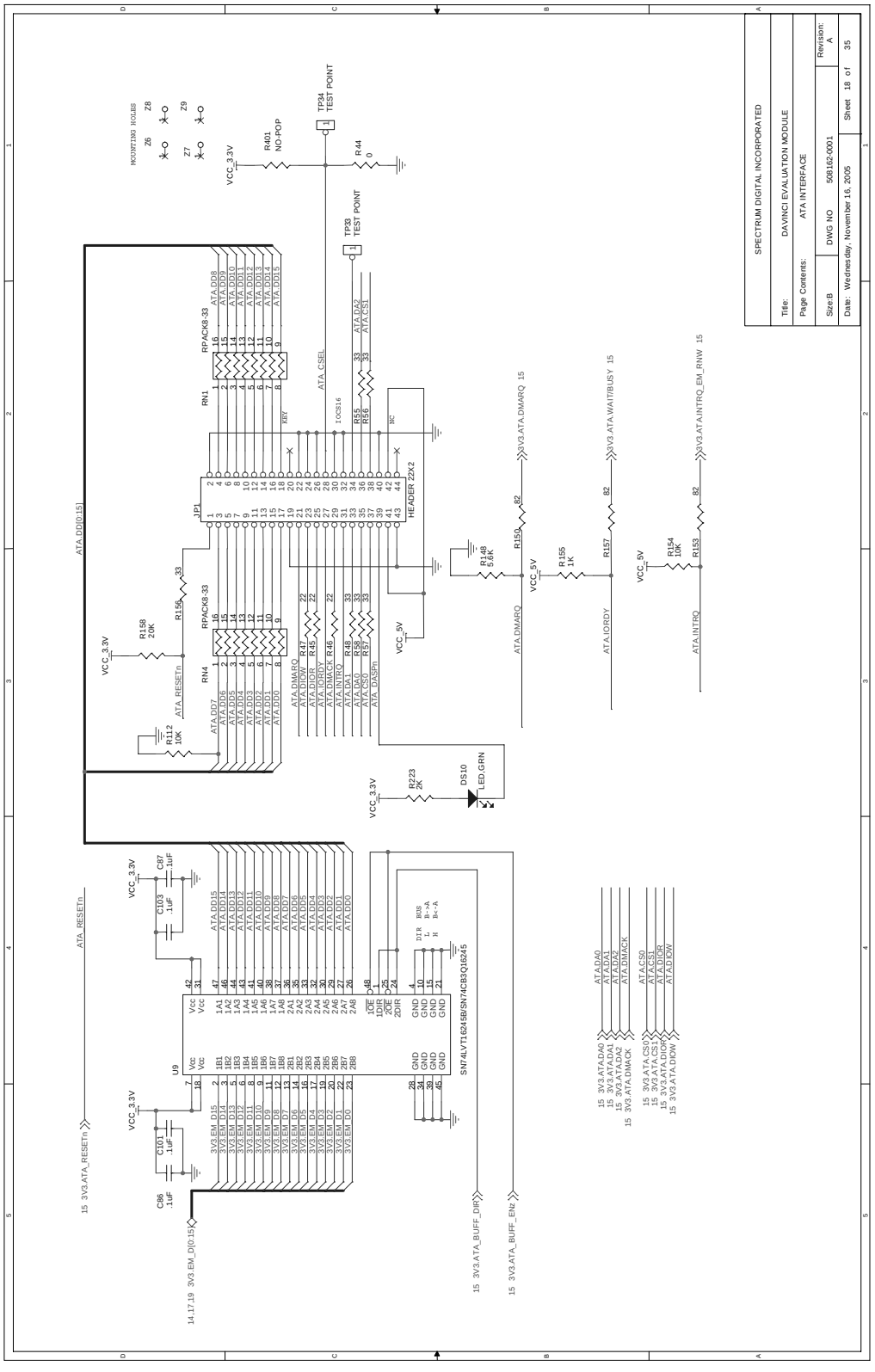

SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: NOR FLASH
Size:B
DWG NO 508162-0001
Revision: A
Date: Wednesday, November 16, 2005
Sheet 13 of 35
16 MBytes
U13 AM29LV256M
VCC_1.8V
VCC_3.3V
R143 10K
C94 .1uF
C120 .1uF
R142 10K
R114 10K
R115 10K
R116 NO-POP
EM_D[0:15] 3,12,14,29
3,12,15,29 ATA1_EM_BA1
3,12,15,29 ATA2_EM_A0
3,12,15,29 ALE_EM_A1
3,12,15,29 CLE_EM_A2
3,12,14,29 EM_A[3:21]
12,14,29 B.EM_A[10:21]
10 FLASH_CE2
3,12,15,29 READ_OE
3,12,15,29 WRITE_WE
8,15,26,29,30,31,34 1.8V_SYS_RESETz

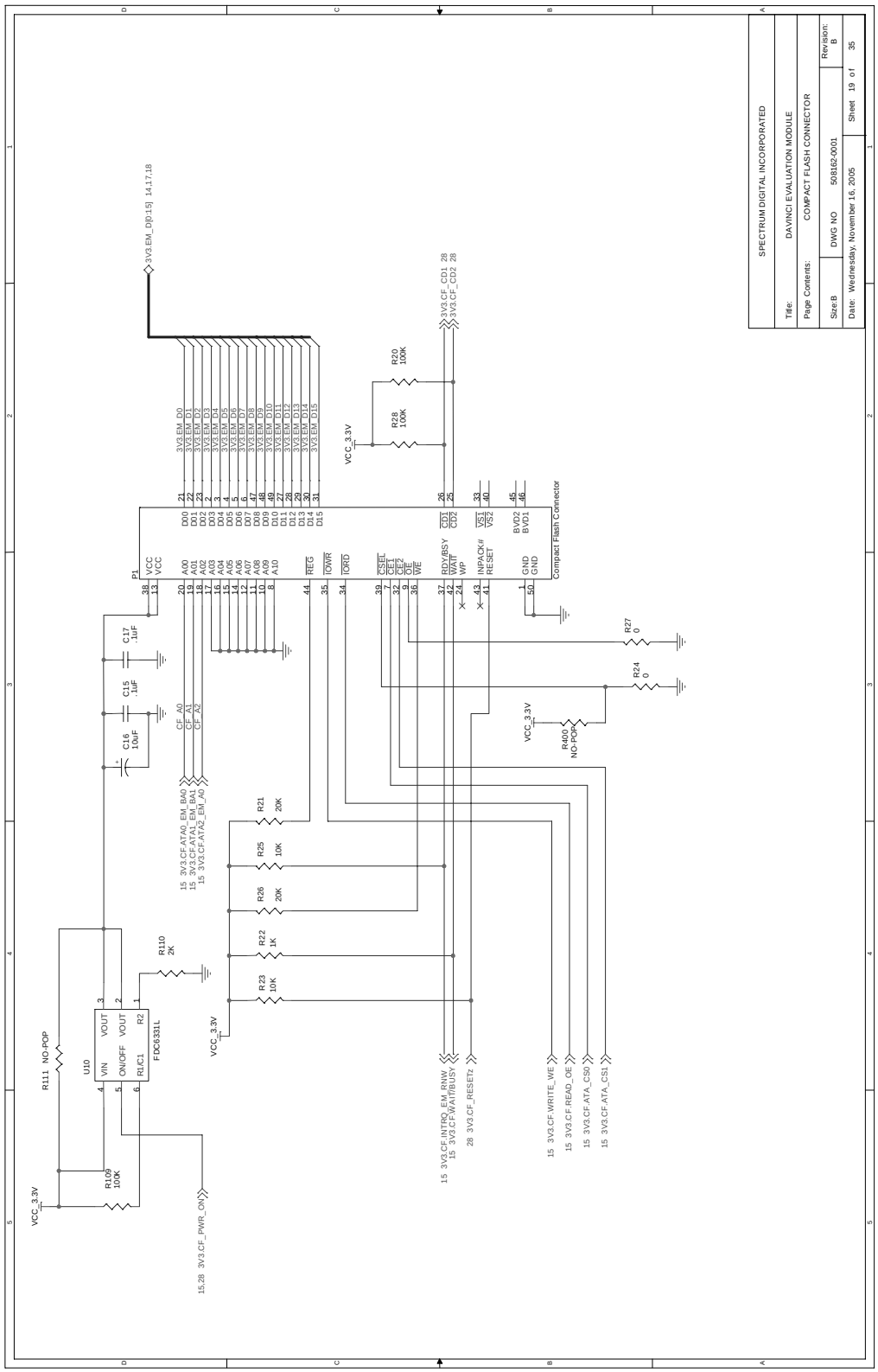

U11 is a switch used to enable Vlynq functions.
Signal levels are at 1.8 volt logic levels on both sides of switch
SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: EMIF LEVEL SHIFTER
Size:B
DWG NO 508162-0001
Revision: D
Date: Monday, March 06, 2006
Sheet 14 of 35
U11
SN74CBTLV16232DGGR
U8
SN74AVCB164245VR
VCC_3.3V
VCC_1.8V
R143 10K
R392 NO-POP
R393 NO-POP
C118 NO-POP
C119 NO-POP
C373 560pF
C116 5.6pF
C117 5.6pF
C121 0.1uF
C89 0.1uF
C106 0.1uF
C105 0.1uF
C88 0.1uF
R412 22
R413 22
R414 22
R415 22
R416 22
R417 22
R418 22
R419 22
VLYNQ_TXD0 32
VLYNQ_TXD1 32
VLYNQ_TXD2 32
VLYNQ_TXD3 32
WLAN_INTR 32
ELP_CLK_EN 32
ELP_REQ/WAKEUP 32
PM_EN 32
B.EM_A[0:21] 12,13,29
3V3.EM_D[0:15] 17,18,19
EM_D[0:15] 3,12,13,29
VLYNQ_RXD0 32
VLYNQ_RXD1 32
VLYNQ_RXD2 32
VLYNQ_RXD3 32
28 VLYNQ_ON
3,12,13,29 EM_A[0:21]
15 1V8.EM_DATA_BUF_DIR
15 1V8.EM_DATA_BUF_EN
L A TO B1
H B1 TO A
DIR BUS
L B->A
H A->B

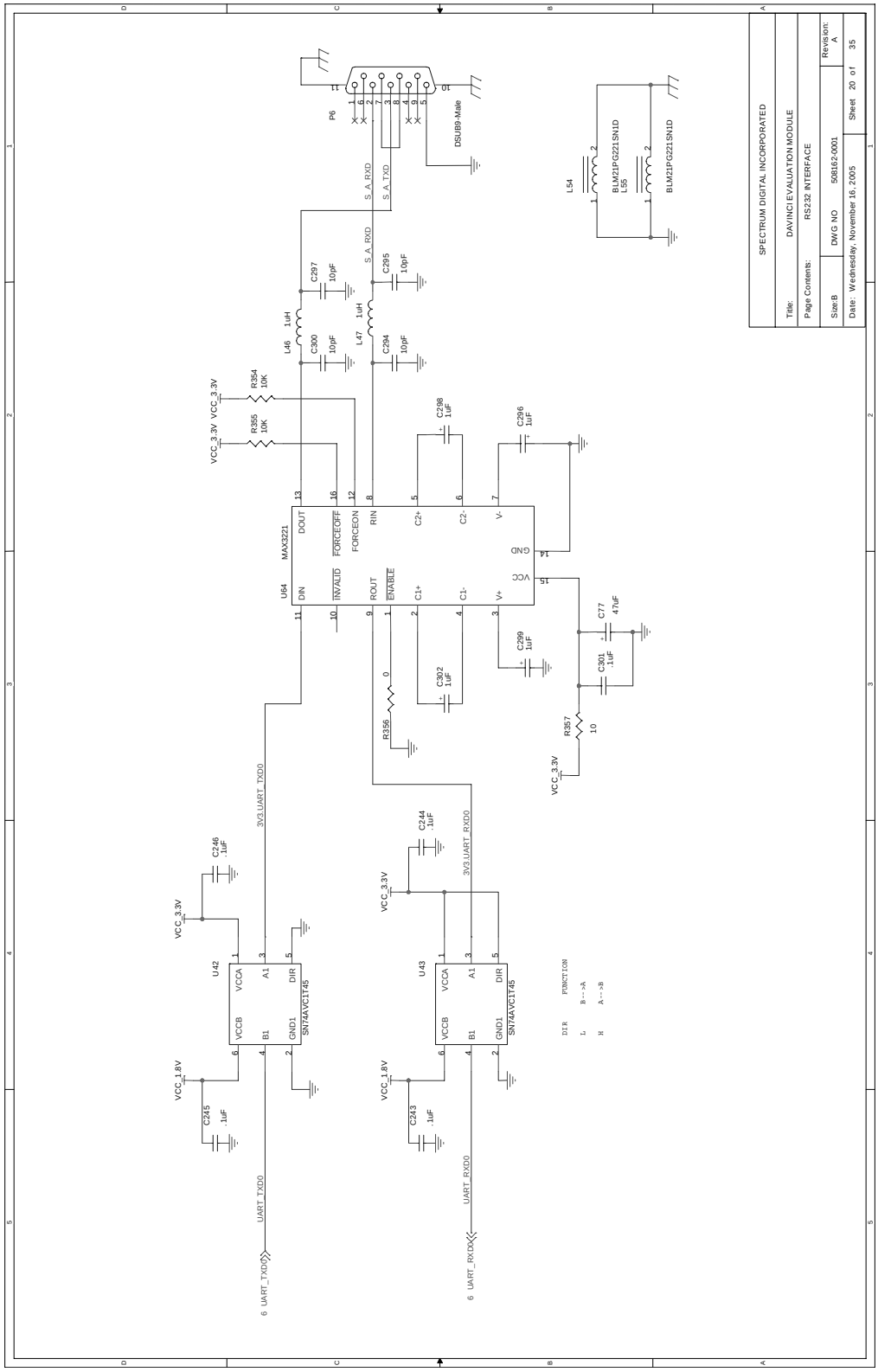

SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: EMIF DATA BUS LEVEL SHIFTER
Size: B
DWG NO 508162-0001
Revision: C
Date: Wednesday, November 16, 2005
Sheet 15 of 35
CPLD REVISION 508163-0001B
EPM240/GTC100
SMT FEMALE HEADER 5X2
RP ACN4-10K
NO-POP
BLM41P750SPT
VCC_3.3V
VCC_1.8V

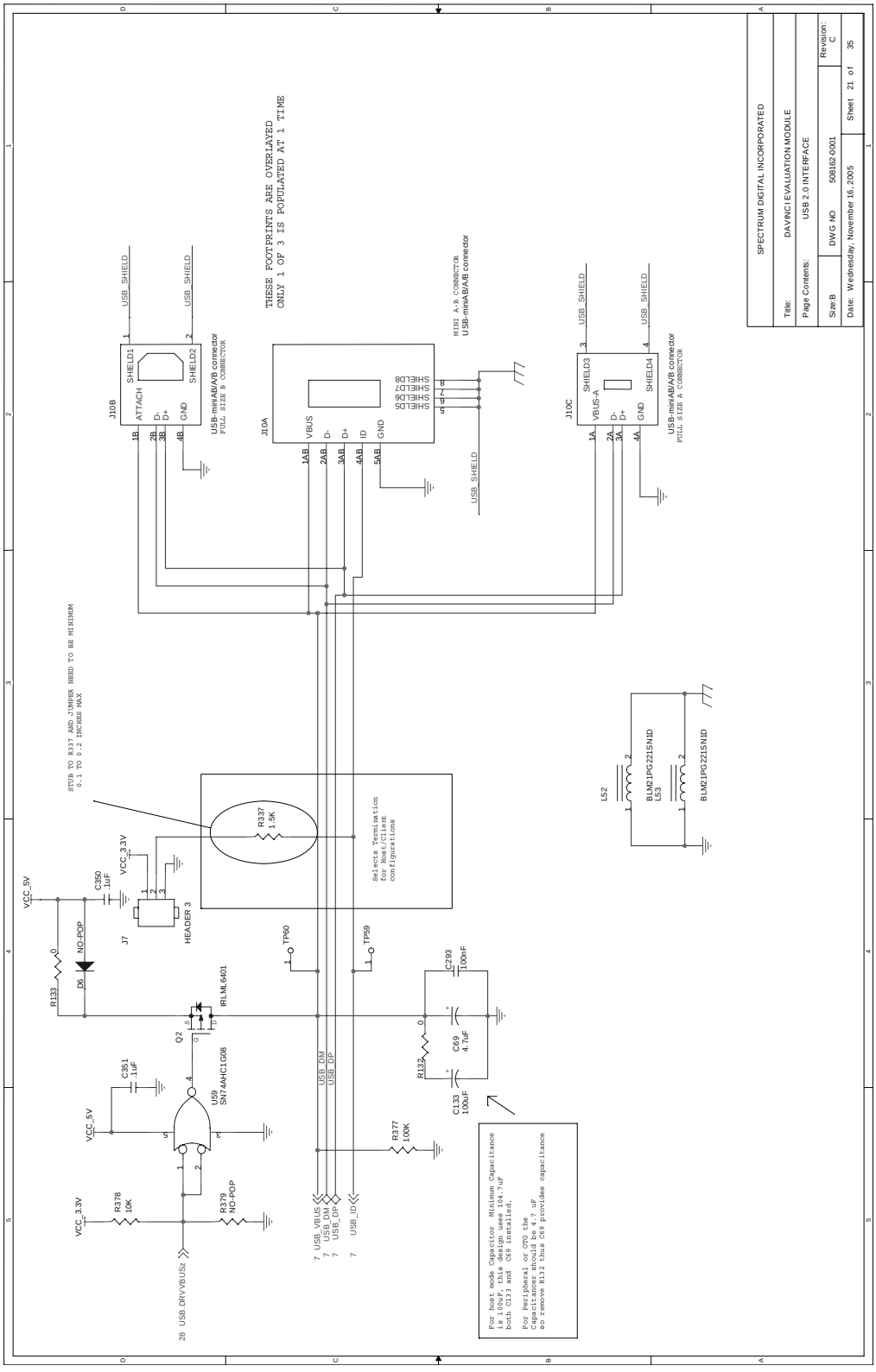

SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: SD/MMC/MS CONNECTOR
Size:B
DWG NO 508162-0001
Revision: A
Date: Wednesday, November 16, 2005
Sheet 16 of 35
J5 TERMINATION
MEMORY STICK
MEMORY STICK PRO
MMC CARD
SD CARD
HEADER 3
SN74LVC1G125
SD/MMC.INS
SD/MMC.WP
SCDB2A101
SELECTS TERMINATION FOR SD/MMC/MS
WHEN USING DAT3 CARD DETECTION PULL DOWN IS POPULATED WITH 470K OHM RESISTOR AND PULL UP IS NOT POPULATED

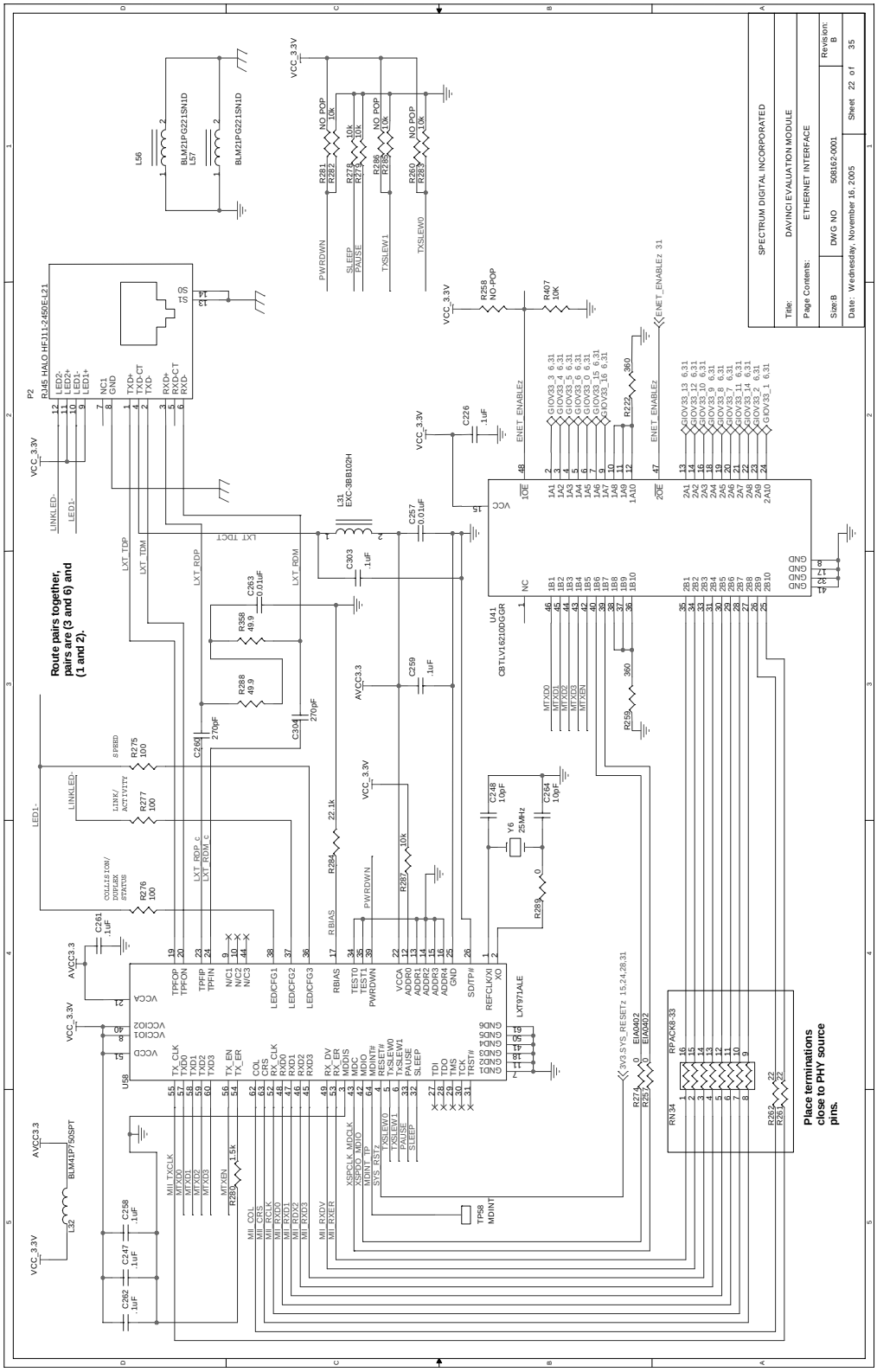

SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: SM/xD CONNECTOR
Size:B DWG NO 508162-0001 Revision: B
Date: Wednesday, November 16, 2005 Sheet 17 of 35
SM/xD_CONNECTOR
Chant Sincere SM/xD Connector
VCC_3.3V
R76 10K
R107 10K
R78 10K
R106 10K
R77 NO-POP
C9 10uF
RN22 100K
RN23 100K
ADD INLINE RESISTORS HERE
J15

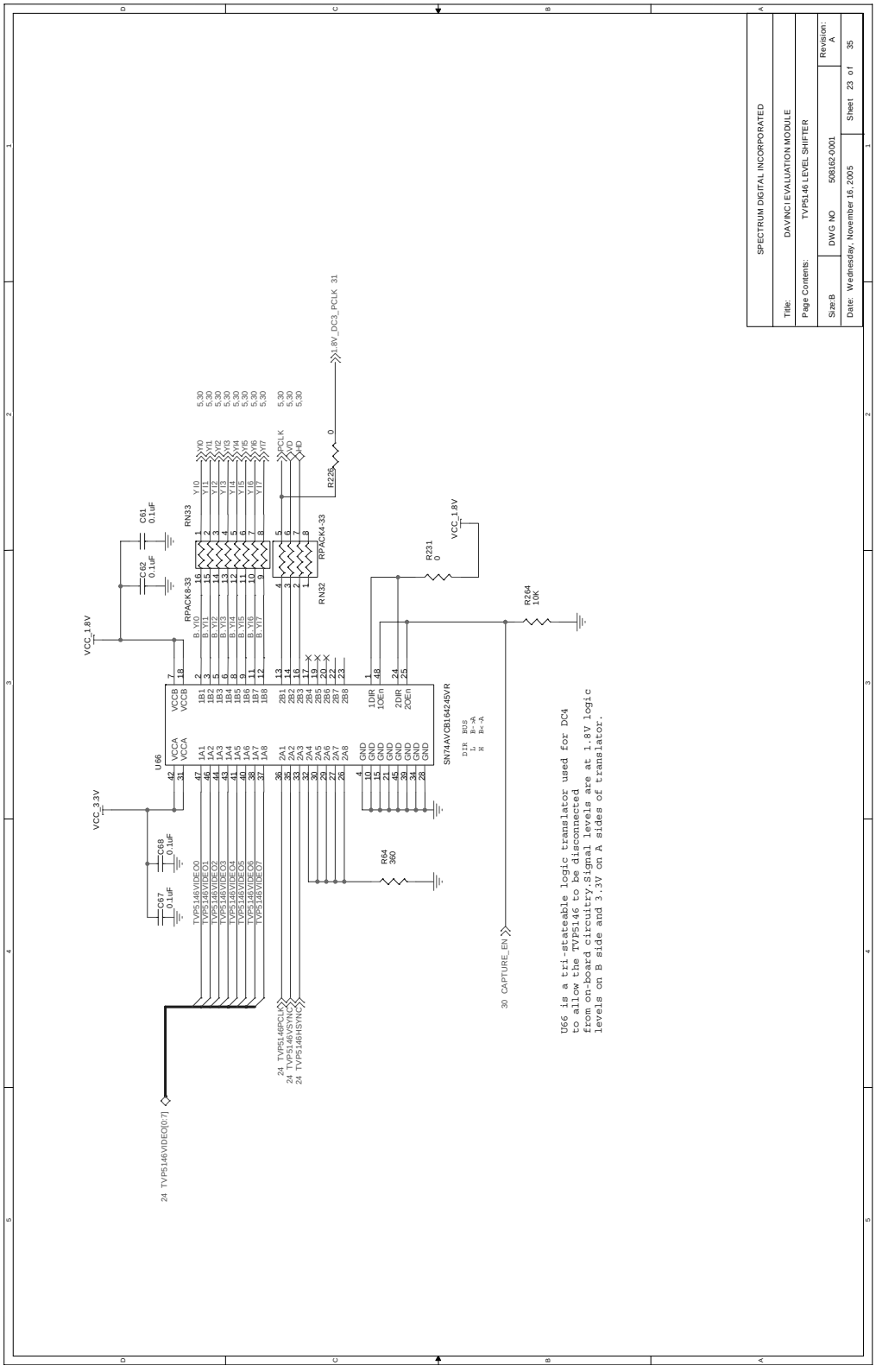

SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: ATA INTERFACE
Size:B
DWG NO 508162-0001
Revision: A
Date: Wednesday, November 16, 2005
Sheet 18 of 35
MOUNTING HOLES
Z5
Z6
Z7
Z8
Z9
TP34 TEST POINT
TP33 TEST POINT
RA01 NO-POP
R44 0
VCC_3.3V
RN1 RPACK8-33
RN4 RPACK8-33
ATA.DD8
ATA.DD9
ATA.DD10
ATA.DD11
ATA.DD12
ATA.DD13
ATA.DD14
ATA.DD15
ATA.DA2
ATA.CS1
ATA.CSEL
KBY
IOCS16
NC
R55 33
R56 33
JP1 HEADER 22X2
R158 20K
R156 33
ATA_RESETn
R112 10K
ATA.DD7
ATA.DD6
ATA.DD5
ATA.DD4
ATA.DD3
ATA.DD2
ATA.DD1
ATA.DD0
ATA.DD[0:15]
ATA.DMARQ
ATA.DIOW
ATA.DIOR
ATA.IORDY
ATA.DMACK
ATA.INTRQ
ATA.DA1
ATA.DA0
ATA.CS0
ATA_DASPn
R47 22
R45 22
R46 33
R48 33
R58 33
R57 33
R149 5.6K
R150 82
R155 1K
R157 82
R154 10K
R153 82
VCC_5V
ATA.DMARQ
ATA.IORDY
ATA.INTRQ
3V3.ATA.DMARQ 15
3V3.ATA.WAITBUSY 15
3V3.ATA.INTRQ_EM_RNW 15
R223 2K
DS10 LED,GRN
U9 SN74LVT16245B/SN74CB3Q16245
C86 .1uF
C101 .1uF
C103 .1uF
C87 .1uF
3V3.EM_D15
3V3.EM_D14
3V3.EM_D13
3V3.EM_D12
3V3.EM_D11
3V3.EM_D10
3V3.EM_D09
3V3.EM_D08
3V3.EM_D07
3V3.EM_D06
3V3.EM_D05
3V3.EM_D04
3V3.EM_D03
3V3.EM_D02
3V3.EM_D01
3V3.EM_D00
3V3.EM_D[0:15]
3V3.ATA_RESETn
3V3.ATA_BUFF_DIR
3V3.ATA_BUFF_ENz
3V3.ATA.DA0
3V3.ATA.DA1
3V3.ATA.DA2
3V3.ATA.DMACK
3V3.ATA.CS0
3V3.ATA.CS1
3V3.ATA.DIOR
3V3.ATA.DIOW
DIR BUS
L B->A
H B<-A

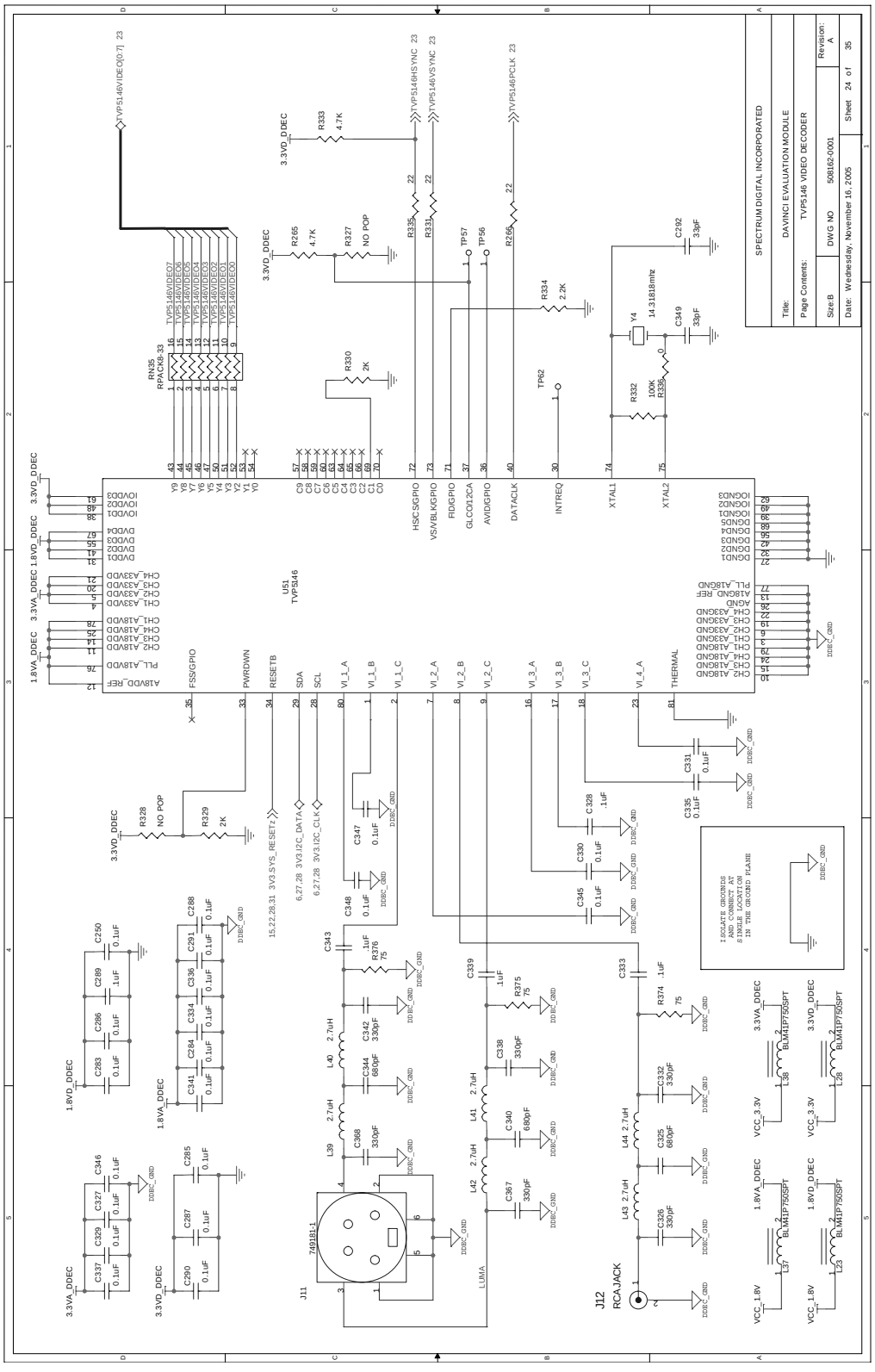

SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: COMPACT FLASH CONNECTOR
Size:B DWG NO 508162-0001 Revision: B
Date: Wednesday, November 16, 2005 Sheet 19 of 35
P1
Compact Flash Connector
U10
FDC6331L
VCC_3.3V
R111 NO-POP
R110 2K
R109 100K
R20 100K
R28 100K
R21 20K
R25 10K
R26 20K
R22 1K
R23 10K
R27 0
R24 0
R400 NO-POP
C17 .1uF
C15 .1uF
C16 10uF
3V3.EM_D[0:15] 14.17.18
3V3.CF_CD1 28
3V3.CF_CD2 28
3V3.CF_PWR_ON 15,28
3V3.CF_INTRQ_EM_RNW 15
3V3.CF.WAIT/BUSY 15
3V3.CF_RESETz 28
3V3.CF.WRITE_WE 15
3V3.CF.READ_OE 15
3V3.CF.ATA_CS0 15
3V3.CF.ATA_CS1 15

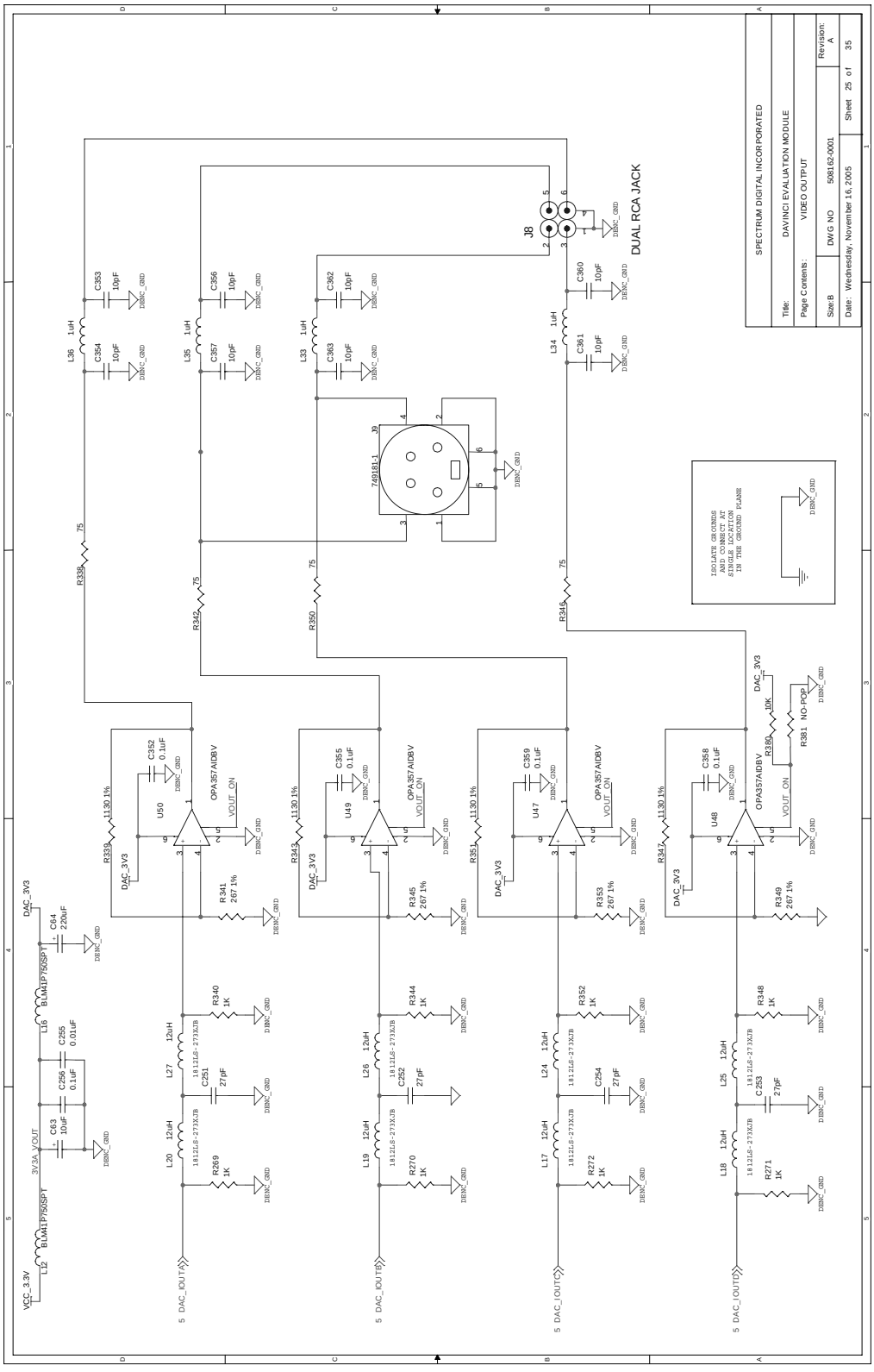

SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: RS232 INTERFACE
Size:B
DWG NO 508162-0001
Revision: A
Date: Wednesday, November 16, 2005
Sheet 20 of 35
P6
DSUB9-Male
S_A_RXD
S_A_TXD
L54
L55
BLM21PG221SN1D
C297 10pF
C295 10pF
L46 1uH
L47 1uH
C300 10pF
C294 10pF
R354 10K
R355 10K
VCC_3.3V
C298 1uF
C296 1uF
U64
MAX3221
DOUT
FORCEOFF
FORCEON
RIN
C2+
C2-
V-
GND
DIN
INVALID
ROUT
ENABLE
C1+
C1-
V+
VCC
C77 47uF
C299 1uF
C301 .1uF
C302 1uF
R356 0
R357 10
3V3_UART_TXD0
3V3_UART_RXD0
C246 1uF
C244 .1uF
U42
U43
SN74AVC1T45
VCCA
VCCB
A1
B1
DIR
GND1
C245 .1uF
C243 .1uF
VCC_1.8V
UART_TXD0
UART_RXD0
6 UART_TXD0
6 UART_RXD0
DIR FUNCTION
L B-->A
H A-->B

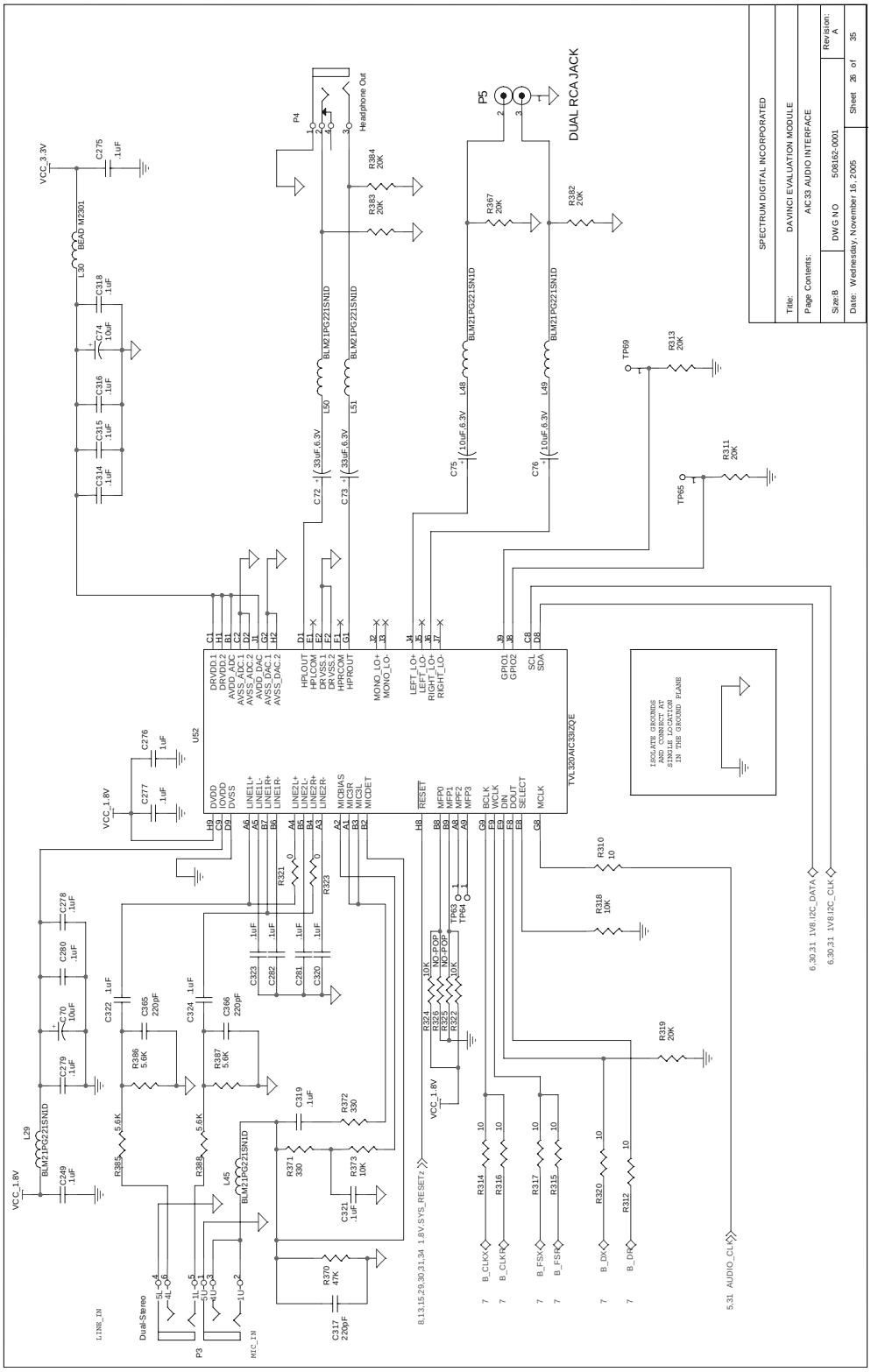

SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: USB 2.0 INTERFACE
Size:B DWG NO 508162-0001 Revision: C
Date: Wednesday, November 16, 2005 Sheet 21 of 35
THESE FOOTPRINTS ARE OVERLAYED
ONLY 1 OF 3 IS POPULATED AT 1 TIME
MINI A-B CONNECTOR
USB-miniAB/A/B connector
J10A
J10B
J10C
USB_SHIELD
VBUS
D-
D+
ID
GND
ATTACH
VBUS-A
USB-miniAB/A/B connector
FULL SIZE B CONNECTOR
FULL SIZE A CONNECTOR
STUB TO R137 AND JUMPER NEED TO BE MINIMUM
0.1 TO 0.2 INCHES MAX.
R337
1.5K
Select Termination
for Host/Peripheral
configurations
VCC_5V
VCC_3.3V
C350
1uF
J7
HEADER 3
R133
0
NO-POP
D6
IRLML6401
Q2
C351
.1uF
U59
SN74AHC1G08
R378
10K
R379
NO-POP
TP60
TP59
C293
100nF
R132
0
C69
4.7uF
C133
100uF
R377
100K
L52
L53
BLM21PG221SN1D
USB_VBUS
USB_DM
USB_DP
USB_ID
USB_DRVVBUS
For host mode Capacitor Minimum Capacitance
is 100uF, this design uses 104.7uF
both C133 and C69 installed.
For Peripheral or OTG the
Capacitance should be 4.7 uF
so remove R132 this C69 provides capacitance

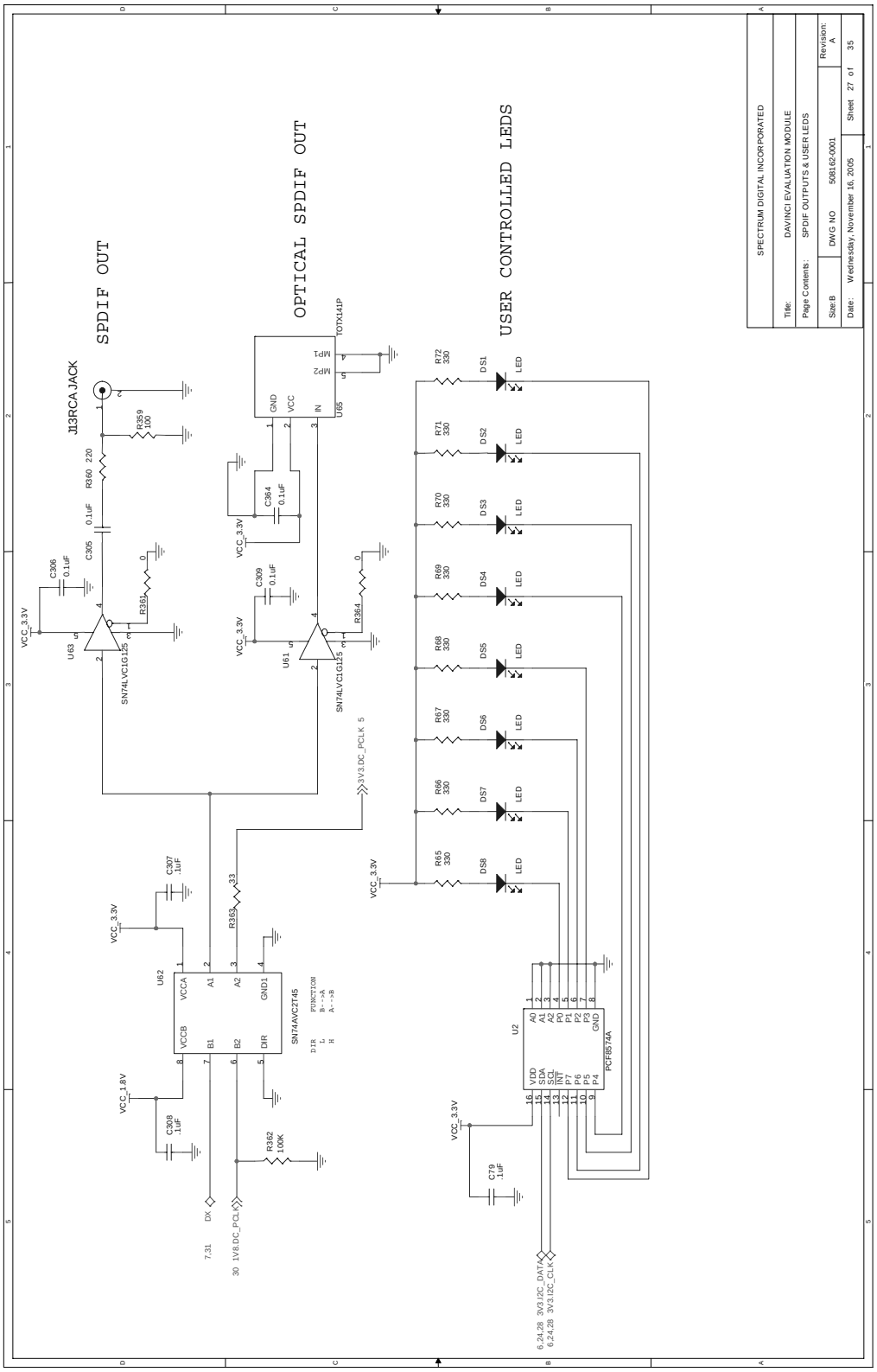

SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: ETHERNET INTERFACE
Size:B
DWG NO. 508162-0001
Revision: B
Date: Wednesday, November 16, 2005
Sheet 22 of 35
Route pairs together, pairs are (3 and 6) and (1 and 2).
Place terminations close to PHY source pins.
P2
RJ45 HALO HFJ11-2450E-L21
U41
CBT-LV16210DGGR
U58
LXT971ALE
Y6
25MHz
L56
L57
BLM21PG221SN1D
L32
BLM41PF750SPT
L31
EXC-38B102H
RN34
RPACK8-33
TP58
MDINT

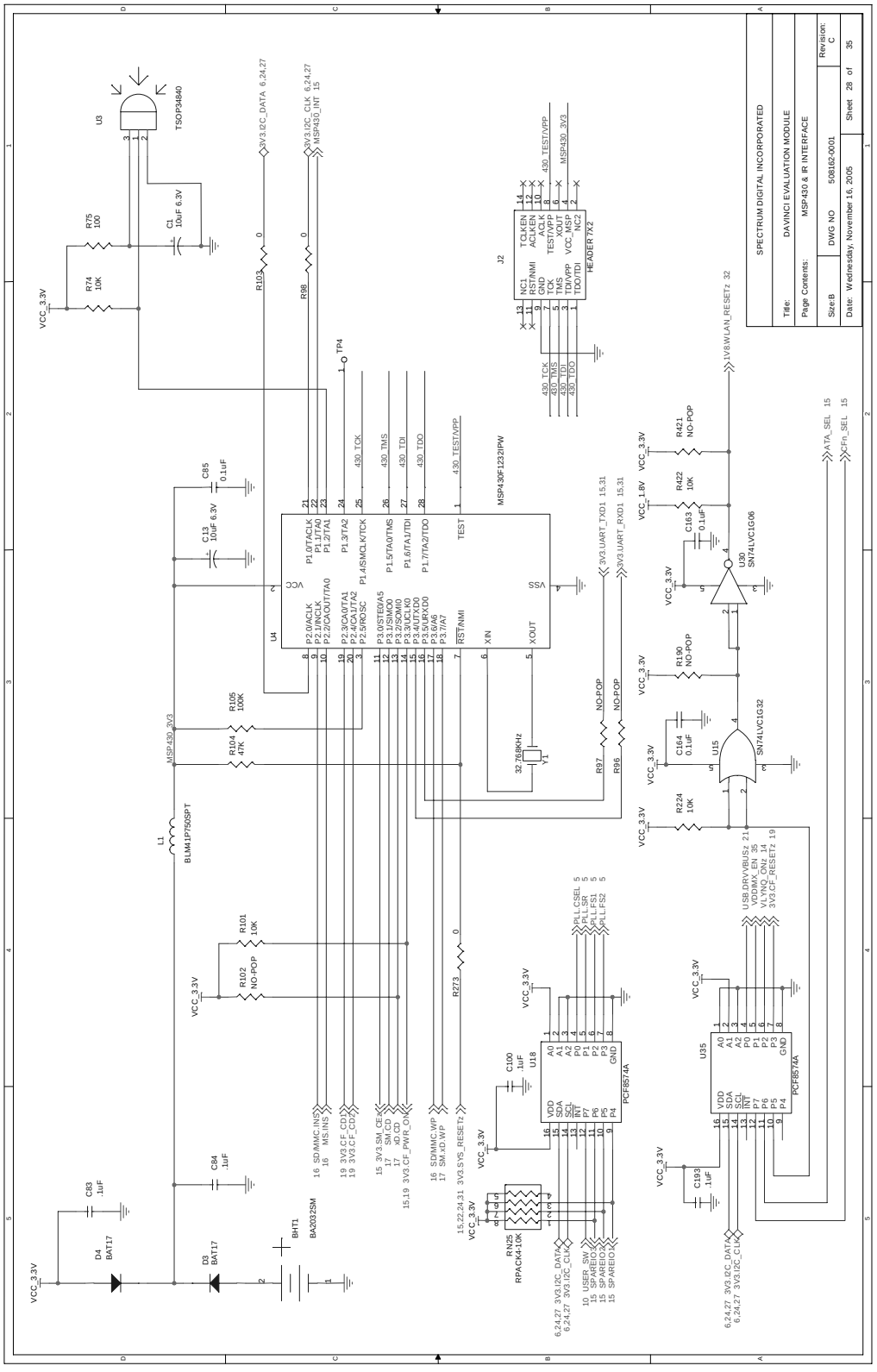

SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: TVP5146 LEVEL SHIFTER
Size: B
DWG NO 508162-0001
Revision: A
Date: Wednesday, November 16, 2005
Sheet 23 of 35
U66
SN74AVCB164245VR
RPACK8-33
RPACK4-33
RN33
RN32
VCC_1.8V
VCC_3.3V
C61 0.1uF
C62 0.1uF
C67 0.1uF
C68 0.1uF
R231 0
R235 0
R264 10K
R64 360
1.8V_DC3_PCLK 31
30 CAPTURE_EN
24 TVP5146VIDEO[0:7]
24 TVP5146PCLK
24 TVP5146VSYNC
24 TVP5146HSYNC
U66 is a tri-stateable logic translator used for DC4
to allow the TVP5146 to be disconnected
from on-board circuitry.Signal levels are at 1.8V logic
levels on B side and 3.3V on A sides of translator.

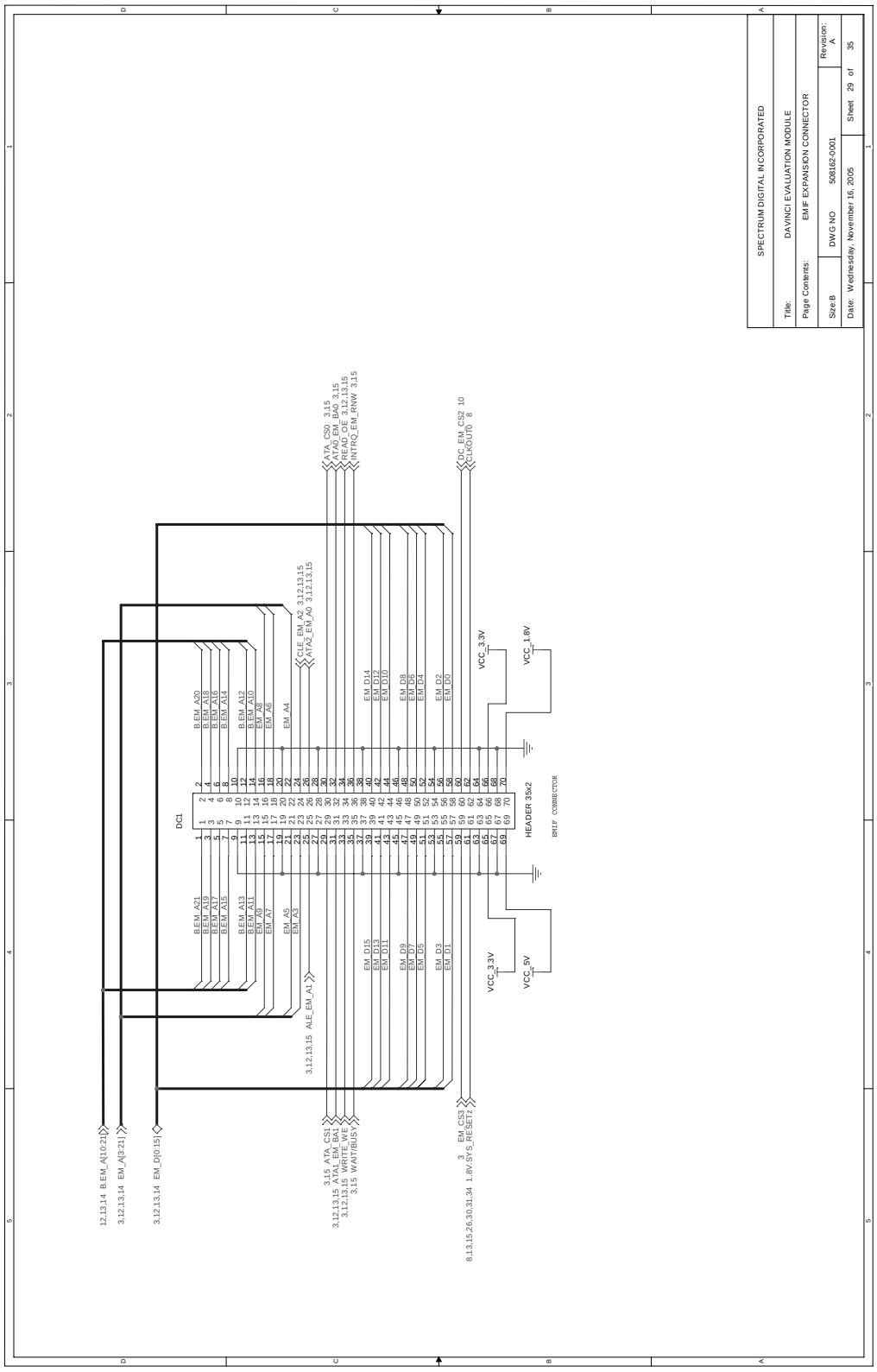

SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: TVP5146 VIDEO DECODER
Size: B
DWG NO 508162-0001
Revision: A
Date: Wednesday, November 16, 2005
Sheet 24 of 35
U51 TVP5146
RN35 RPACK8-33
J11 749181-1
J12 RCA JACK
Y4 14.31818mhz
ISOLATE GROUNDS AND CONNECT AT SINGLE LOCATION IN THE GROUND PLANE
LUMA

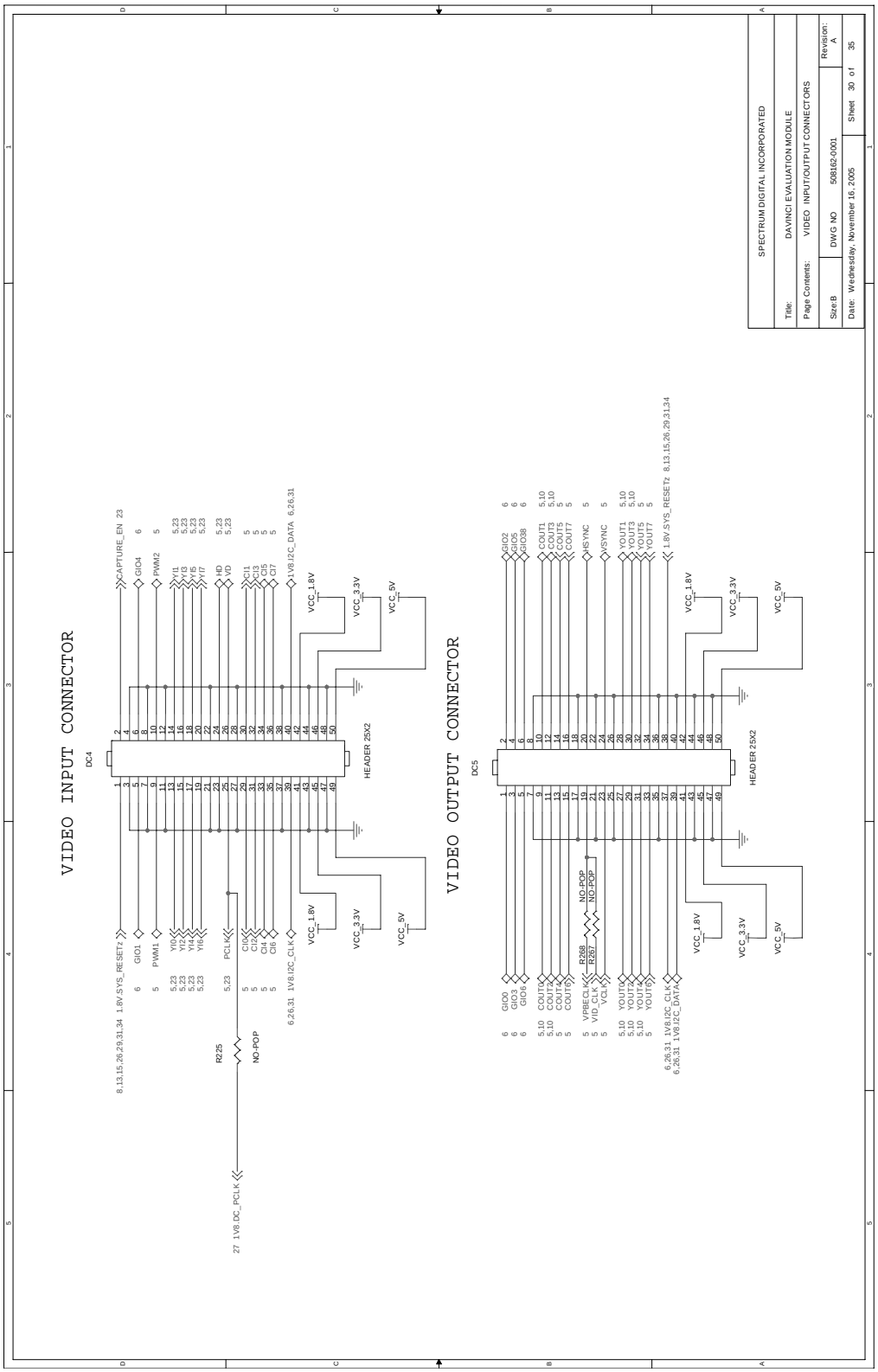

SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: VIDEO OUTPUT
Size: B
DWG NO 508102-0001
Revision: A
Date: Wednesday, November 16, 2005
Sheet 25 of 35
DUAL RCA JACK
J8
J9
74981-1
OPA357AIDBV
VOUT_ON
DAC_3V3
VCC_3.3V
3V3A_VOUT
DAC_IOUTA
DAC_IOUTB
DAC_IOUTC
DAC_IOUTD
DBNC_GND
ISOLATE GROUNDS AND CONNECT AT SINGLE LOCATION IN THE GROUND PLANE
NO-POP

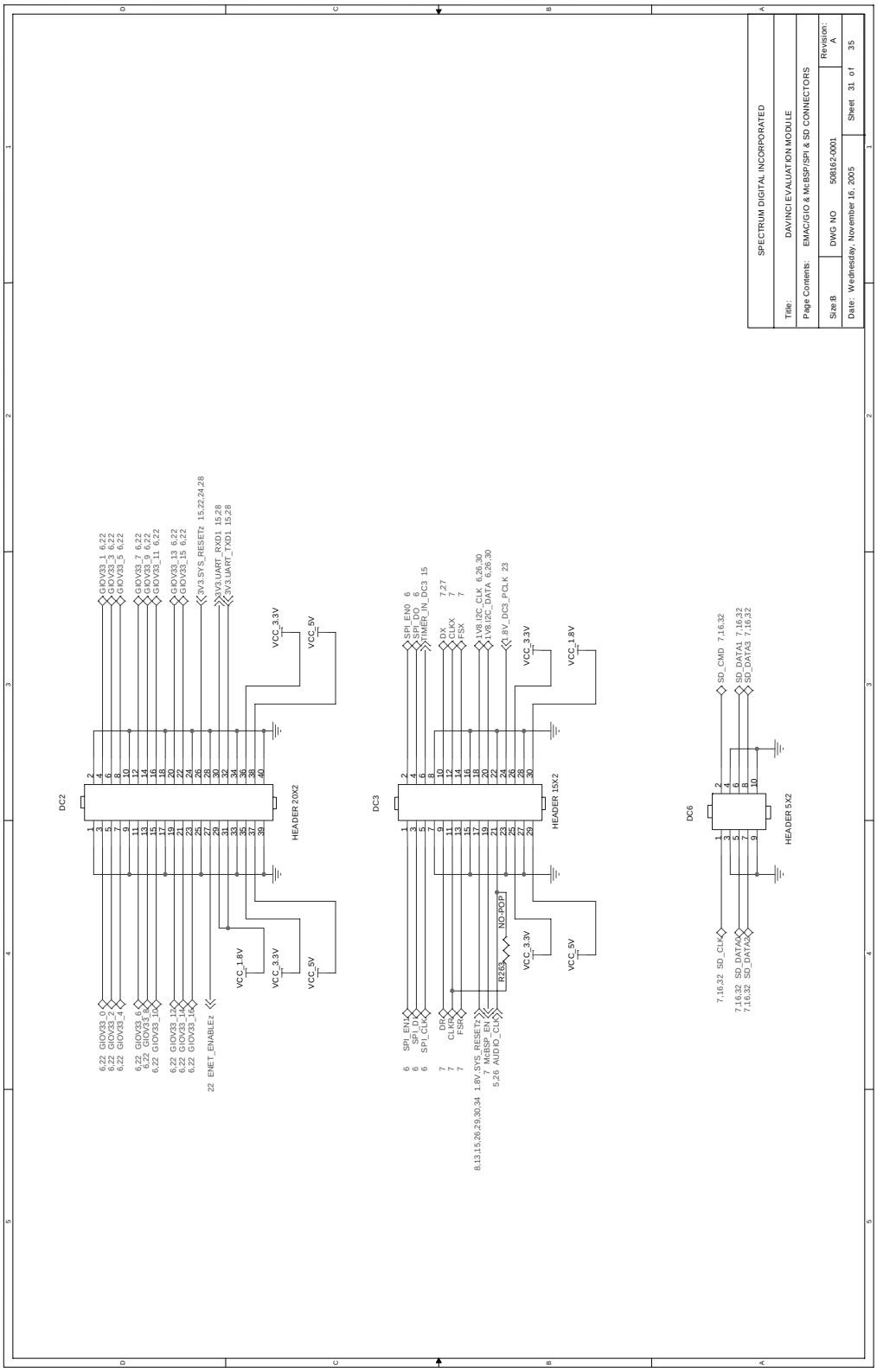

SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: AIC33 AUDIO INTERFACE
Size:B DWG NO 508162-0001 Revision: A
Date: Wednesday, November 16, 2005 Sheet 26 of 35
TVL320AIC3312QE
DUAL RCA JACK
Headphone Out
ISOLATE GROUNDS AND CONNECT AT SINGLE LOCATION IN THE GROUND PLANE
6,30,31 1V8 I2C_DATA
6,30,31 1V8 I2C_CLK
8,13,15,29,30,31,34 1.8V SYS_RESETz
5,31 AUDIO_CLK

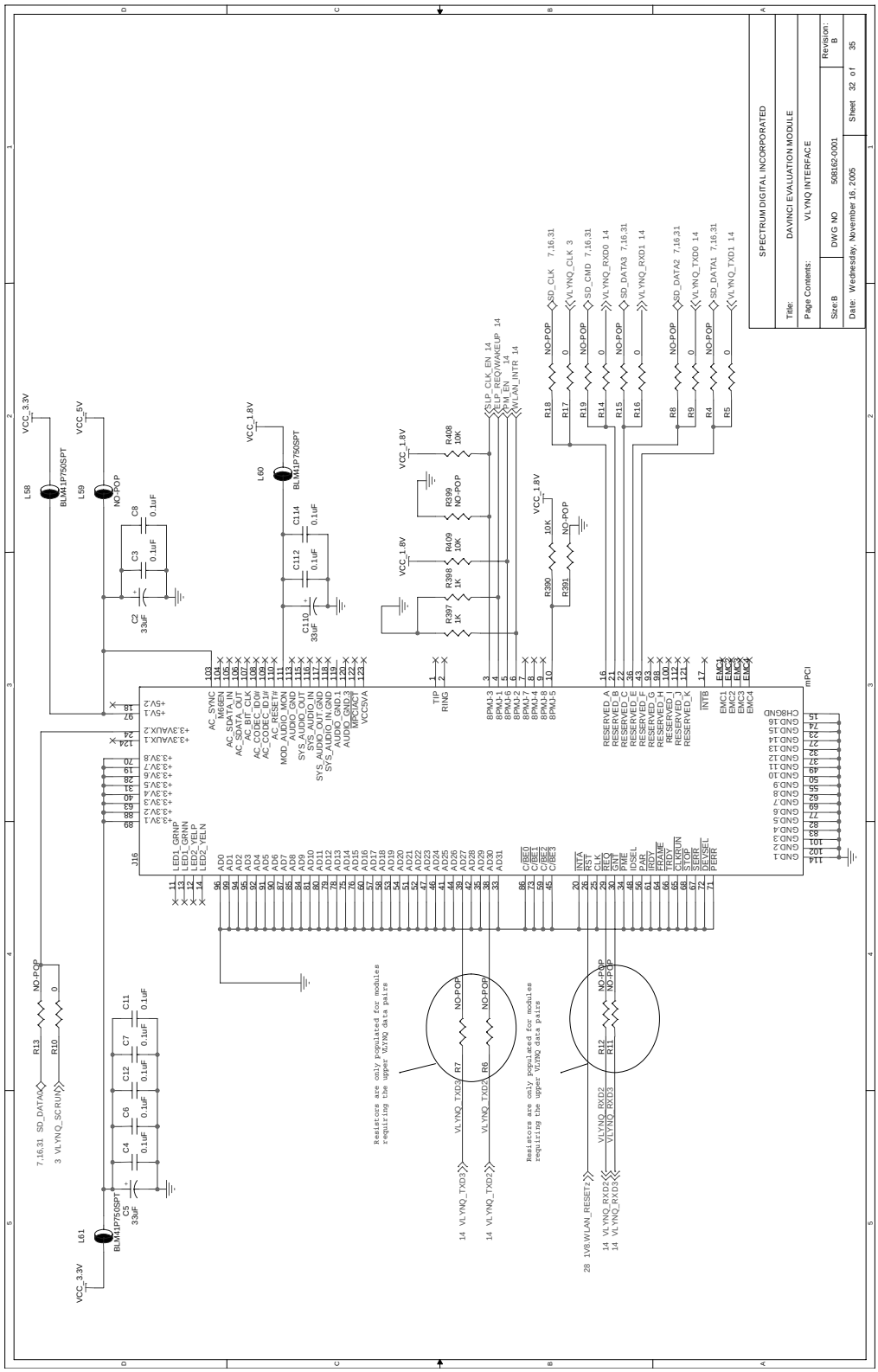

SPDIF OUT
J13RCA JACK
OPTICAL SPDIF OUT
TOTX141P
U65
GND
VCC
IN
MP1
MP2
R359 100
R360 220
C305 0.1uF
C306 0.1uF
R361 0
U63
SN74LVC1G125
C364 0.1uF
C309 0.1uF
R364 0
U61
SN74LVC1G125
VCC_3.3V
USER CONTROLLED LEDS
DS1 LED
DS2 LED
DS3 LED
DS4 LED
DS5 LED
DS6 LED
DS7 LED
DS8 LED
R72 330
R71 330
R70 330
R69 330
R68 330
R67 330
R66 330
R65 330
3V3.I2C_PCLK 5
C307 .1uF
R363 33
U62
SN74AVC2T45
VCCA
VCCB
A1
A2
B1
B2
DIR
GND1
C308 .1uF
R362 100K
VCC_1.8V
DX
7,31
30 1V8.I2C_PCLK
U2
PCF8574A
VDD
SDA
SCL
INT
P7
P6
P5
P4
P0
P1
P2
P3
GND
A0
A1
A2
C79 .1uF
6,24,28 3V3.I2C_DAT
6,24,28 3V3.I2C_CLK
SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: SPDIF OUTPUTS & USER LEDS
Size: B
DWG NO 508162-0001
Revision: A
Date: Wednesday, November 16, 2005
Sheet 27 of 35

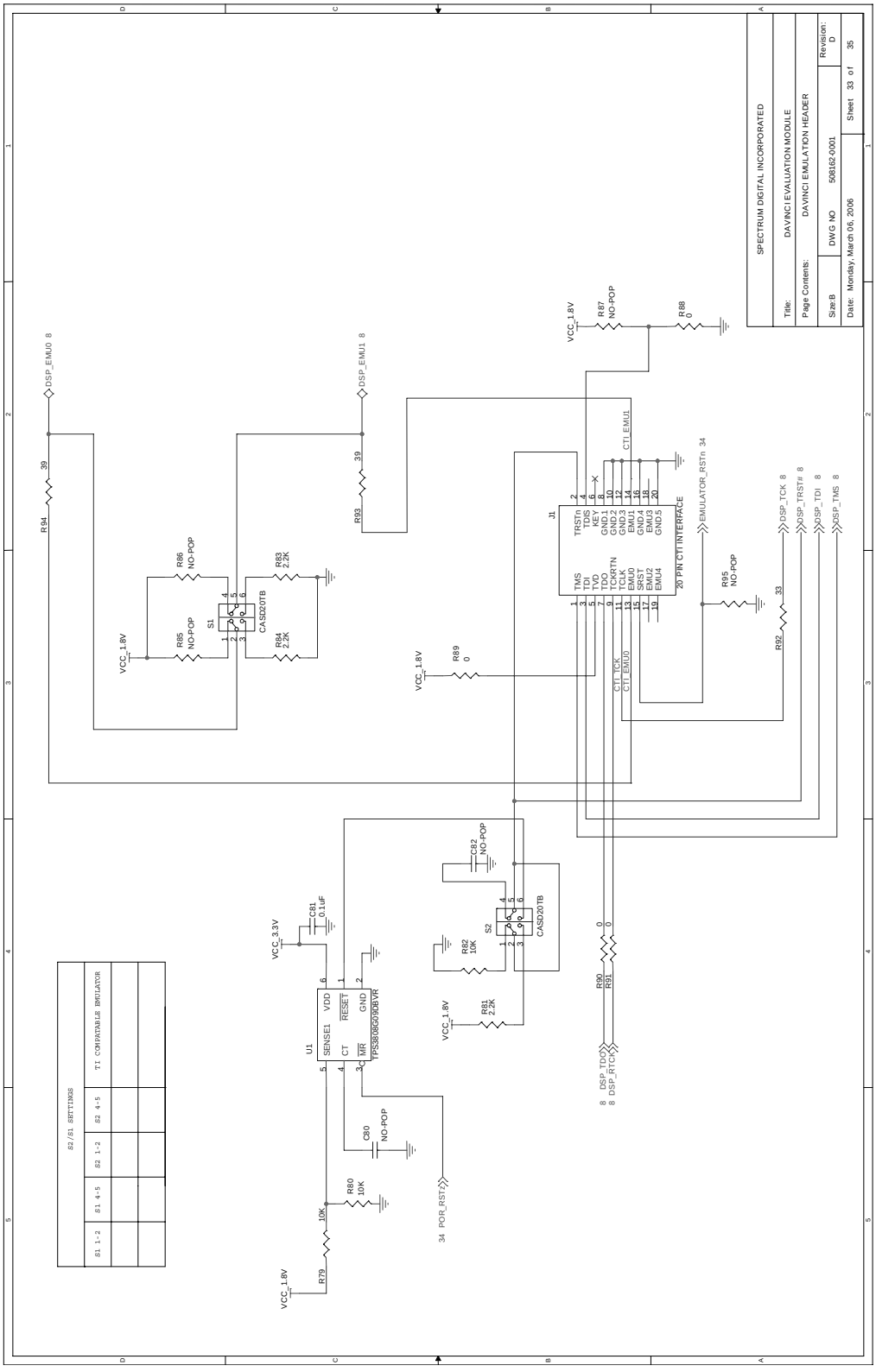

SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: MSP430 & IR INTERFACE
Size B
DWG NO 508162-0001
Revision: C
Date: Wednesday, November 16, 2005
Sheet 28 of 35
MSP430F1232IPW
TSOP34840
PCF8574A
SN74LVC1G32
SN74LVC1G06
HEADER 7X2
BA2032SM
BLM41P750SPT
RPACK4-10K
32.768KHz
VCC_3.3V
VCC_1.8V
MSP430_3V3
NO-POP

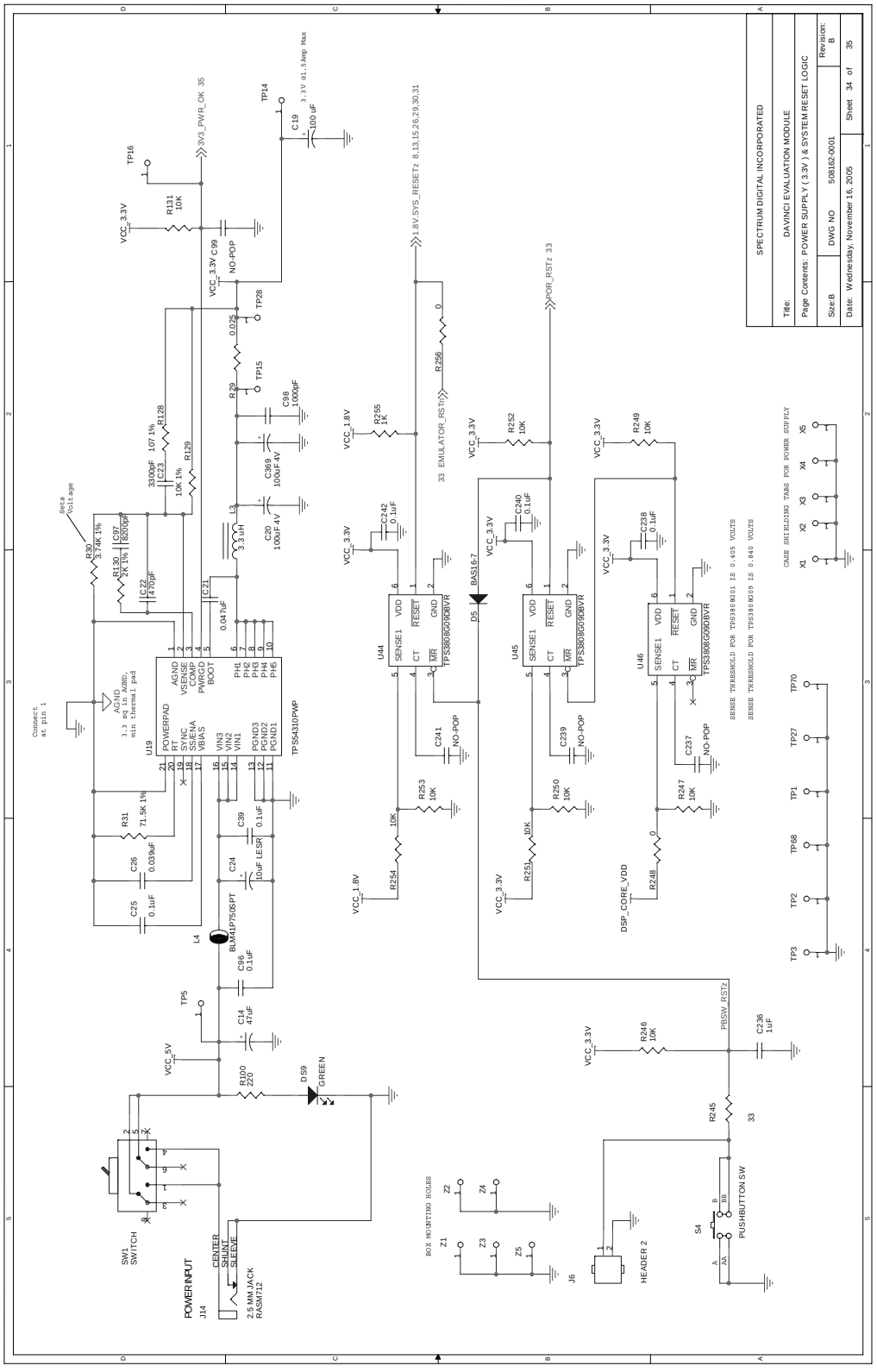

SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: EMIF EXPANSION CONNECTOR
Size:B
DWG NO 508152-0001
Revision: A
Date: Wednesday, November 16, 2005
Sheet 29 of 35
DC1
HEADER 35x2
EMIF CONNECTOR
VCC_3.3V
VCC_1.8V
VCC_5V
VCC_3.3V
B.EM_A21
B.EM_A19
B.EM_A17
B.EM_A15
B.EM_A13
B.EM_A11
EM_A9
EM_A7
EM_A5
EM_A3
B.EM_A20
B.EM_A18
B.EM_A16
B.EM_A14
B.EM_A12
B.EM_A10
EM_A8
EM_A6
EM_A4
C1LE_EM_A2 3,12,13,15
ATA2_EM_A0 3,12,13,15
EM_D15
EM_D13
EM_D11
EM_D9
EM_D7
EM_D5
EM_D3
EM_D1
EM_D14
EM_D12
EM_D10
EM_D8
EM_D6
EM_D4
EM_D2
EM_D0
ATA_CS0 3,15
ATA0_EM_BA0 3,15
READ_OE 3,12,13,15
INTRQ_EM_RNW 3,15
OP_EM_CS2 10
CLKOUT0 8
12,13,14 B.EM_A[10:21]
3,12,13,14 EM_A[3:21]
3,12,13,14 EM_D[0:15]
3,15 ATA_CS1
3,12,13,15 ATA1_EM_BA1
3,12,13,15 WRITE_WE
3,15 WAIT/BUSY
3 EM_CS2
8,13,15,26,30,31,34 1.8V SYS_RESET2
ALE_EM_A1
3,12,13,15

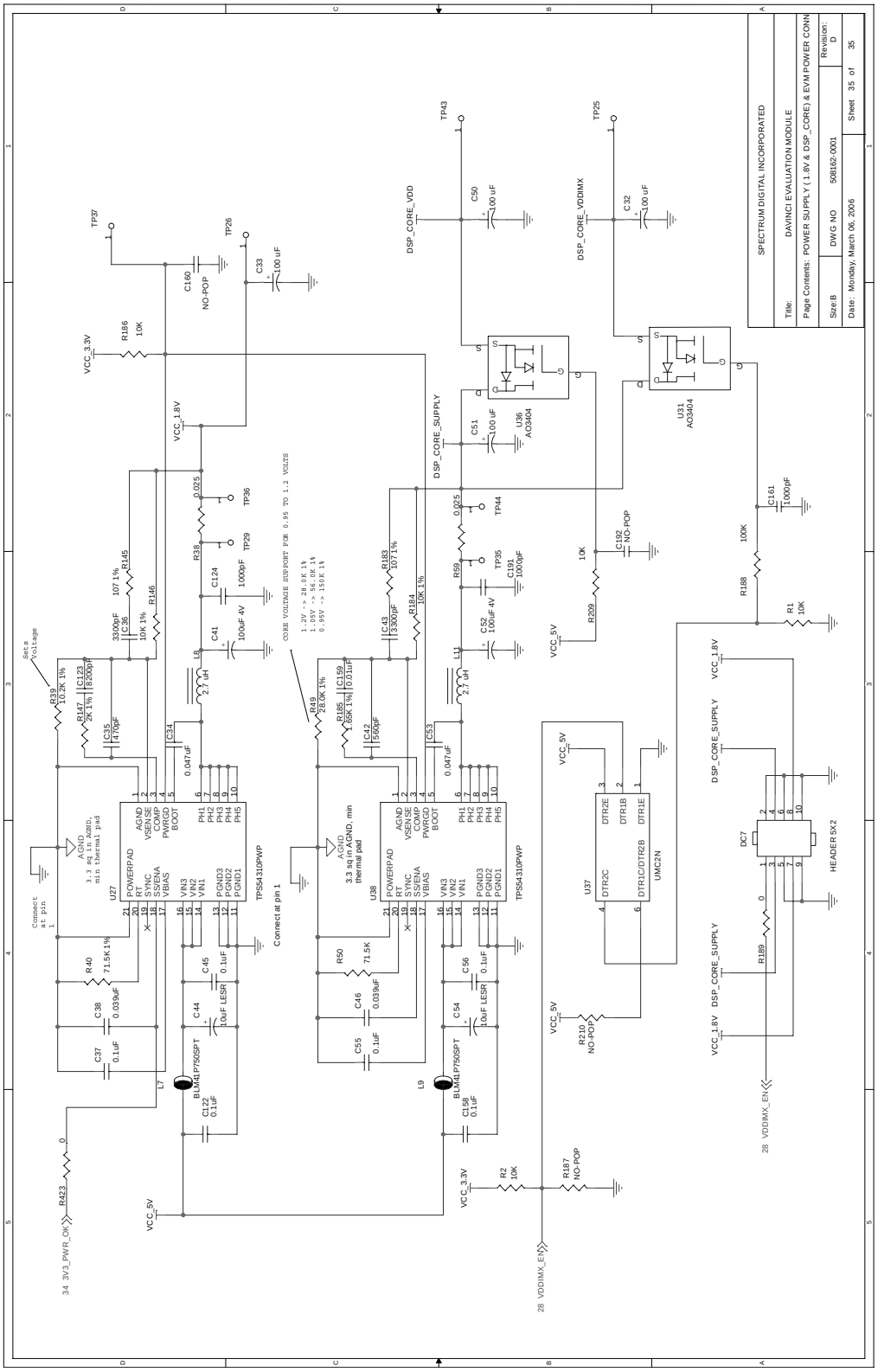

VIDEO INPUT CONNECTOR
VIDEO OUTPUT CONNECTOR
HEADER 25X2
VCC_1.8V
VCC_3.3V
VCC_5V
R225
NO-POP
R268
R267
SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: VIDEO INPUT/OUTPUT CONNECTORS
Size:B
DWG NO 508162-0001
Revision: A
Date: Wednesday, November 16, 2005
Sheet 30 of 35


SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: EMAC/GIO & McBSP/SPI & SD CONNECTORS
Size:B DWG NO 508162-0001 Revision: A
Date: Wednesday, November 16, 2005 Sheet 31 of 35
DC2
HEADER 20X2
DC3
HEADER 15X2
DC6
HEADER 5X2
R263
NO-POP
VCC_3.3V
VCC_5V
VCC_1.8V
GIOV33_0 6,22
GIOV33_1 6,22
GIOV33_2 6,22
GIOV33_3 6,22
GIOV33_4 6,22
GIOV33_5 6,22
GIOV33_6 6,22
GIOV33_7 6,22
GIOV33_8 6,22
GIOV33_9 6,22
GIOV33_10 6,22
GIOV33_11 6,22
GIOV33_12 6,22
GIOV33_13 6,22
GIOV33_14 6,22
GIOV33_15 6,22
ENET_ENABLEz 22
3V3.SYS_RESETz 15,22,24,28
3V3.UART_RXD1 15,28
3V3.UART_TXD1 15,28
SPI_EN0 6
SPI_DO 6
TIMER_IN_DC3 15
DX 7,27
CLKX 7
FSX 7
1V8.I2C_CLK 6,26,30
1V8.I2C_DATA 6,26,30
1.8V_DC3_PCLK 23
SPI_EN1 6
SPI_DI 6
SPI_CLK 6
DR 7
CLKR 7
FSR 7
1.8V,SYS_RESETz 8,13,15,26,29,30,34
McBSP_EN 7
AUDIO_CLK 5,26
SD_CMD 7,16,32
SD_DATA1 7,16,32
SD_DATA3 7,16,32
SD_CLK 7,16,32
SD_DATA0 7,16,32
SD_DATA2 7,16,32


SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: VLYNQ INTERFACE
Size:B
DWG NO 508162-0001
Revision: B
Date: Wednesday, November 16, 2005
Sheet 32 of 35
J16
mPCI
VCC_3.3V
VCC_5V
VCC_1.8V
BLM41P750SPT
NO-POP
SD_DATA0
VLYNQ_SCRUN
VLYNQ_TXD3
VLYNQ_TXD2
VLYNQ_TXD1
VLYNQ_TXD0
VLYNQ_RXD3
VLYNQ_RXD2
VLYNQ_RXD1
VLYNQ_RXD0
SD_CLK
SD_CMD
SD_DATA3
SD_DATA2
SD_DATA1
VLYNQ_CLK
1V8_WLAN_RESET#
WLAN_INTR
Resistors are only populated for modules requiring the upper VLYNQ data pairs
Resistors are only populated for modules requiring the upper VLYNQ data pairs


SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: DAVINCI EMULATION HEADER
Size: B
DWG NO 5082162-0001
Revision: D
Date: Monday, March 06, 2006
Sheet 33 of 35
S2/S1 SETTINGS
TI COMPATABLE EMULATOR
S1 1-2
S1 4-5
S2 1-2
S2 4-5
DSP_EMU0 8
DSP_EMU1 8
VCC_1.8V
VCC_3.3V
R94 39
R93 39
R86 NO-POP
R85 NO-POP
R83 2.2K
R84 2.2K
S1
CAS-20TB
R87 NO-POP
R88 0
R89 0
J1
20 PIN CTI INTERFACE
CTI_EMU1
CTI_EMU0
CTI_TCK
EMULATOR_RST# 34
R95 NO-POP
R92 33
DSP_TCK 8
DSP_TRST# 8
DSP_TDI 8
DSP_TMS 8
C82 NO-POP
S2
CAS-20TB
R82 10K
R81 2.2K
R90 0
R91 0
8 DSP_TDO
8 DSP_RTCK
C81 0.1uF
U1
TPS3808G09DBVR
SENSE# VDD
RESET
CT
MR
GND
C80 NO-POP
R80 10K
R79 10K
34 POR_RST#

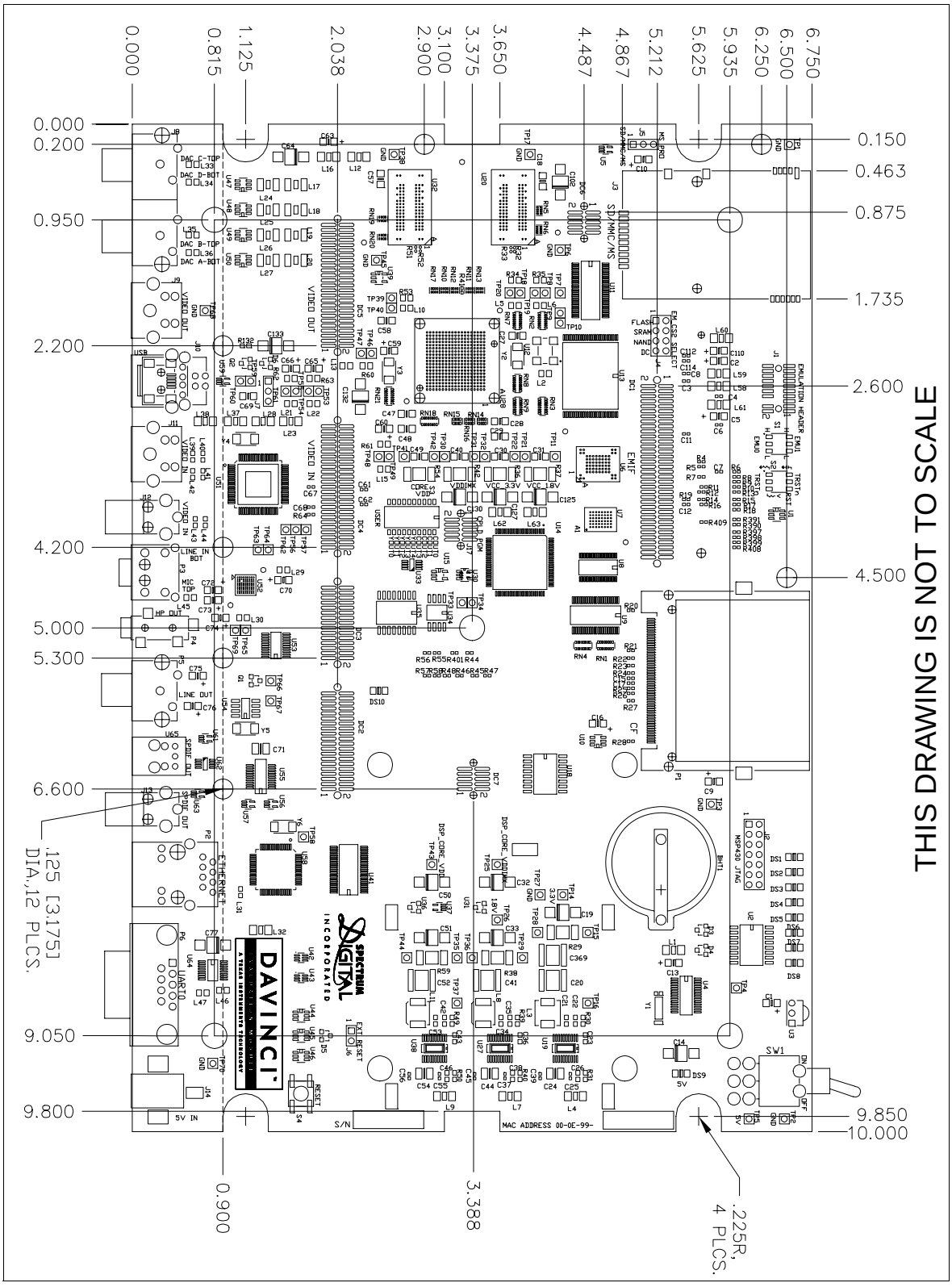

SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: POWER SUPPLY (3.3V) & SYSTEM RESET LOGIC
Size: B
DWG NO 508162-0001
Revision: B
Date: Wednesday, November 16, 2005
Sheet 34 of 35
TPS54310PWP
TPS3808G09DBVR
BAS16.7
BLM41P750SPT
POWERINPUT
J14
2.5 MM JACK
RASM712
SW1
SWITCH
CENTER
SHUNT
SLEEVE
PUSHBUTTON SW
HEADER 2
GREEN
BOX MOUNTING HOLES
CASE SWITCHING TABS FOR POWER SUPPLY
SENSE THRESHOLD FOR TPS3808G01 IS 0.405 VOLTS
SENSE THRESHOLD FOR TPS3808G09 IS 0.840 VOLTS
3.3 EMULATOR_RSTn
POR_RSTz 33
1.8V_SYS_RESETz 8,13,15,26,29,30,31
3V3_PWR_OK 35
3.3V @1.5Amp Max
Connect at pin 1
Bare Voltage
AGND
3.3 amp in AGND, min thermal pad
DSP_CORE_VDD
PBSW_RSTz
NO-POP


SPECTRUM DIGITAL INCORPORATED
Title: DAVINCI EVALUATION MODULE
Page Contents: POWER SUPPLY (1.8V & DSP_CORE) & EVM POWER CONN
Size:B DWG NO 508162-0001 Revision: D
Date: Monday, March 06, 2006 Sheet 35 of 35
TPS54310PWP
U27
U38
U37
UMC2N
U31
AO3404
U36
AO3404
DC7
HEADER 5X2
VCC_3.3V
VCC_1.8V
VCC_5V
DSP_CORE_VDD
DSP_CORE_VDDMX
DSP_CORE_SUPPLY
VDDIMX_EN
CORE VOLTAGE STEPPORT FOR 0.95 TO 1.2 VOLTS
1.2V -> 28.0K 1%
1.05V -> 15.4K 1%
0.95V -> 150K 1%
Set Voltage
Connect at pin 1
NO-POP

Appendix B

Mechanical Information

This appendix contains the mechanical information about the DM644x EVM produced by Spectrum Digital.


0.000
0.815
1.125
2.038
2.900
3.100
3.375
3.650
4.487
4.867
5.212
5.625
5.935
6.250
6.500
6.750
0.000
0.200
0.950
2.200
4.200
5.000
5.300
6.600
9.050
9.800
0.150
0.463
0.875
1.735
2.600
4.500
9.850
10.000
0.900
3.388
.225R, 4 PLCS.
.125 [3.175] DIA,12 PLCS.
THIS DRAWING IS NOT TO SCALE
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A TEXAS INSTRUMENTS TECHNOLOGY
MAC ADDRESS 00-0E-99-
S/N
5V IN
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