

## Audio/video switch matrix

### Features

- I<sup>2</sup>C bus control
- Standby mode with interrupt signal output
- Video section:
  - 3 CVBS inputs, 2 CVBS outputs
  - 3 Y/C inputs, 2 Y/C outputs
  - 6 dB gain on all CVBS/Y and C outputs
  - Integrated 150 Ω buffers
  - 2 RGB/FB inputs, 1 tri-state RGB/FB output with 6 dB adjustable gain (from +3 dB to +9 dB)
  - Video muting on all outputs
  - 2 slow blanking inputs/outputs
  - Sync bottom clamp on all CVBS/Y and RGB inputs, average clamp on C inputs
  - Bandwidth: 15 MHz
  - Crosstalk: 50 dB minimum
- Audio section:
  - 3 stereo inputs, 3 stereo outputs
  - Stereo-to-mono sound capability
  - 0/6/9 dB selectable gain on one stereo input
  - Full range volume control with soft control
  - Audio muting on all outputs



**Table 1. Device summary**

Order code	Packaging
STV6413D	Tray
STV6413CT	Tape and Reel

### Description

The STV6413 is a highly integrated I<sup>2</sup>C bus-controlled audio and video switch matrix, optimized for use in digital set-top box applications. It provides the audio and video routings required in a two SCART set-top box design.

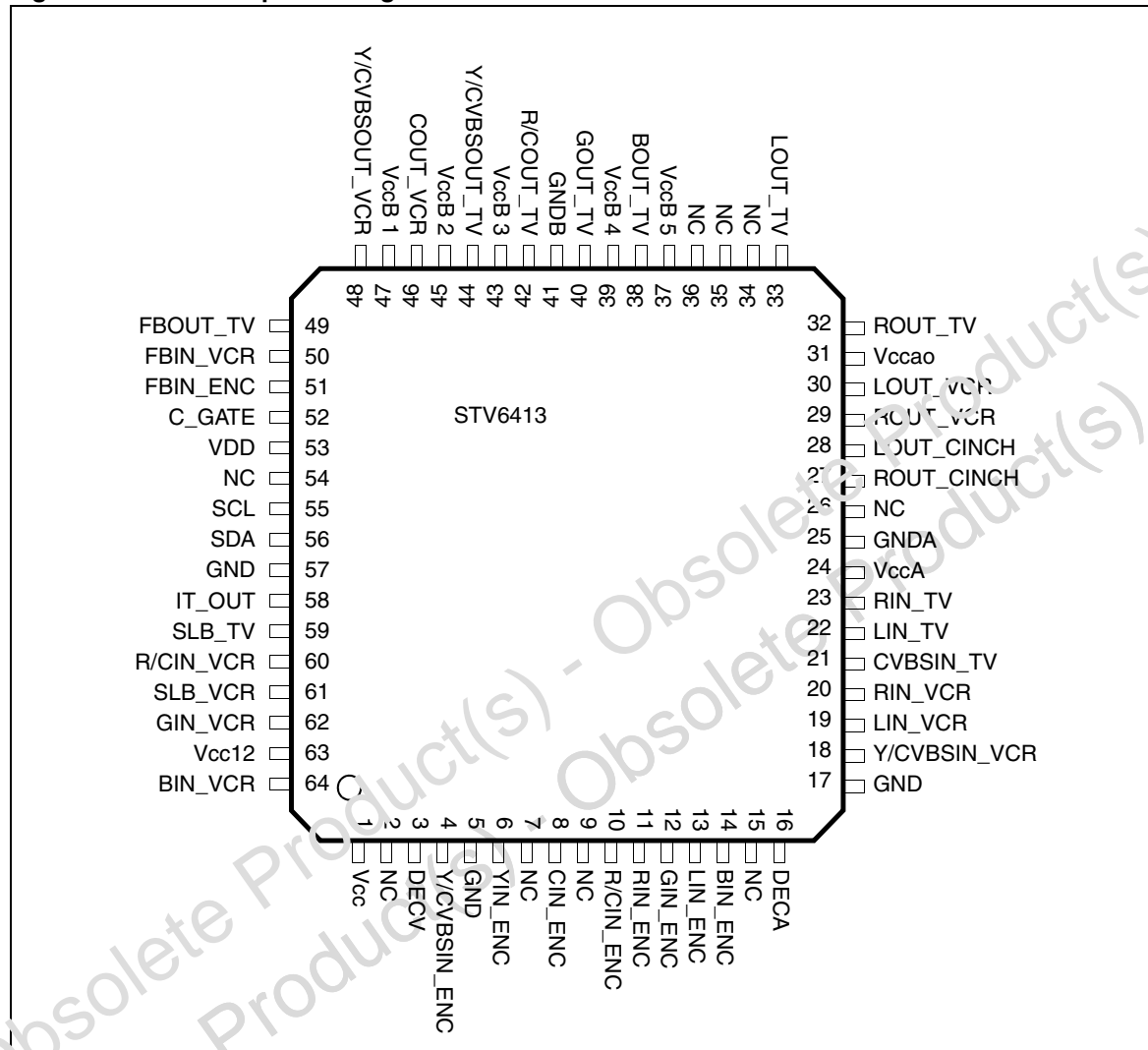
In a TQFP64 (10 x 10 mm) package, the STV6413 is compatible with the STV6412A (TQFP64 14 x 14 mm) used for designing boards with two levels of integration.

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# 1 General information

Figure 1. STV6413 pinout diagram



## 1.1 I/O pin description

Table 2. Pin description

Pin no.	Name	Function
1	Vcc	+5 V Supply
2	NC	Not connected
3	DECV	Video decoupling capacitor
4	Y/CVBSIN_ENC	Y/CVBS input from encoder

Table 2. Pin description (continued)

Pin no.	Name	Function
5	GND	Ground
6	YIN_ENC	Y input from encoder
7	NC	Not connected
8	CIN_ENC	Chroma input from encoder
9	NC	Not connected
10	R/CIN_ENC	Red/Chroma input from encoder
11	RIN_ENC	Audio right, input from encoder
12	GIN_ENC	Green input from encoder
13	LIN_ENC	Audio left, input from encoder
14	BIN_ENC	Blue input from encoder
15	NC	Not connected
16	DECA	Audio decoupling capacitor
17	GND	Ground
18	Y/CVBSIN_VCR	Y/CVBS input from VCR SCART
19	LIN_VCR	Audio left, input from VCR SCART
20	RIN_VCR	Audio right, input from VCR SCART
21	CVBSIN_TV	CVBS input from TV SCART
22	LIN_TV	Audio left, input from TV SCART
23	RIN_TV	Audio right, input from TV SCART
24	VCCA	Audio supply voltage - or - audio supply decoupling
25	GNDA	Audio ground
26	NC	Not connected
27	ROUT_CINCH	Audio right output to CINCH
28	LOUT_CINCH	Audio left output to CINCH
29	ROUT_VCR	Audio right output to VCR SCART
30	LOUT_VCR	Audio left output to VCR SCART
31	VCCAO	Audio output supply voltage - or - main audio supply Voltage
32	ROUT_TV	Audio right output to TV SCART
33	LOUT_TV	Audio left output to TV SCART
34	NC	Not connected
35	NC	Not connected
36	NC	Not connected
37	VCCB5	Video output buffer supply pin
38	BOUT_TV	Blue output to TV SCART
39	VCCB4	Video output buffer supply pin

**Table 2. Pin description (continued)**

Pin no.	Name	Function
40	GOUT_TV	Green output to TV SCART
41	GNDB	Video buffer ground
42	R/COUT_TV	Red/Chroma output to TV SCART
43	VCCB3	Video output buffer supply pin
44	Y/CVBSOUT_TV	Y/CVBS output to TV SCART
45	VCCB2	Video output buffer supply pin
46	COUT_VCR	Chroma output to VCR SCART
47	VCCB1	Video output buffer supply pin
48	Y/CVBSOUT_VCR	Y/CVBS output to VCR SCART
49	FBOUT_TV	Fast blanking output to TV SCART
50	FBIN_VCR	Fast blanking input from VCR SCART
51	FBIN_ENC	Fast blanking input from encoder
52	C_GATE	External MOS command for C_VCR bidirectional mode
53	VDD	+5 V I <sup>2</sup> C supply
54	NC	Not connected
55	SCL	I <sup>2</sup> C bus clock
56	SDA	I <sup>2</sup> C bus data
57	GND	Ground digital
58	IT_OUT	Interrupt output
59	SLB_TV	Slow blanking input/output from TV SCART
60	R/CIN_VCR	Red input (or C Input) from VCR SCART
61	SLB_VCR	Slow blanking input/output from VCR SCART
62	GIN_VCR	Green input from VCR SCART
63	VCC12	+12 V supply
64	BIN_VCR	Blue input from VCR SCART

Figure 2. STV6413 block diagram

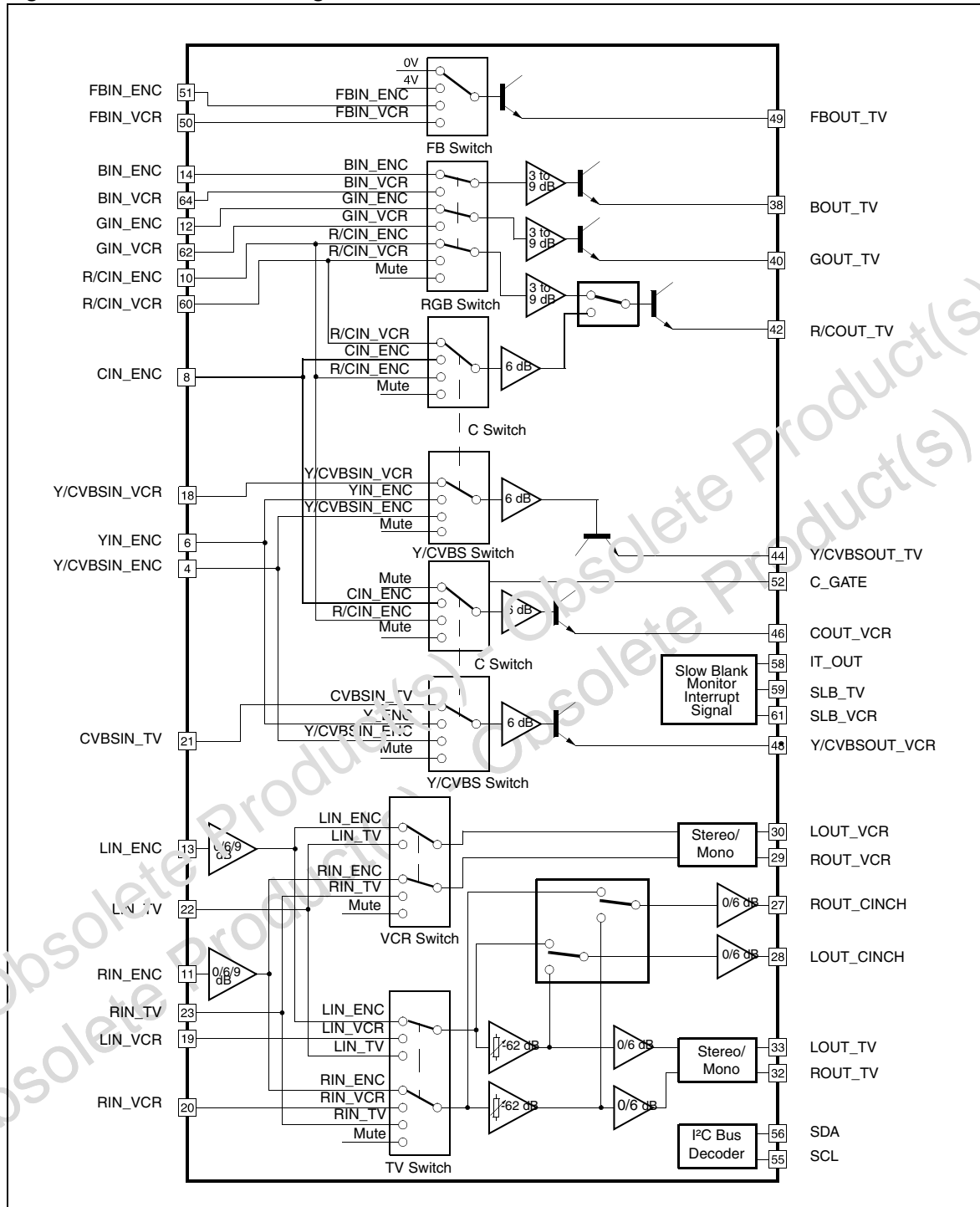
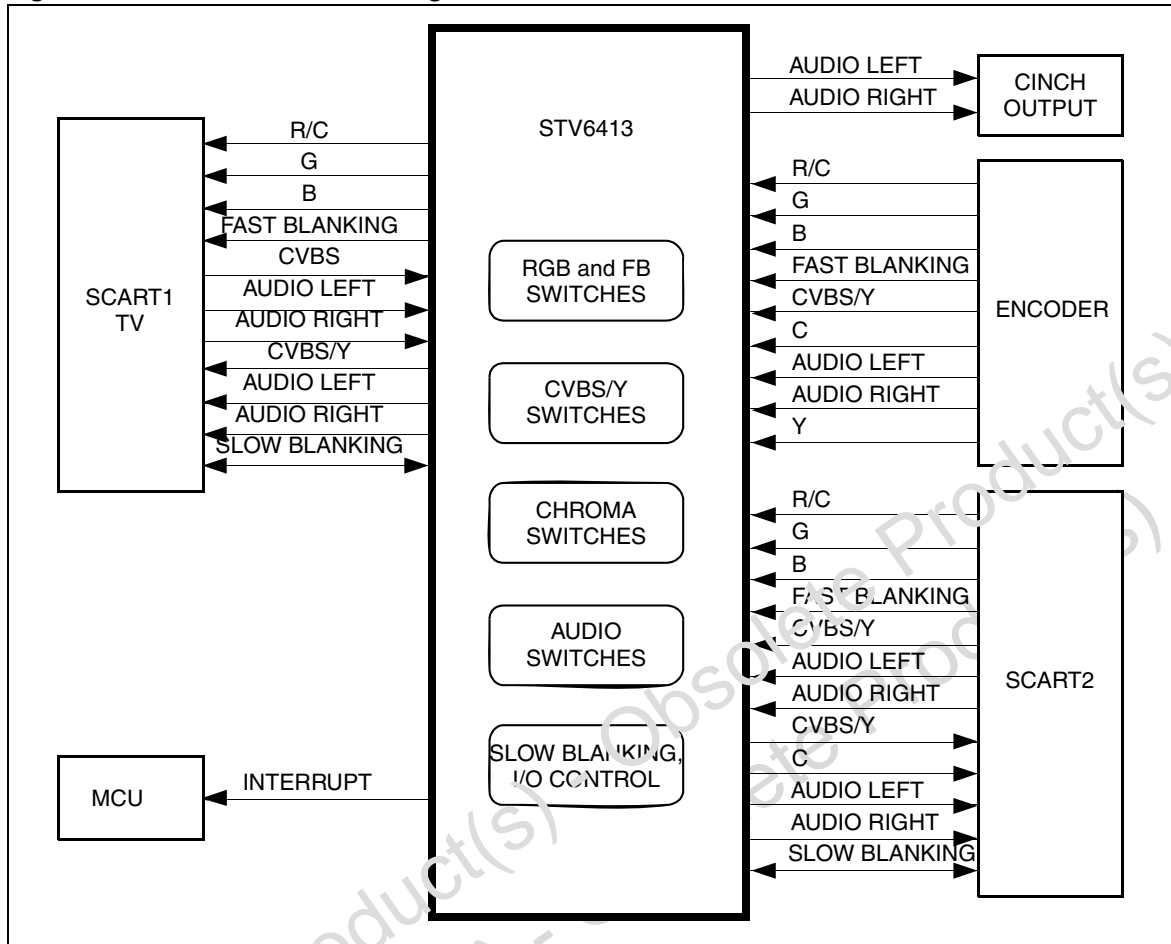


Figure 3. STV6413 functional diagram



Obsolete Product(s)  
 Obsolete Product(s)

## 2 Electrical characteristics

### 2.1 Absolute maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Parameter		Value	Unit
$V_{CC12}$	Supply voltage for slow blanking sections		13.2	V
$V_{CCAO}$	Supply voltage for audio drivers		13.2	V
$V_{CCA}$	Supply voltage for digital audio sections		10	V
$V_{DD}$	Supply voltage for digital sections		6	V
$V_{CC}, V_{CCB1}$	Supply voltage for video sections		6	V
$V_{IN}$	Input voltage at pin (in reference to GND)	Audio pins Video pins Bus pins Slow blanking pins	0, $V_{CCA}$ 0, $V_{CC}$ or $V_{CCB1}$ 0 to 5 0, $V_{CC12}$	V
$V_{ESD}$	Maximum ESD voltage allowed. (human body model: 100 pF capacitor discharged through 1.5 k $\Omega$ serial resistor)		$\pm 4$	kV
$T_{OPER}$	Ambient operating temperature		0 to +70	$^{\circ}\text{C}$
$T_{STG}$	Storage temperature		-20 to +150	$^{\circ}\text{C}$

### 2.2 Thermal data

**Table 4. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Junction-to-case thermal resistance	8.2	$^{\circ}\text{C}/\text{W}$
$R_{thJA}$	Junction-to-ambient thermal resistance <sup>(1)</sup>	48	$^{\circ}\text{C}/\text{W}$
$T_J$	Maximum junction temperature	150	$^{\circ}\text{C}$

1. Measured on 4-layer application board.

### 2.3 Latch-up data

At an ambient temperature of 25  $^{\circ}\text{C}$ , all pins meet the following specifications:

- $I_{trigger} = 200 \text{ mA}$  or  $I_{trigger} = -200 \text{ mA}$ .
- Pin 58 (IT\_OUT) does not meet this specification and the trigger current must be limited to 100 mA.



## 2.4 Electrical characteristics

$T_{AMB} = 25^{\circ}C$ ,  $V_{CCA0} = 12V$ ,  $V_{CC} = 5V$ ,  $V_{CC12} = 12V$ ,  $V_{DD} = 5V$

$R_{GA} = 600\ \Omega$ ,  $R_{GV} = 50\ \Omega$ ,  $R_{LOUTA} = 10\ k\Omega$ ,  $R_{LOUTV} = 150\ \Omega$  (unless otherwise specified).

**Table 5. Supply section**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{DD}$	Digital supply voltage		4.75	5	5.25	V
$V_{CCA0}$	Audio operating supply voltage	- Decoupling capacitor on $V_{CCA}$ - Connected to $V_{CCA}$	11.2 8.5	12 9	12.8 9.5	V
$V_{CC}$	Video operating supply voltage		4.75	5	5.25	V
$V_{CC12}$	Slow blanking control supply voltage		11.2	12	12.8	V

**Table 6. Active mode (all channels ON)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{DD}$	Digital supply current	$V_{DD} = 5V$		4.5	10	mA
$I_{CCA}$	Audio supply current	$V_{CCA0} = 12V$ , no load		9	15	mA
$I_{CCV}$	Total video supply current ( $V_{CC} + V_{CCB1} + V_{CCB2} + V_{CCB3} + V_{CCB4} + V_{CCB5}$ )	$V_{CC} = 5V$ , no load		43	60	mA
$I_{CC12}$	12 V supply current	$V_{CC12} = 12V$ SLB input mode SLB output mode, no load		0 2.5	1 4	mA

**Table 7. Standby mode (all channels OFF)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{DD}$	Digital supply current	$V_{DD} = 5V$		4.5	10	mA
$I_{CCASTD}$	Audio supply current	$V_{CCA0} = 12V$ , no load		3		mA
$I_{CCVSTD}$	Total video supply current	$V_{CC} = 5V$ , no load		1		mA

**Table 8. Audio section**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SVR100	Supply voltage rejection	$V_{RIPPLE} = 500\ mV_{RMS}$ at 100 Hz, gain = 0 dB DECA filter cap = 47 $\mu F$ DECA filter cap = 220 $\mu F$	60	70 80		dB
SVR1K	Supply voltage rejection	$V_{RIPPLE} = 500\ mV_{RMS}$ at 1 kHz, gain = 0 dB	70	80		dB
$V_{INDC}$	Input DC level	$V_{CCA} = 9V$		$V_{CCA}/2$		V

Table 8. Audio section (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{INAC}$	Input signal amplitude				2	$V_{RMS}$
$R_{IN}$	Input resistance		30	50		$k\Omega$
$R_{INmatch}$	Input resistance matching			$\pm 2$	$\pm 10$	%
$F_{RANGE}$	Bandwidth	-3 dB, $0.5 V_{RMS}$ , $R_{LOAD} = 10 k\Omega$ , gain = 0 dB	50			kHz
Flatness	Spread of gain in audio band	-0.5 $V_{RMS}$ , 20 Hz to 20 kHz, gain = 0 dB			0.5	dB
CS	Channel separation, from audio inputs between L & R of TV outputs	$V_{IN} = 0.5 V_{RMS}$ at 1 kHz on one input, $R_{LOAD} = 10 k\Omega$ , gain = 0 dB	80 70	90 74		dB
$C_i$	Channel isolation from video inputs	$V_{IN} = 1 V_{PP}$ at 15 kHz on one point		85		dB
$V_{OUT}$	Output DC level	$V_{CCA} = 9 V$		$V_{CC}/2$		V
$V_{OFF}$	DC offset change	Switching between inputs		1	$\pm 15$	mV
$R_{OUT}$	Output resistance			60	120	$\Omega$
PHD	Phase difference	1 $V_{RMS}$ input on each input channel at 1 kHz			3	$^{\circ}$ deg.
ASN	S/N ratio	$V_{IN} = 1 V_{RMS}$ at 1 kHz input weighted CCIT, 168-4 quasi peak, gain = 0 dB	80	90		dB
eNI	Equivalent RMS input voltage noise	BW = 20 Hz, 20 kHz flat, gain = 0 dB		5		$\mu V$
G0	0 dB gain	$0.5 V_{RMS}$ , $R_{LOAD} = 10 k\Omega$ , gain = 0 dB	-0.5		+0.5	dB
$G_{STEP}$	Gain step	-62 dB to +6 dB (see Figure 2)		2		dB
$G_{MATCH1}$	Gain matching between different inputs of one output	$V_{IN} = 0.5 V_{RMS}$ at 1 kHz, gain = 0 dB	-0.5		0.5	dB
$G_{MATCH2}$	Gain matching between left/right outputs of one input channel	$V_{IN} = 0.5 V_{RMS}$ at 1 kHz, gain = 0 dB	-0.5		0.5	dB
THD0 THD6 THD9	Total harmonic distortion ENC Input at 0 dB ENC Input at 6 dB ENC Input at 9 dB	$V_{OUT} = 0.5 V_{RMS}$ at 1 kHz, LPF at 80 kHz, volume level adjustment = 0 dB		0.01 0.01 0.01	0.05 0.05 0.05	%
$V_{CL}$	Output clipping level	THD = 0.2%, 1 kHz	2.1	2.3		$V_{RMS}$
$R_L$	Output load resistance	$V_{IN} = 1 V_{RMS}$ , THD = 0.3%, gain = 0 dB	2	2.25		$k\Omega$
Mute	Mute suppression	$V_{IN} = 0.5 V_{RMS}$ , on one point	90			dB

Table 9. Video section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{DCIN}$	DC input level	Bottom sync pulse		2		V
$I_{CLAMP}$	Clamping current	at $V_{DCIN} - 400$ mV	1	2		mA
$I_{LEAK}$	Input leakage current	$V_{IN} = V_{DCIN} + 1$ V		1	10	$\mu$ A
$C_{IN}$	Input capacitance			2		pF
$V_{IN}$	Max input signal	$V_{CC} = 5$ V		1.5		$V_{PP}$
DYN	Dynamic output signal	$V_{CC} = 5$ V		3		$V_{PP}$
BW	Bandwidth at -3 dB - Y/CVBS - RGB	$V_{IN} = 1 V_{PP}$ $V_{IN} = 1 V_{PP} V_{INC} =$ muted	12 12	15 15		MHz
Flatness	Spread of gain in video band (15 kHz - 5 MHz) - Y/CVBS - RGB	$V_{IN} = 1 V_{PP}$ $V_{IN} = 1 V_{PP} V_{INC} =$ muted			-0.5 $\pm 0.5$	dB
CTi	Crosstalk isolation between input channel	$V_{IN} = 1 V_{PP}$ at 4.43 MHz on one point		60		dB
CTo	Crosstalk isolation between output channel	$V_{IN} = 1 V_{PP}$ at $f = 4.43$ MHz, on one point, $R_{LOAD} = 150\Omega$		50		dB
$R_{OUT}$	Output resistance			5	10	$\Omega$
$G_{RGB}$	Gain at RGB outputs	$V_{IN} = 1 V_{PP}$ , gain = 6 dB	5.5	6	6.5	dB
$G_{RGBM}$	Gain matching between R, G, B	$V_{IN} = 1 V_{PP}$ , gain = 6 dB	-0.3	0	0.3	dB
$G_{RGBSTEP}$	Step of gain	3 dB to 6 dB	0.75	1	1.25	dB
$G_{YCVBS}$	Gain on Y/CVBS channels	$V_{IN} = 1 V_{PP}$	5.5	6	6.5	dB
$G_{YCVBSM}$	Gain matching between Y, CVBS inputs	$V_{IN} = 1 V_{PP}$	-0.5	0	0.5	dB
$DC_{OUT}$	DC output voltage	Bottom sync pulse		0.6		V
DPHI	Differential phase	$V_{IN} = 1 V_{PP}$ at 4.43 MHz		1	5	$^{\circ}$ deg.
DG	Differential gain	$V_{IN} = 1 V_{PP}$ at 4.43 MHz		1	5	%
Mute	Mute suppression	$V_{IN} = 1 V_{PP}$ at 5 MHz on one point	55			dB
LNL	Luminance non-linearity			0.3	3	%
VSN	Video S/N ratio	Refer to <a href="#">Note 1</a>	65			dB

Note: 1  $S/N = 20 \log (V_{OUT} \text{ Black to White} = 0.7 V_{PP} / V_{Noise} (mV_{RMS}) \text{ weighted CCIR 567})$ .

Table 10. Chroma section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>DCIN</sub>	DC input level			3		V
R <sub>IN</sub>	Input resistance		30	50		kΩ
C <sub>IN</sub>	Input capacitance			2		pF
V <sub>IN</sub>	Max input signal			1.5		V <sub>PP</sub>
DYN	Dynamic output signal			3		V <sub>PP</sub>
DC <sub>OUT</sub>	DC output VCR voltage			2.2		V
CBW	Chroma bandwidth	C <sub>IN</sub> = 1 V <sub>PP</sub> at -3 db	10			MHz
CTi	Crosstalk Isolation between input channel	V <sub>IN</sub> = 1 V <sub>PP</sub> at 4.43 MHz on one input		55		dB
CTo	Crosstalk Isolation between output channel	V <sub>IN</sub> = 1 V <sub>PP</sub> at 4.43 MHz on one input, R <sub>LOAD</sub> = 150 Ω		50		dB
R <sub>OUT</sub>	Output resistance			5	10	Ω
G <sub>OUTC</sub>	Gain at OUTC	V <sub>IN</sub> = 1 V <sub>PP</sub>	5.5	6	6.5	dB
G <sub>CM</sub>	Gain matching between C inputs	V <sub>IN</sub> = 1 V <sub>PP</sub>	-0.5	0	0.5	dB
Mute	Mute suppression	V <sub>IN</sub> = 1 V <sub>PP</sub> at 4.43 MHz on one input	55			dB
CToYdel	Chroma to luma delay, source Y/C	V <sub>PP</sub> at 4.43 MHz			20	ns
CToYdel	Chroma to luma delay, source Y/C				20	ns

Table 11. Slow blanking section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
<b>Input mode</b>						
SLBlow	Input low level threshold		2.5	3.25	4	V
SLBhigh	Input high level threshold		7.5	8.25	9	V
I <sub>IN</sub>	Input current			50	100	μA
<b>Output mode</b>						
SLBlow	Output low level (Int. TV)		0	0.02	1.5	V
SLBmed	Output medium level (ext. 16:9)		5	5.75	6.5	V
SLBhigh	Output high level (ext. 4:3)		10	11	12	V

**Table 12. Fast blanking section**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
<b>Input mode</b>						
FB <sub>low/high</sub>	Input low/high level threshold		0.4	0.7	0.9	V
I <sub>IN</sub>	Input current			2	10	μA
<b>Output mode</b>						
FB <sub>LOW</sub>	Output low level	R <sub>LOAD</sub> = 150 Ω			0.5	V
FB <sub>HIGH</sub>	Output high Level		3.0	3.4	3.8	V
FB <sub>DEL</sub>	Fast blanking RGB delay	At 50% on digital RGB transients, at 2 V on FB rise transient, at 1 V on FB fall, C <sub>LOAD</sub> = 10pF maximum		15		ns
FB <sub>TRANS</sub>	FB transitions at FB output - Rise time - Fall time	C <sub>LOAD</sub> = 10 pF maximum between 10% and 90% between 90% and 10%		10 10		ns

**Table 13. C\_Gate function output section**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_GATE-H	Pull-up resistor value to V <sub>CCB1</sub>			20		kΩ
C_GATE-L	Output low level	I <sub>IN</sub> = 0 mA I <sub>IN</sub> = 1 mA			0.3 0.7	V

**Table 14. Interrupt output section**Refer to [Note 1](#).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
IT-Leak	High level leakage	External pull-up to 5 V			10	μA
IT-Low	Output low level (active)	I <sub>IN</sub> = 0 mA I <sub>IN</sub> = 1 mA			0.3 0.7	V

*Note 1: The interrupt is forced low when a change is detected on slow blanking inputs. It can be used in standby mode to wake up the microprocessor. It is released when the I<sup>2</sup>C bus register is read.*

Table 15. I<sup>2</sup>C bus characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
<b>SCL</b>						
V <sub>IL</sub>	Low level input voltage		-0.3		1.5	V
V <sub>IH</sub>	High level input voltage		2.3		5.5	V
I <sub>LI</sub>	Input leakage current	V <sub>IN</sub> = 0 to 5.5 V	-10	0	10	μA
<b>SDA</b>						
V <sub>IL</sub>	Low level input voltage		-0.3		1.5	V
V <sub>IH</sub>	High level input voltage		2.3		5.5	V
I <sub>LI</sub>	Input leakage current	V <sub>IN</sub> = 0 to 5.5 V	-10	0	10	μA
C <sub>I</sub>	Input capacitance				10	pF
t <sub>R</sub>	Input rise time	1.5 V to 3 V			1	μs
t <sub>F</sub>	Input fall time	3 V to 1.5 V			300	ns
V <sub>OL</sub>	Low level output voltage	I <sub>OL</sub> = 3 mA			0.4	V
t <sub>F</sub>	Output fall time	3 V to 1.5 V			250	ns
C <sub>L</sub>	Load capacitance				400	pF
<b>Timing</b>						
t <sub>LOW</sub>	Clock low period		4.7			μs
t <sub>HIGH</sub>	Clock high period		4			μs
t <sub>SU,DAT</sub>	Data setup time		250			ns
t <sub>HD,DAT</sub>	Data hold time		0		340	ns
t <sub>SU,STO</sub>	Setup time from clock high to stop		4			μs
t <sub>BUF</sub>	Start setup time following a stop		4.7			μs
t <sub>HD,STA</sub>	Start Hold Time		4			μs
t <sub>SU,STA</sub>	Start setup time following clock low to high transition		4.7			μs

### 3 I<sup>2</sup>C bus selection

Data transfers follow the usual I<sup>2</sup>C format; i.e. after the start condition (S), a 7-bit slave address is sent, followed by an eight-bit data direction bit (W). An 8-bit sub-address is sent to select a register, followed by an 8-bit data word to be included in the register. The IC's I<sup>2</sup>C bus decoder enables the automatic incrementation mode in write mode.

#### String format

Write only mode (S = Start condition, P = Stop condition, A = Acknowledge)

S	Slave Address	0	A	Sub-address	A	Data	A	P
---	---------------	---	---	-------------	---	------	---	---

#### Read only mode

S	Slave Address	1	A	Data	A	P
---	---------------	---	---	------	---	---

#### Slave address

Address	A7	A6	A5	A4	A3	A2	A1
Value	1	0	0	1	0	1	1

#### Auto increment mode

S	Slave address	0	A	Sub-address	A	Data0	A	Data1	A	...	Data n	A	P
						Sub-address		Sub-address + 1			Sub-address + N		

### 3.1 I<sup>2</sup>C bus addresses

Write address: 1001 0110 = 96(hex), read address: 1001 0111 = 97(hex)

Table 16. Input signal summary (write mode)

Reg. addr. (hex)	Data							
	d7	d6	d5	d4	d3	d2	d1	d0
<b>Audio</b>								
00h	TV stereo mono	TV 0/6 dB	TV volume-62 dB to 0 dB - 2 dB steps					Soft volume mode
01h	VCR stereo mono	Not used (See Note 1)	VCR audio switch control	CINCH audio gain	TV/CINCH audio switch control			
<b>Video</b>								
02h	VCR chroma muted	VCR video and chroma switch control		TV chroma muted	TV video and chroma switch control			

**Table 16. Input signal summary (write mode) (continued)**

Reg. add. (hex)	Data							
	d7	d6	d5	d4	d3	d2	d1	d0
03h	RGB and FB tri-state	RGB gain			RGB switch control		Fast blanking mode/input selection	
<b>Miscellaneous</b>								
04h	IT enable	SLB mode	Not used (see <a href="#">Note 1</a> )	VCR-C output control	VCR-C gate control	Not used (see <a href="#">Note 1</a> )	Not used (see <a href="#">Note 1</a> )	TV R or C output selection
05h	VCR slow blanking		TV slow blanking		ENC audio input gain 0/6/9 dB		VCR R/C sub clamp	ENC R/C sub clamp
<b>Standby</b>								
06h	Not used (see <a href="#">Note 1</a> )	TV outputs	CINCH outputs	VCR outputs	Not used (see <a href="#">Note 1</a> )	TV inputs	V.C.F. inputs	ENC inputs

Note: 1 At register address 06h, bits marked "Not used" must be set to "1". All other bits marked "Not used" must be set "0".

**Table 17. TV audio output**

Reg. add. (hex)	Description	Bits	Data							Comments	
			d7	d6	d5	d4	d3	d2	d1		d0
00h	Soft volume change	1	X X	X X	X X	X X	X X	X X	X X	0 1	Active Disabled
	Level adjustment	5	X X	X X	0 1	0 1	0 1	0 1	0 1	X X	0 dB -62 dB (-2 dB/step)
	6 dB extra gain	1	X X	0 1	X X	X X	X X	X X	X X	X X	0 dB +6 dB
	TV stereo or mono mode	1	0 1	X X	X X	X X	X X	X X	X X	X X	0 = stereo 1 = mono



Table 18. Audio selection &amp; VCR audio output

Reg. add. (hex)	Description	Bits	Data							Comments	
			d7	d6	d5	d4	d3	d2	d1		d0
01h	TV & CINCH audio output selection	3	X	X	X	X	X	0	0	0	Muted
			X	X	X	X	X	0	0	1	Encoder L/R selected
			X	X	X	X	X	0	1	0	VCR L/R selected
			X	X	X	X	X	0	1	1	Not allowed
			X	X	X	X	X	1	0	0	TV L/R selected
			X	X	X	X	X	1	0	1	Not allowed
			X	X	X	X	X	1	1	0	Not allowed
	CINCH audio gain	1	X	X	X	X	0	X	X	X	0 dB
			X	X	X	X	1	X	X	X	Follow TV Gain
	VCR audio output selection	2	X	X	0	0	X	X	X	X	Muted
			X	X	0	1	X	X	X	X	Encoder L/R selected
			X	X	1	0	X	X	X	X	TV L/R selected
			X	X	1	1	X	X	X	X	Not allowed
	VCR stereo or mono mode	1	0	X	X	X	X	X	X	X	0 = stereo
			1	X	X	X	X	X	X	X	1 = mono

Table 19. TV &amp; VCR video selection

Reg. add. (hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
02h	TV video output selection	3	X	X	X	X	X	0	0	0	Y/CVBS muted & chroma muted
			X	X	X	X	X	0	0	1	Y/CVBS_ENC & R/C_ENC
			X	X	X	X	X	0	1	0	Y_ENC & C_ENC
			X	X	X	X	X	0	1	1	Y/CVBS_VCR & R/C_VCR
			X	X	X	X	X	1	0	0	R/C_VCR
			X	X	X	X	X	1	0	1	Not allowed
			X	X	X	X	X	1	1	0	Not allowed
			X	X	X	X	X	1	1	1	Not allowed
	TV chroma output control	1	X	X	X	X	0	X	X	X	Chroma defined by d2d1d0
			X	X	X	X	1	X	X	X	Chroma force to mute
VCR video output selection	3	X	0	0	0	X	X	X	X	Y/CVBS muted & chroma muted	
		X	0	0	1	X	X	X	X	Y/CVBS_ENC & R/C_ENC	
		X	0	1	0	X	X	X	X	Y_ENC & C_ENC	
		X	0	1	1	X	X	X	X	CVBS_TV & chroma muted	
		X	1	0	0	X	X	X	X	Not allowed	
		X	1	0	1	X	X	X	X	Not allowed	
		X	1	1	1	X	X	X	X	Not allowed	
VCR chroma output control	1	0	X	X	X	X	X	X	X	Chroma defined by d6d5d4	
		1	X	X	X	X	X	X	X	Chroma force to mute	

Table 20. RGB &amp; fast blanking outputs

Reg. add. (hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
03h	Fast blanking control	2	X	X	X	X	X	X	0	0	FB forced to low level
			X	X	X	X	X	X	0	1	FB forced to high level
			X	X	X	X	X	X	1	0	FB from Encoder
			X	X	X	X	X	X	1	1	FB from VCR
	RGB selection	2	X	X	X	X	0	0	X	X	Muted
			X	X	X	X	0	1	X	X	RGB_ENC selected
			X	X	X	X	1	0	X	X	RGB_VCR selected
			X	X	X	X	1	1	X	X	Not allowed
	RGB gain	2	X	X	0	0	X	X	X	X	+6 dB gain
			X	X	0	1	X	X	X	X	+5 dB gain
			X	X	1	0	X	X	X	X	+4 dB gain
			X	X	1	1	X	X	X	X	+3 dB gain
	RGB gain	1	X	0	X	X	X	X	X	X	+0 dB extra gain
			X	1	X	X	X	X	X	X	+3 dB for weak input signals
	RGB and FB control	1	0	X	X	X	X	X	X	X	RGB and FB outputs high impedance state
			1	X	X	X	X	X	X	X	RGB and FB outputs active

Table 21. Miscellaneous Control

Reg. add. (hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
04h	R/C TV output selection	1	X	X	X	X	X	0	0	0	Red signal selected
			X	X	X	X	X	0	0	1	Chroma signal selected
	C_gate output control	1	X	X	X	X	0	0	0	X	High level
			X	X	X	X	1	0	0	X	Low level
	C_VCF output control	1	X	X	X	0	X	0	0	X	Tri-state mode (high impedance)
			X	X	X	1	X	0	0	X	Active
	Slow blanking mode	1	X	0	X	X	X	0	0	X	Normal mode
			X	1	X	X	X	0	0	X	SLB TV is driven by SLB VCR
	IT enable	1	0	X	X	X	X	0	0	X	No interrupt flag
			1	X	X	X	X	0	0	X	IT enable

Table 22. Slow blanking &amp; inputs control

Reg. add. (hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
05h	Encoder R/Csub clamp	1	X X	X X	X X	X X	X X	X X	X X	0 1	Bottom level clamp Average level clamp
	VCR R/Csub clamp	1	X X	X X	X X	X X	X X	X X	0 1	X X	Bottom level clamp Average level clamp
	Encoder input level adjustment	2	X X X	X X X	X X X	X X X	0 0 1	0 1 0	X X X	X X X	0 dB for normal audio inputs +6 dB for weak audio inputs +9 dB for weak audio inputs
	Slow blanking TV SCART	2	X X X X	X X X X	0 0 1 1	0 1 0 1	X X X X	X X X X	X X X X	X X X X	Input mode only Output < 2 V Output 16/9 format Output 4/3 format
	Slow blanking VCR SCART	2	0 0 1 1	0 1 0 1	X X X X	X X X X	X X X X	X X X X	X X X X	X X X X	Input mode only Output < 2 V Output 16/9 format Output 4/3 format

Table 23. Standby modes

Reg. add. (hex)	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
06h	ENC inputs	1	1 1	X X	X X	X X	1 1	X X	X X	0 1	Inputs active Inputs disabled
	VCR inputs	1	1 1	X X	X X	X X	1 1	X X	0 1	X X	Inputs active Inputs disabled
	TV inputs	1	1 1	X X	X X	X X	1 1	0 1	X X	X X	Inputs active Inputs disabled
	VCR outputs	1	1 1	X X	X X	0 1	1 1	X X	X X	X X	Audio & video outputs ON Audio & video outputs OFF
	CINCH outputs	1	1 1	X X	0 1	X X	1 1	X X	X X	X X	Audio & video outputs ON Audio & video outputs OFF
	TV outputs	1	1 1	0 1	X X	X X	1 1	X X	X X	X X	Audio & video outputs ON Audio & video outputs OFF
	Full stop		1	1	1	1	1	1	1	1	1

Table 24. Output signals (read mode)

Reg. Add.	Description	Bits	Data								Comments
			d7	d6	d5	d4	d3	d2	d1	d0	
	Slow blanking TV SCART	2	X	X	X	X	X	X	0	1	Input < 2 V Input 16/9 format Input 4/3 format
	Slow blanking VCR SCART	2	X	X	X	X	0	1	X	X	Input < 2 V Input 16/9 format Input 4/3 format
	Interrupt flag	1	X	X	X	0	X	X	X	X	No change since read One change has been detected (refer to <a href="#">Note 1</a> )

Note: 1 The interrupt flag will be cleared when this register is read. To prepare for a new interrupt, a "1" must be re-written in the IT Enable bit (Reg. 04, d7).

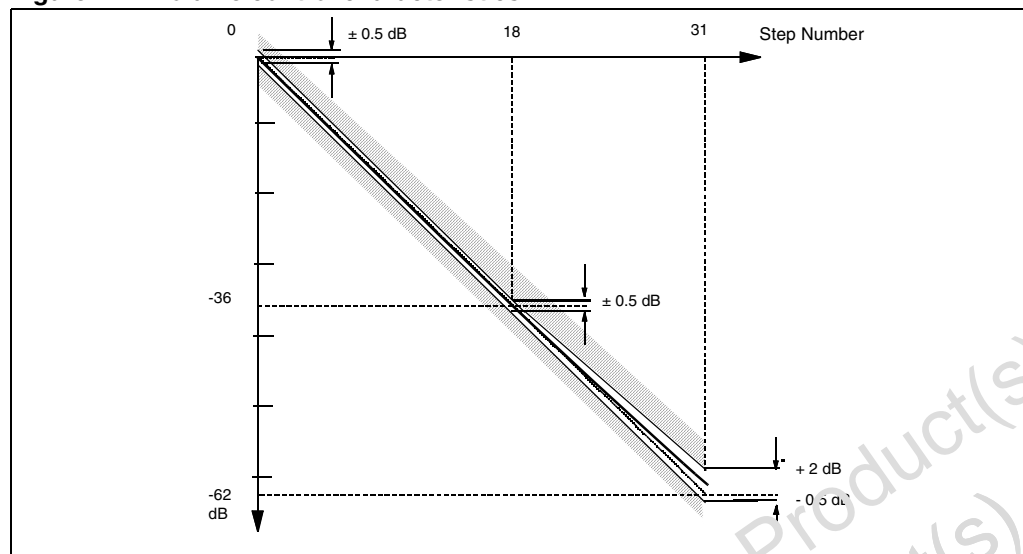
### 3.2 Power-on reset — bus register initial conditions

Power-on reset is active when the supply V<sub>DD</sub> is less than 3.5 volts. Non-significant bits (X) are pre-set to "0"

Table 25. Power on reset

Reg. add. (hex)	Data								Comments
	d7	d6	d5	d4	d3	d2	d1	d0	
00h	0	0	0	0	0	0	0	0	Audio TV and CINCH outputs are in stereo mode, 0 dB gain adjustment.
01h	0	0	0	0	0	0	0	0	TV, CINCH and VCR audio outputs are muted. VCR output is in stereo mode.
02h	0	0	0	0	0	0	0	0	VCR, TV video outputs are muted.
03h	0	0	0	0	0	0	0	0	Fast blanking is forced to '0'. RGB outputs are muted and in high impedance.
04h	0	0	0	0	0	0	0	0	C_GATE is high. C_VCR is high impedance.
05h	0	0	0	0	0	0	0	0	Encoder and VCR R/Csub bottom level clamp, RGB outputs 6 dB gain, and slow blanking parts are in read mode.
06h	0	0	0	0	0	0	0	0	All internal blocks are ON.

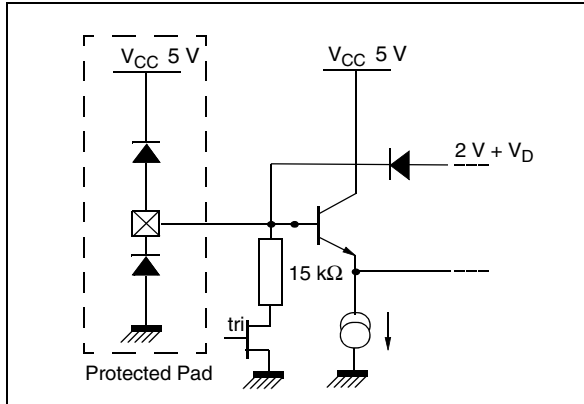
Figure 4. Volume control characteristics



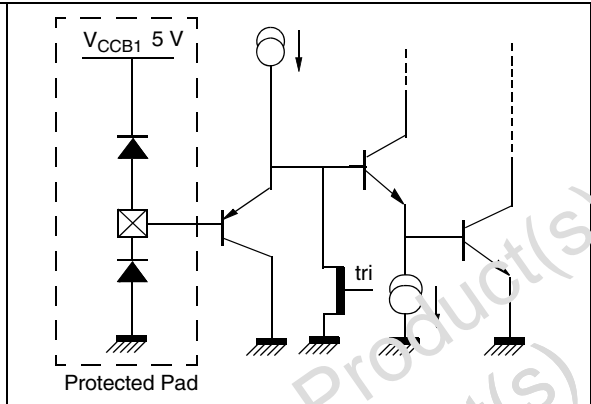
Obsolete Product(s) - Obsolete Product(s)  
Obsolete Product(s) - Obsolete Product(s)

## 4 Input/output groups

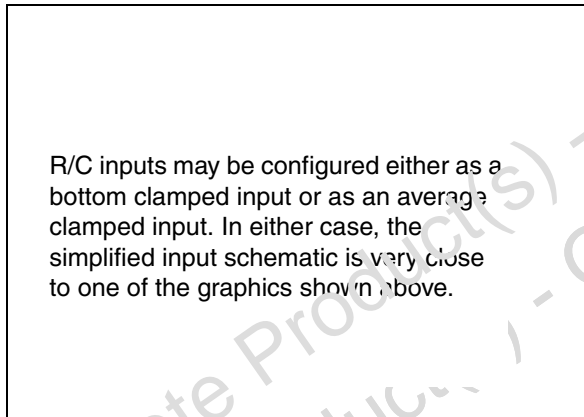
**Figure 5. Bottom clamped video inputs (pins 4, 6, 12, 14, 18, 21, 62 and 64)**



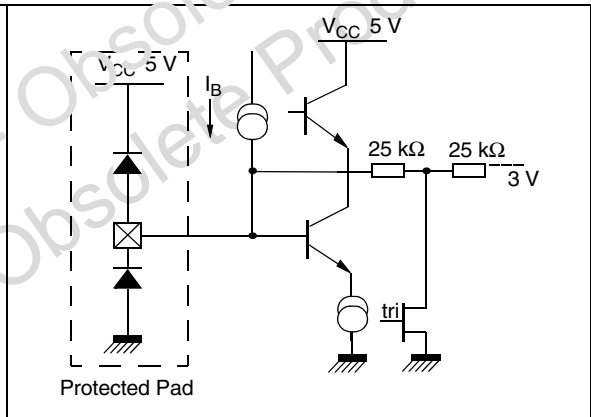
**Figure 6. Fast blanking inputs (pins 50 and 51)**



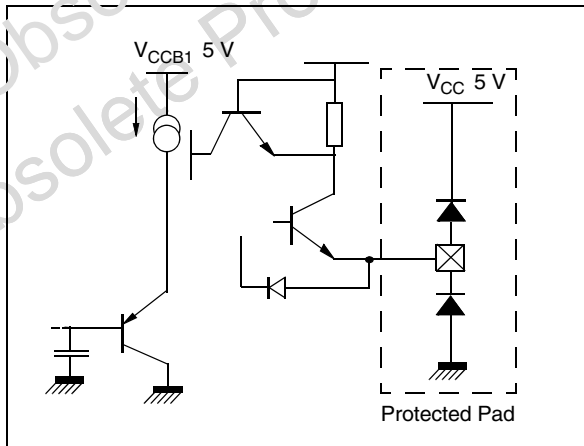
**Figure 7. R/C clamped video inputs (pins 10 and 60)**



**Figure 8. Average clamped video inputs (pin 8)**



**Figure 9. Fast blanking output (pin 49)**



**Figure 10. C-gate logical output (pin 52)**

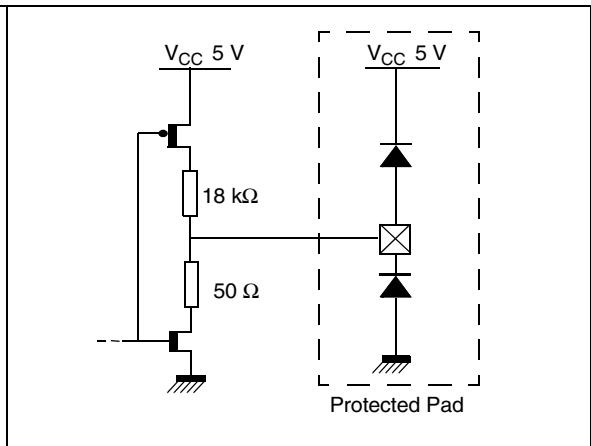


Figure 11. Video outputs (pins 38, 40, 42, 44, 46 and 48)

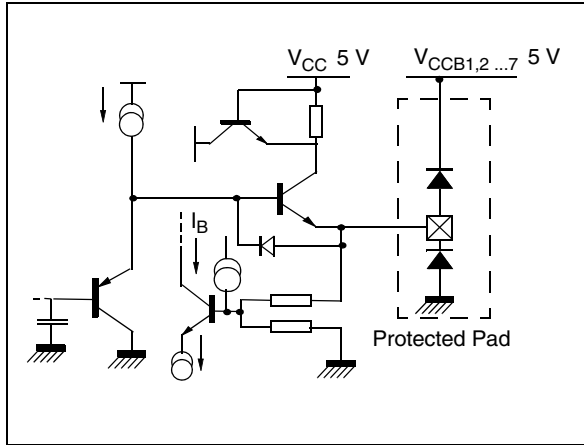


Figure 12. Audio outputs (pins 27, 28, 29, 30, 32 and 33)

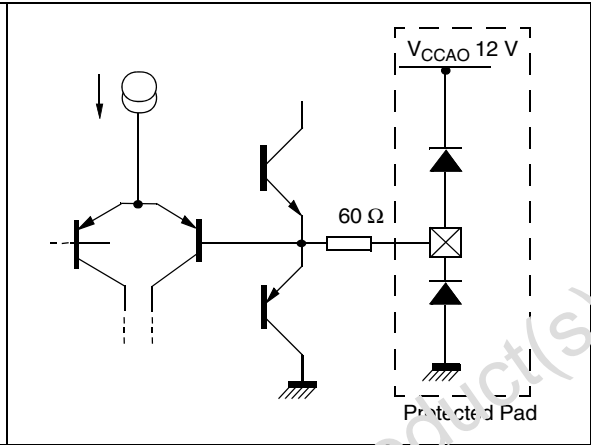


Figure 13. Audio inputs pins 11, 13, 19, 20, 22 and 23)

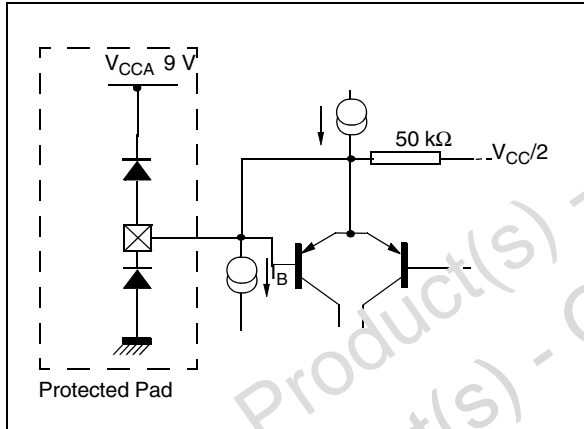


Figure 14. Interrupt output (pin 58)

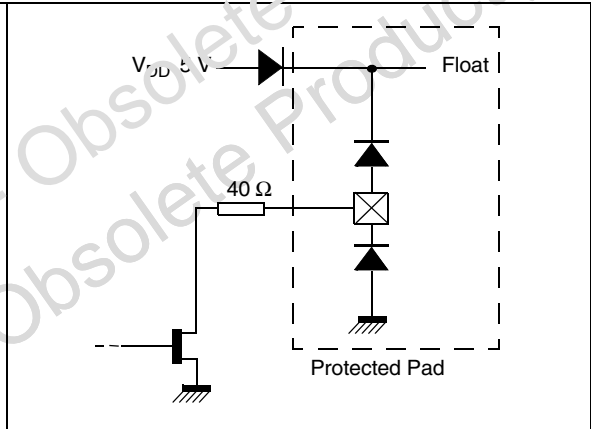


Figure 15. Snow blanking I/O (pins 59 and 61)

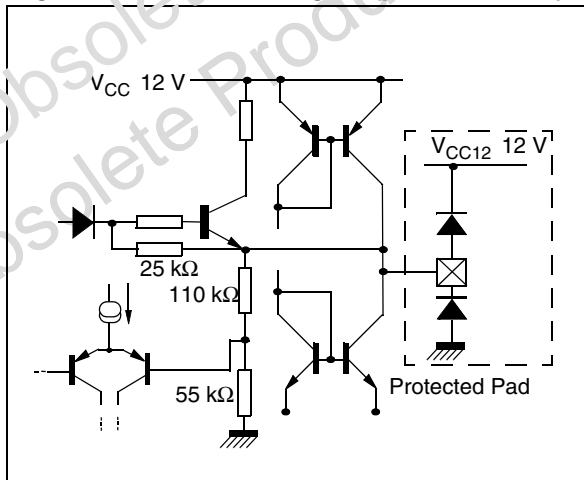


Figure 16. I²C bus (SDA) (pin 56)

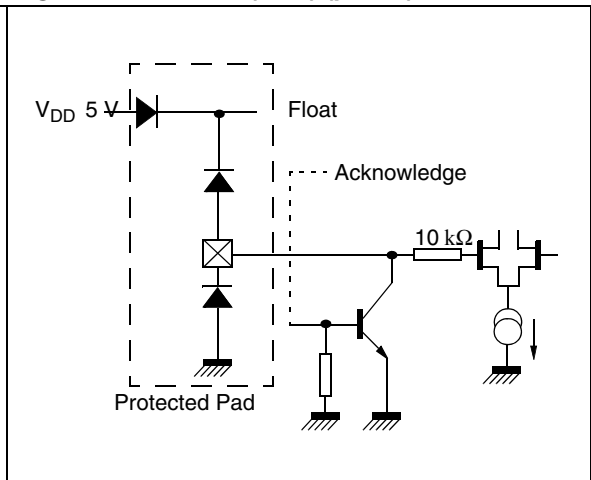




Figure 17. I<sup>2</sup>C bus (SCL) (pin 55)

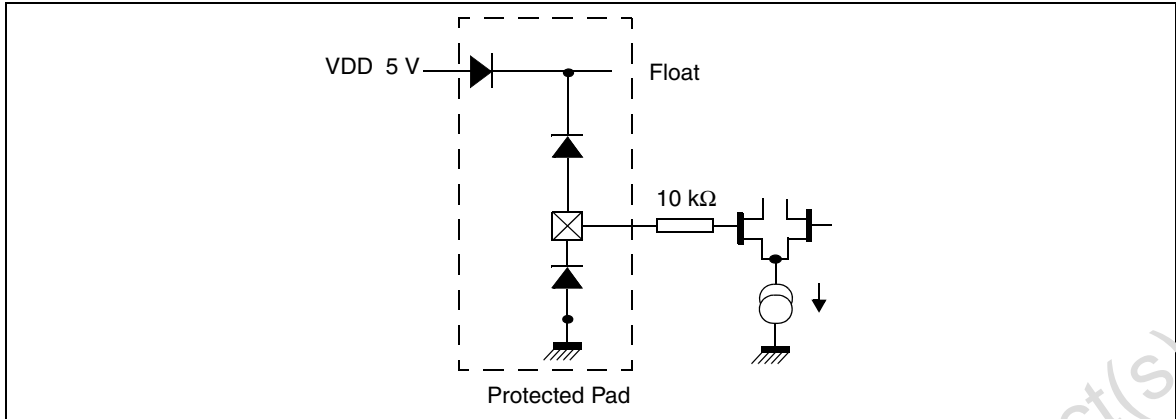
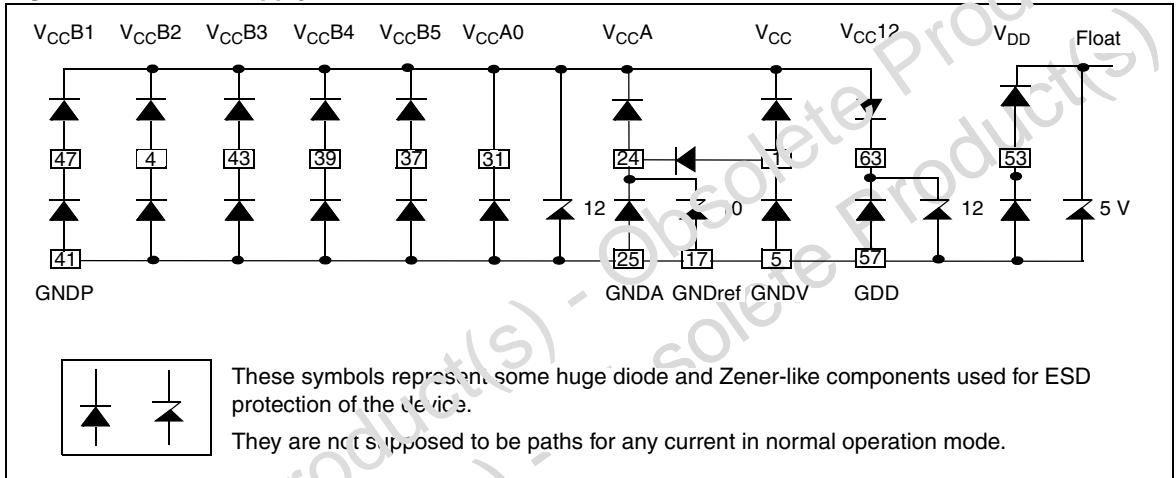


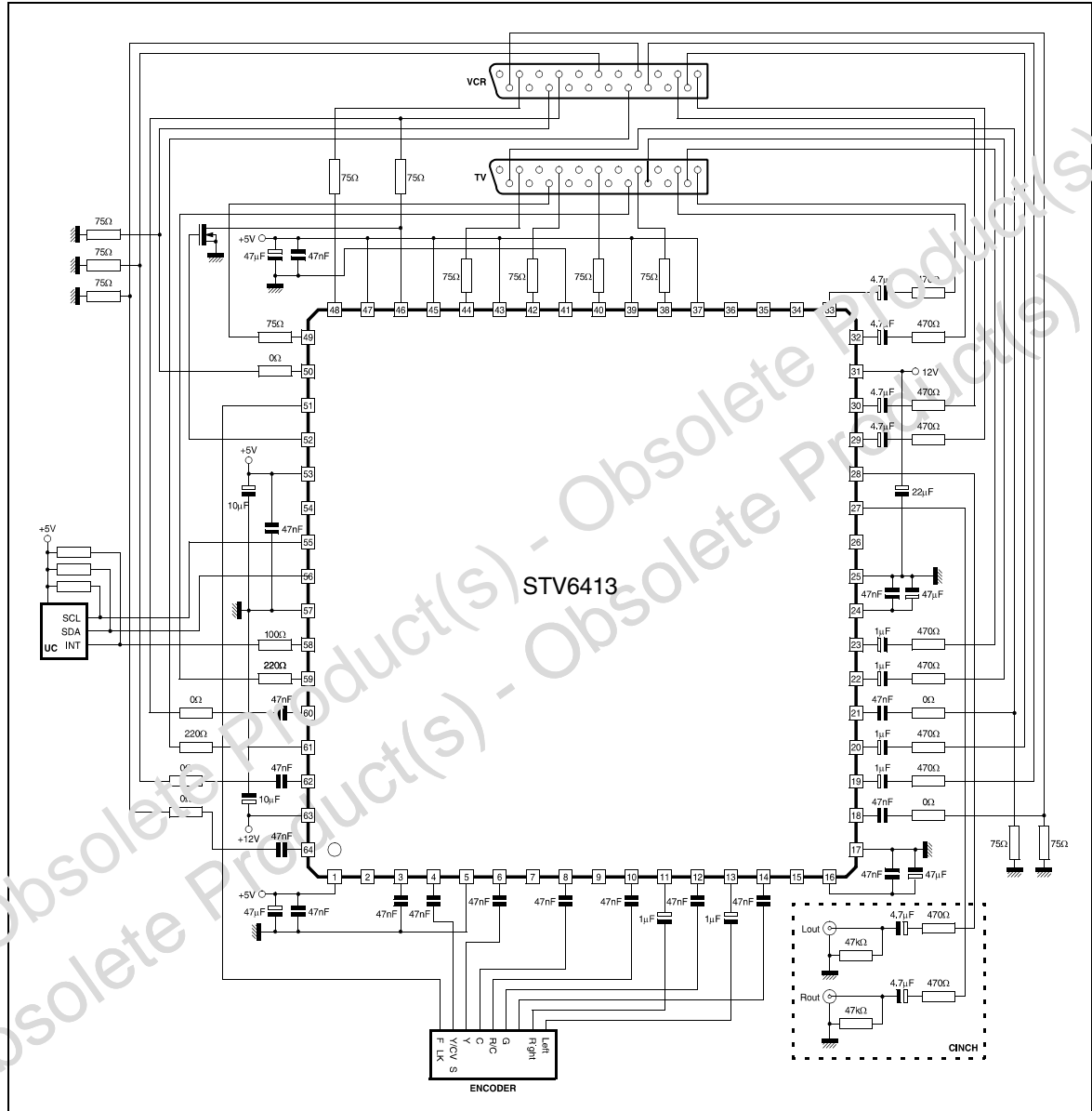
Figure 18. Power supply connection



# 5 Application diagram

Note: The application diagram presented here is an example only and is subject to change without notice. The real application diagram will depend on application conditions and constraints.

Figure 19. STV6413 application diagram



Note: For more details refer to STV6412A Application Note.

## 6 Package mechanical data

Figure 20. 64-pin, thin full plastic quad flat pack (TQFP)

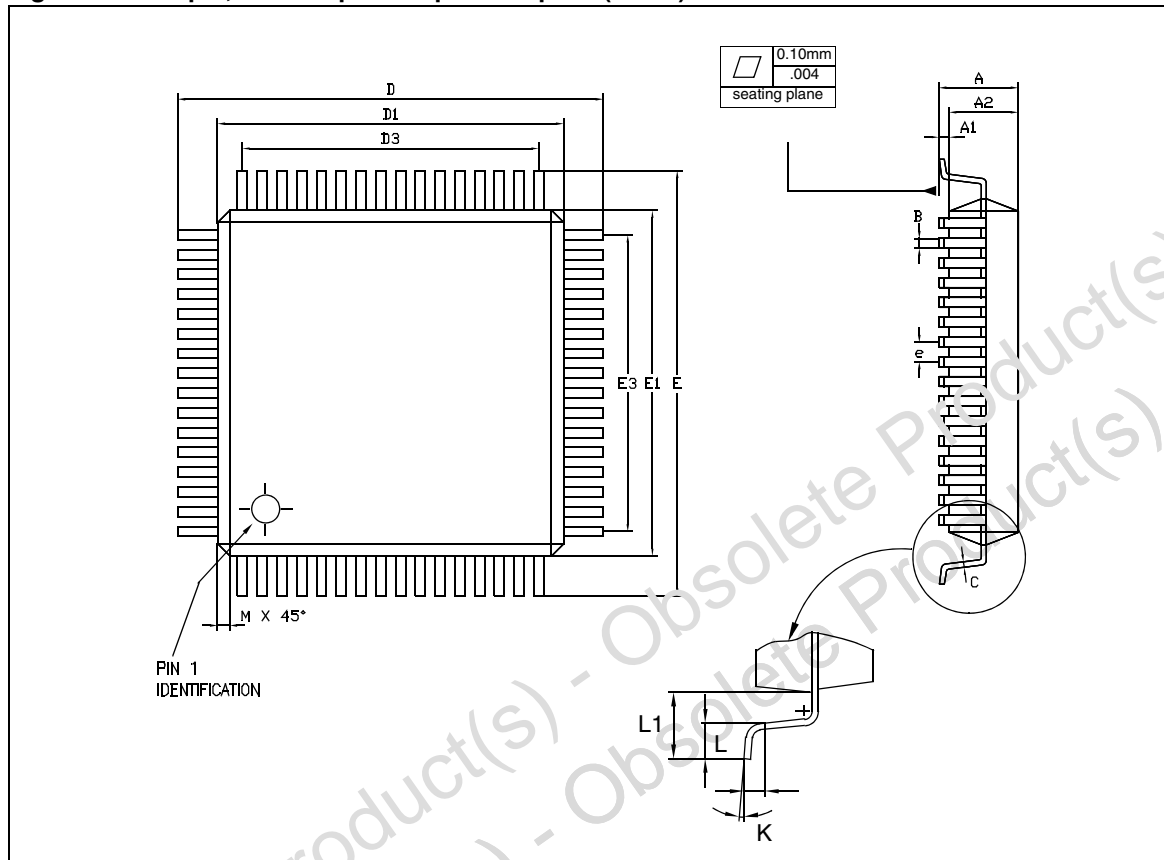


Table 26. 64-pin TQFP dimensions

Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
E		12.00			0.472	
E1		10.00			0.394	
e		0.50			0.020	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of pins					
N	64		ND	16	NE	16

## 6.1 Environmentally-friendly packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance.

ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

## 7 Revision history

**Table 27. Revision revision history**

Date	Revision	Changes
September 2001	1.0	First issue
December 2001	1.1	Pin list updated.
March 2002	1.2	STV6413 Product Preview updated to datasheet. Order codes updated. Note added to <a href="#">Section 2.2: Thermal data on page 8</a> . Test Conditions updated for total harmonic distortion values in <a href="#">Table 8: Audio section</a> .
July 2002	1.3	Modification to <a href="#">Note 1 on page 16</a>
March 2007	1.4	Reformatted to new corporate template. Corrections to <a href="#">Figure 19: STV6413 application diagram on page 26</a> and addition of application diagram disclaimer.
April 2007	2	Added values for $R_{thJC}$ and $T_{thJC}$ in <a href="#">Section 2.2: Thermal data on page 8</a> .
01-Apr-2009	3	Preliminary banner removed, <a href="#">Section 6.1: Environmentally-friendly packages</a> added.

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