

P-channel 20 V, 0.0195 Ω typ., 9 A STripFET™ H7 Power MOSFET in a SO-8 package

Datasheet - production data

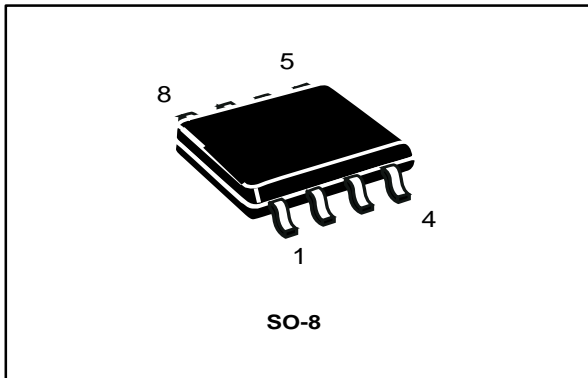
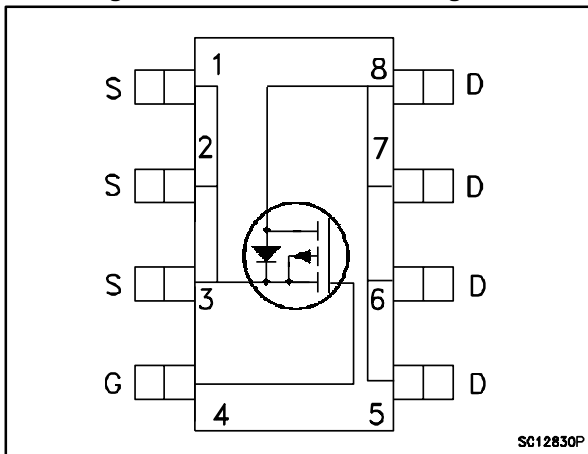


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STS9P2UH7	20 V	0.0225 Ω @ 4.5 V	9 A

- Very low on-resistance
- Very low capacitance and gate charge
- High avalanche ruggedness
- Ultra logic level

Applications

- Switching applications

Description

This device exhibits low on-state resistance and capacitance for improved conduction and switching performance.

Table 1: Device summary

Order code	Marking	Package	Packaging
STS9P2UH7	9L2U	SO-8	Tape and reel



For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	20	V
V_{GS}	Gate-source voltage	± 8	V
I_D	Drain current (continuous) at $T_{pcb} = 25\text{ °C}$	9	A
I_D	Drain current (continuous) at $T_{pcb} = 100\text{ °C}$	5.8	A
$I_{DM}^{(1)}$	Drain current (pulsed)	36	A
P_{TOT}	Total dissipation at $T_{pcb} = 25\text{ °C}$	2.7	W
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

Notes:

⁽¹⁾Pulse width limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	47	°C/W

Notes:

⁽¹⁾When mounted on 1inch² FR-4 board, 2 oz Cu



For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0, I _D = 250 μA	20			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0, V _{DS} = 20 V			1	μA
I _{GSS}	Gate-body leakage current	V _{DS} = 0, V _{GS} = ± 5 V			± 5	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	0.4		1	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 4.5 V, I _D = 4.5 A		0.0195	0.0225	Ω
		V _{GS} = 2.5 V, I _D = 4.5 A		0.02	0.025	Ω
		V _{GS} = 1.8 V, I _D = 4.5 A		0.036	0.043	Ω
		V _{GS} = 1.5 V, I _D = 4.5 A		0.05	0.085	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{GS} = 0, V _{DS} = 16 V, f = 1 MHz	-	2390	-	pF
C _{oss}	Output capacitance		-	220	-	pF
C _{rss}	Reverse transfer capacitance		-	188	-	pF
Q _g	Total gate charge	V _{DD} = 16 V, I _D = 9 A, V _{GS} = 4.5 V	-	22	-	nC
Q _{gs}	Gate-source charge		-	4.2	-	nC
Q _{gd}	Gate-drain charge		-	3.6	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 16 V, I _D = 9 A, R _G = 1 Ω, V _{GS} = 4.5 V	-	12.5	-	ns
t _r	Rise time		-	30.5	-	ns
t _{d(off)}	Turn-off delay time		-	128	-	ns
t _f	Fall time		-	84.5	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	$V_{GS} = 0, I_{SD} = 1 \text{ A}$	-		1	V
t_{rr}	Reverse recovery time	$V_{DD} = 16 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}, I_{SD} = 1 \text{ A}$	-	15.8		ns
Q_{rr}	Reverse recovery charge		-	5.9		nC
I_{RRM}	Reverse recovery current		-	0.7		A

Notes:

(1) Pulsed: pulse duration = 300 μs , duty cycle 1.5%



For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

2.1 Electrical characteristics (curves)

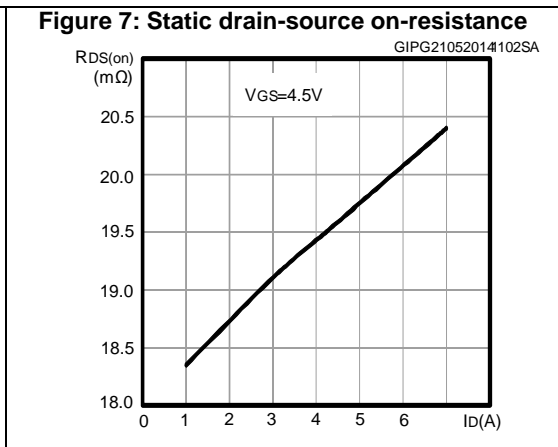
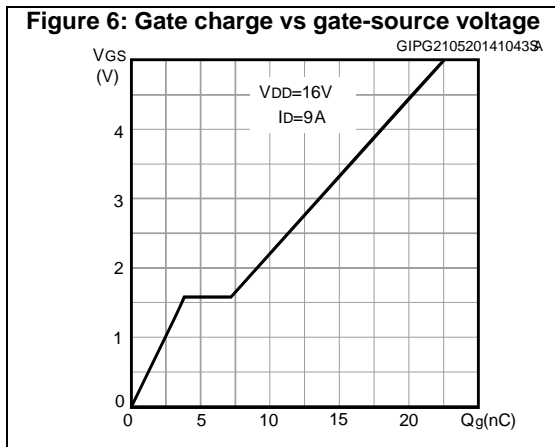
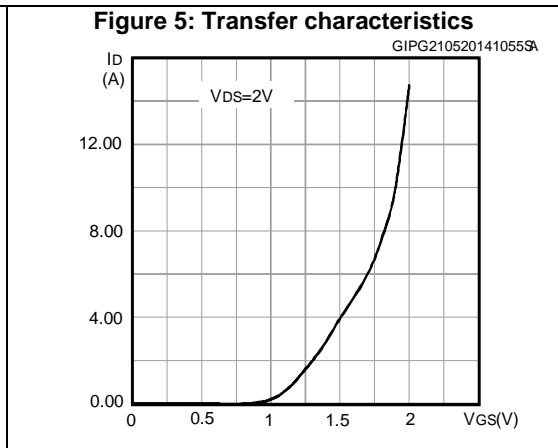
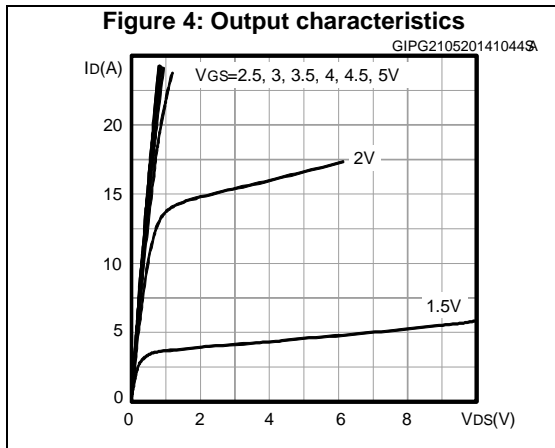
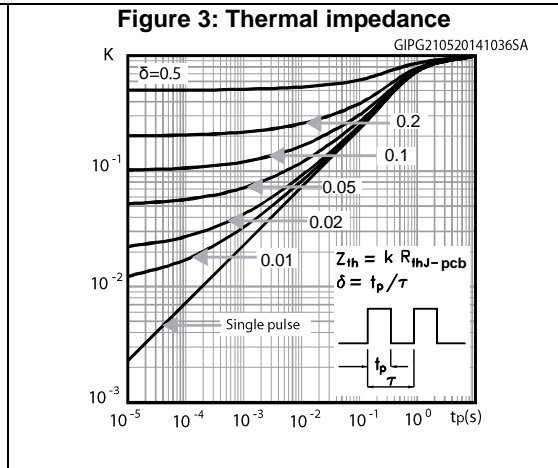
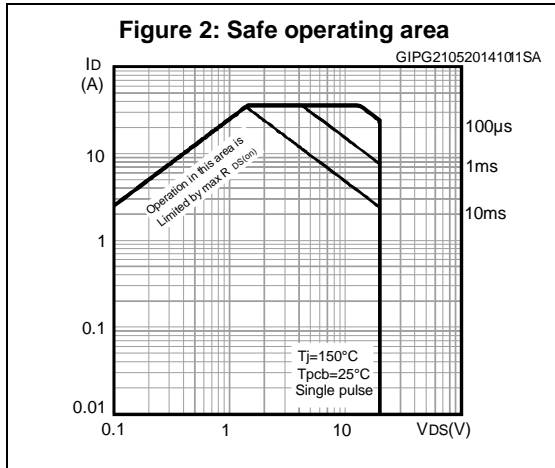


Figure 8: Capacitance variations

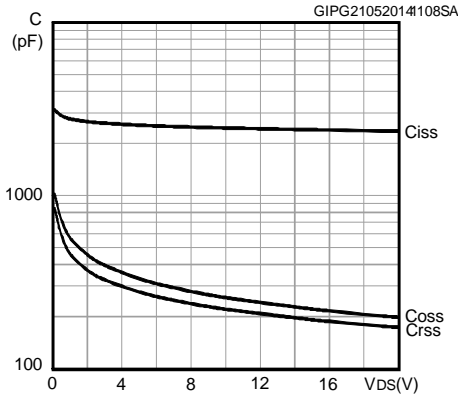


Figure 9: Normalized gate threshold voltage vs temperature

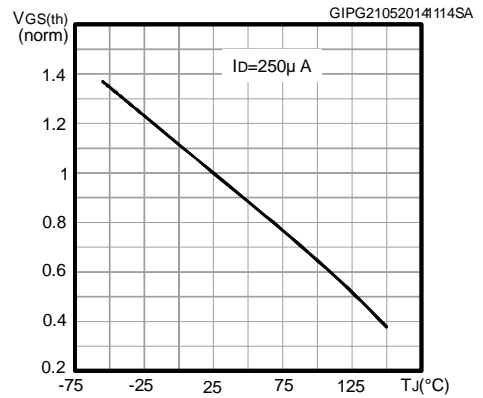


Figure 10: Normalized on-resistance vs temperature

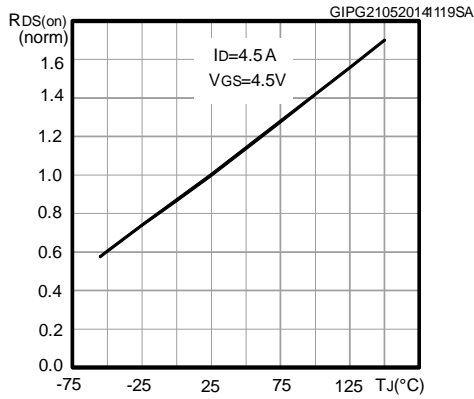


Figure 11: Normalized V(BR)DSS vs temperature

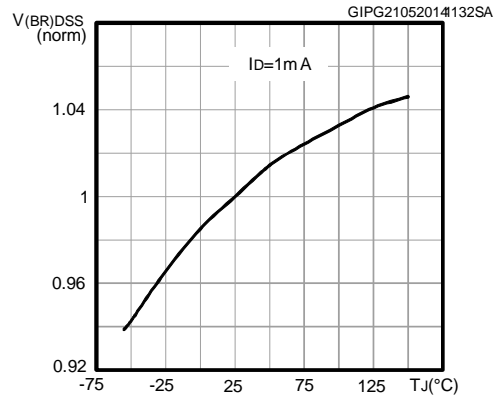
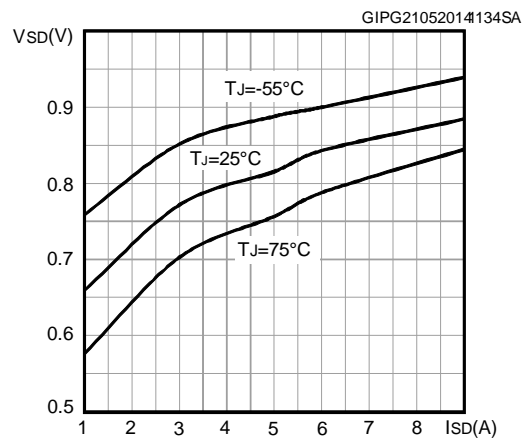


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Switching times test circuit for resistive load

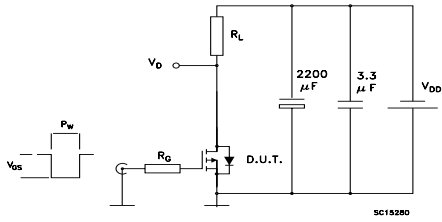


Figure 14: Gate charge test circuit

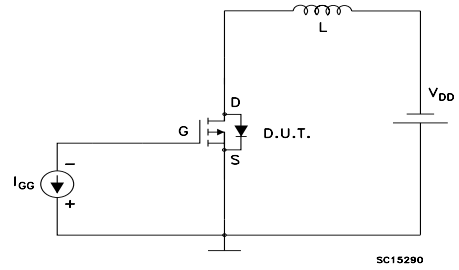
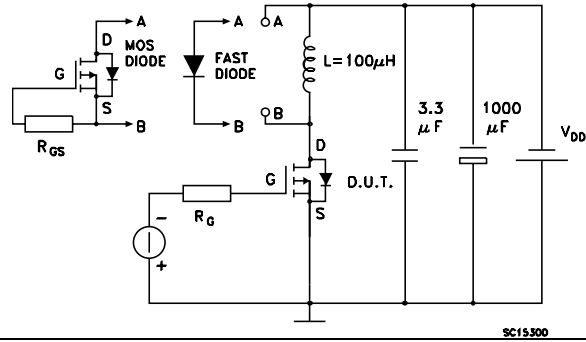


Figure 15: Test circuit for inductive load switching and diode recovery times

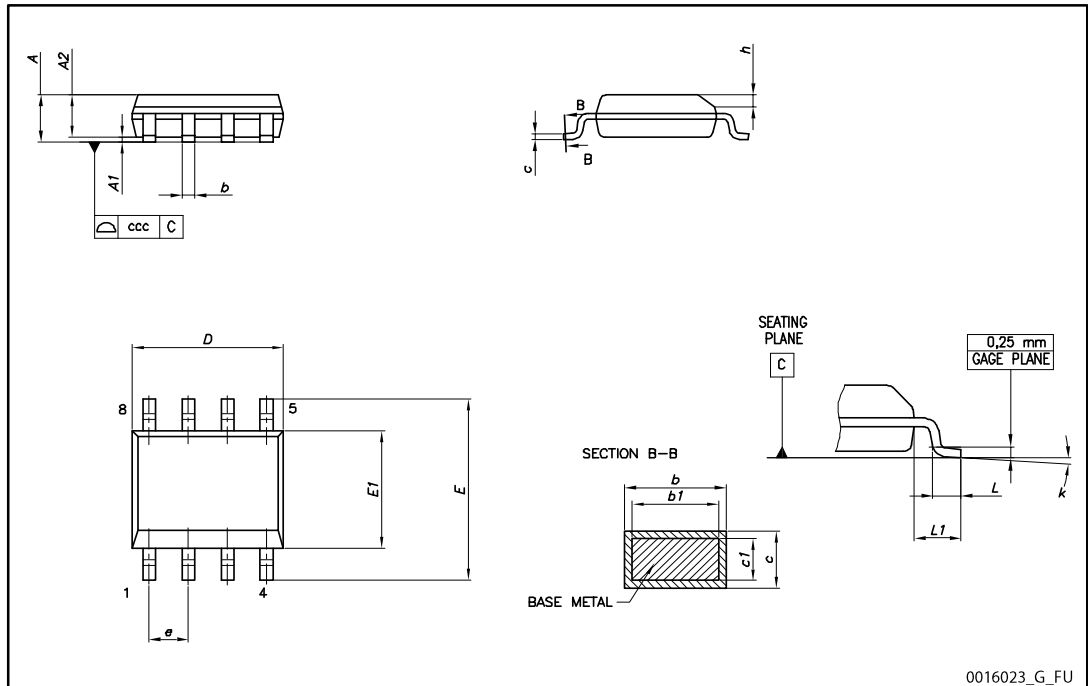


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 SO-8 package mechanical data

Figure 16: SO-8 drawing

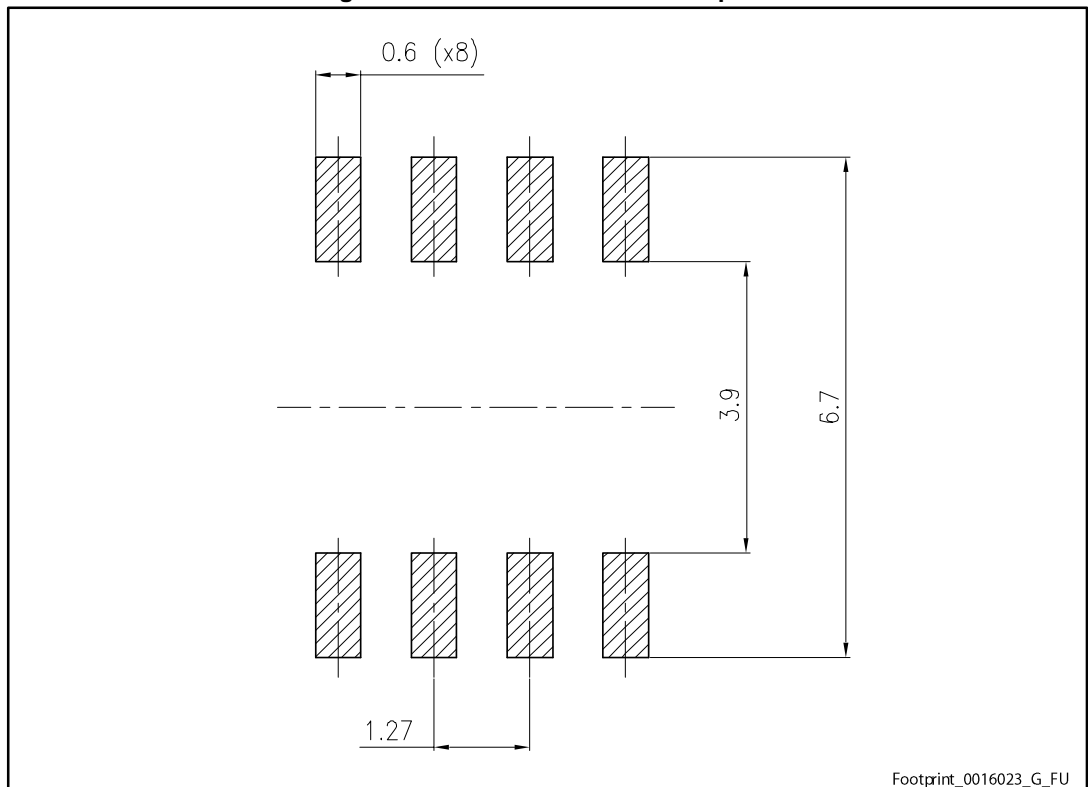


0016023_G_FU

Table 8: SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 17: SO-8 recommended footprint



5 Packaging mechanical data

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5.1 SO-8 tape and reel mechanical data

Figure 18: SO-8 tape and reel dimensions

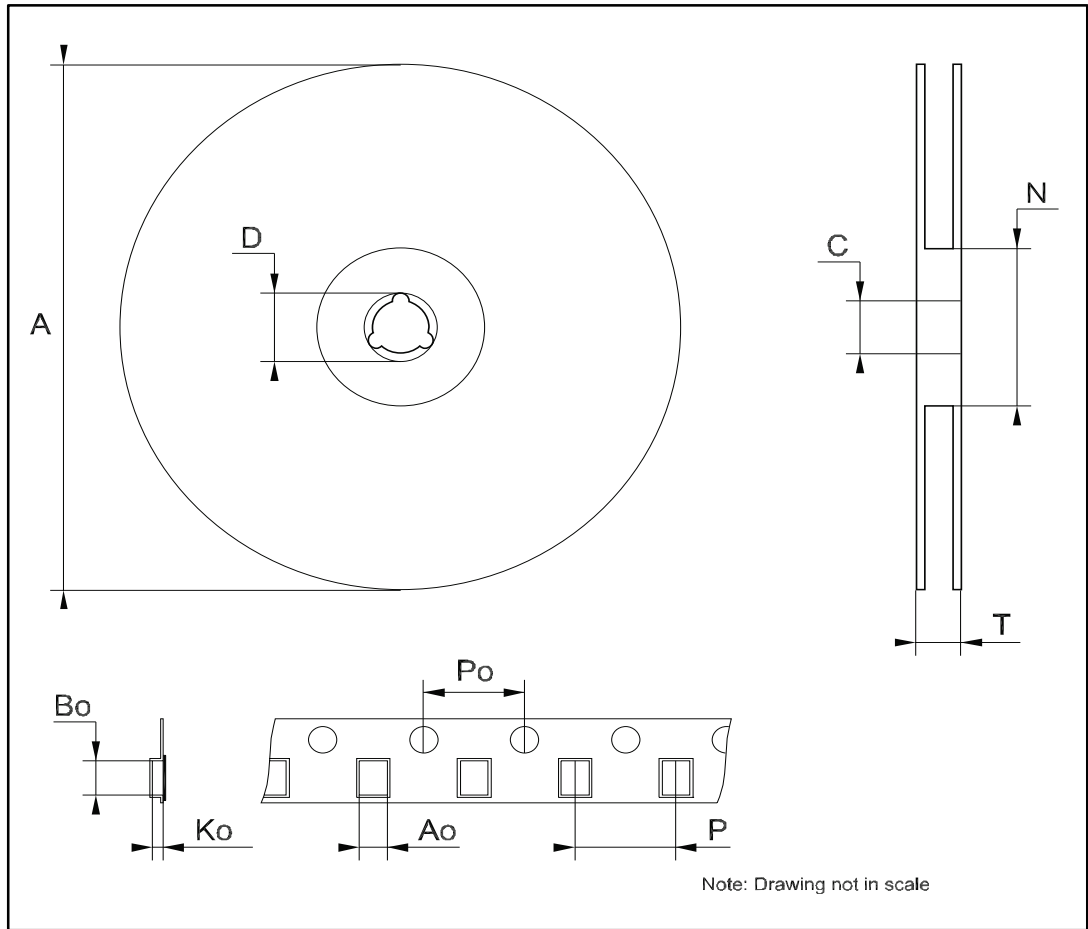


Table 9: SO-8 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A		-	330
C	12.8	-	13.2
D	20.2	-	
N	60	-	
T		-	22.4
Ao	8.1	-	8.5
Bo	5.5	-	5.9
Ko	2.1	-	2.3
Po	3.9	-	4.1
P	7.9	-	8.1

6 Revision history

Table 10: Document revision history

Date	Revision	Changes
27-Aug-2013	1	First release.
04-Jun-2014	2	Document status promoted from preliminary data to production data Modified: title Modified: $R_{DS(on)}$ max value in cover page Modified: $R_{DS(on)}$ (typical and maximum) values in Table 4: "On /off states" Modified: the entire typical values in Table 5: "Dynamic" , Table 6: "Switching times" and Table 7: "Source drain diode" Added: Section 8.1: "Electrical characteristics (curves)" Minor text changes
12-Jan-2015	3	Updated title, features and description in cover page. Updated Figure 3: "Thermal impedance" .

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