Errata Sheet for Stratix IV GT Devices

This errata sheet provides updated information about known device issues affecting Stratix® IV GT devices.

Production Device Issues for Stratix IV GT Devices

Table 1 lists the issues and affected Stratix IV GT production devices.

Table 1. Production Device Issues for Stratix IV GT Devices (Part 1 of 2)

Issue	Affected Devices	Planned Fix
"PLL phasedone Signal Stuck at Low" In some cases, the Stratix IV phase-locked loop (PLL) blocks exhibit the `phasedone` signal stuck at low during the PLL dynamic phase shift.	All Stratix IV GT (ES and Production) Devices	Quartus II software version 12.0 and later.
"Remote System Upgrade" The remote system upgrade feature fails when loading an invalid configuration image.	All Stratix IV GT (ES and Production) Devices	Quartus II software version 9.1 and later.
"EDCRC False Errors" The error detection CRC (SEU detection) feature may falsely assert the `CRC_ERROR` signal when no SEU event has occurred.	All Stratix IV GT (ES1 and Production) Devices	—
"Minimum Differential Eye Opening Requirement" The minimum differential eye opening specification has been revised for Stratix IV GT devices.	All Stratix IV GT (ES1 and Production) Devices	—
"PCI Express (PCIe) Interface with Hard IP Block Migration" PCIe interfaces using the hard IP block between specific devices cannot be migrated.	All Stratix IV GT (ES1 and Production) Devices	Quartus II software version 10.1 SP1
"PCIe Gen2 Protocol Link Establishment Issue" The PCIe rate switch controller may not be initialized correctly for the PCIe Gen2 protocol, preventing the link from being established.	All Stratix IV GT (ES1 and Production) Devices	Quartus II software version 10.1 SP1 and later. Patches are available for the Quartus II software versions 9.1 SP2 and 10.1.
"Quartus II Software Incorrect Setting for Transceiver CDR in All Modes Except PCIe Mode" The Quartus II software incorrectly sets the CDR unit when the transceiver channel is configured in any mode except PCIe mode and the CDR is configured to automatic lock mode.	All Stratix IV GT (ES1 and Production) Devices	Quartus II software version 10.1 and later. Patches are available for the Quartus II software versions 9.1 SP2 and 10.0 SP1.

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Table 1. Production Device Issues for Stratix IV GT Devices (Part 2 of 2)

Issue	Affected Devices	Planned Fix
"Dynamic Reconfiguration Issue Between PCIe Mode and Any Other Transceiver Mode" The transceiver may not be initialized correctly if your application uses dynamic reconfiguration to change the transceiver channel between PCIe mode and any other transceiver mode.	All Stratix IV GT (ES1 and Production) Devices	No plan to fix silicon. Apply the reset sequence in "Dynamic Reconfiguration Issue Between PCIe Mode and Any Other Transceiver Mode".
"Quartus II Mapping Issue with PCIe Interfaces Using the Hard IP Block" The Quartus II software incorrectly maps the PCIe interfaces when using the hard IP block.	Stratix IV GT ES1 and all production devices	For more information, refer to "Quartus II Mapping Issue with PCIe Interfaces Using the Hard IP Block".
"I/O Jitter" Affected Stratix IV GT production devices may exhibit higher than expected jitter on general purpose I/O pins.	EP4S40G5, EP4S100G3, EP4S100G4, EP4S100G5	EP4S40G5 Rev F, EP4S100G3 Rev F, EP4S100G4 Rev F, EP4S100G5 Rev F
"Fast Passive Parallel (FPP) Mode Configuration Failures at High DCLK Frequency" Stratix IV GT configuration fails in FPP mode when the DCLK frequency is set to 125 MHz with a 60/40 or 40/60 duty cycle.	All production devices	—
"FPP Mode Configuration Failures When the Minimum Hold Time (t_{DH}) is set to 0 ns or 24 ns" Stratix IV GT configuration fails in FPP mode when the minimum data hold time (t_{DH}) is set to 0 ns for uncompressed and unencrypted configuration data or 24 ns for compressed and/or encrypted data.	All production devices	—
"Transmitter PLL Lock (pll_locked) Status Signal" The transmitter PLL lock status signal (`pll_locked`) does not deassert when the `pll_powerdown` signal is asserted in configurations that use the reference clock pre-divider of 2, 4, or 8.	Stratix IV GT ES1 and all production devices	No plan to fix silicon. For a soft-fix solution, refer to "Transmitter PLL Lock (pll_locked) Status Signal"
"M144K RAM Block Lock-Up" M144K RAM blocks may lock up if there is a glitch in the clock source.	All production devices	—
"×8 and ×N Clock Line Timing Issue for Transceivers" xN clock line performance limits data rates depending on clock source configuration.	All production devices	—
"Stratix IV GT Power-up Sequencing on Production Devices" The device fails to power up and exit POR at low temperatures when V_{CC} is powered after V_{CCAUX}.	All production devices	—
"High Power Supply Current During Power-Up for V_{CCPD} and $V_{CCA\_L/R}$" Higher power-up current requirements are needed for V_{CCPD} and $V_{CCA\_L/R}$ power supplies.	Stratix IV GT ES1 and all production devices	For more information, refer to "High Power Supply Current During Power-Up for V_{CCPD} and $V_{CCA\_L/R}$"

PLL phasedone Signal Stuck at Low

In some cases, the Stratix IV PLL blocks exhibit the phasedone signal stuck at low during the PLL dynamic phase shift. When the PLL phasedone signal is stuck at low, the intended phase shift does not happen. You can recover from the PLL phasedone signal being stuck at low by resetting the PLL or by restarting the phase shift operation by asserting the phasestep signal.

Solution

To resolve the PLL phasedone signal stuck at low issue, the Altera PLL megafunction is enhanced to automatically restart the phase shift operation internally in the Altera PLL megafunction whenever the PLL phasedone signal is stuck at low. Restarting the phase shift operation compensates for the missing phase shift operation and also recovers the phasedone signal.

This Altera PLL megafunction solution will be implemented in the Quartus II software version 12.0 and later. Altera recommends upgrading to the latest Quartus II software, regenerating the PLL megafunction, and recompiling your design.

Additionally, software patches are available for the Quartus II software versions 9.1 SP2 and 10.1 SP1 to upgrade the PLL megafunction with the solution. To download and install the Quartus II software patch, refer to the PLL Phasedone Stuck at Low Solution.

If you need additional support, file a service request using mySupport.

Remote System Upgrade

The remote system upgrade feature does not operate correctly when you initiate a reconfiguration cycle that goes from a factory configuration image to an invalid application configuration image. In this scenario, the device fails to revert back to the factory configuration image after a configuration error is detected while loading the invalid application configuration image. The failure is indicated by a continuous toggling of the nSTATUS pin.

In correct operation, the device reverts to the factory configuration image after a configuration error is detected with the invalid configuration image.

An invalid application configuration image is classified as one of the following:

- A partially programmed application image
- A blank application image
- An application image assigned with a wrong start address

The remote system upgrade feature works correctly with all other reconfiguration trigger conditions.

This issue is addressed by enabling the Reconfig POF Checking feature in the updated ALTREMOTE_UPDATE megafunction and is available in the Quartus® II software version 9.1 and later.

For more information about how to enable the Reconfig POF Checking feature, refer to *AN 603: Active Serial Remote System Upgrade Reference Design*.

EDCRC False Errors

The error detection cyclic redundancy check (CRC) (single event upset [SEU] detection) feature may falsely assert the CRC_ERROR signal when no SEU event has occurred. The falsely asserted CRC_ERROR signal happens because the configuration RAM is incorrectly read for the EDCRC checks. In this scenario, the configuration RAM data and the functionality of the device are not affected.

- If EDCRC is not critical to your system, turn it off.
- If EDCRC is required, insert a soft IP in your design.

For more support and to request the soft IP, file a service request using mySupport.

Minimum Differential Eye Opening Requirement

Stratix IV GT devices have a revised minimum differential eye opening specification at the receiver serial input pins from 85 mV for all data rates to:

- 85 mV for data rates less than or equal to 10.3125 Gbps
- 165 mV for data rates greater than 10.3125 Gbps

This information will be reflected in the *DC and Switching Characteristics for Stratix IV Devices* chapter, version 4.9.

PCI Express (PCIe) Interface with Hard IP Block Migration

The Quartus II software version 10.1 and earlier incorrectly allows migration for PCI Express® (PCIe®) interfaces using the hard IP block from EP4S40G2F40 and EP4S100G2F40 devices to EP4S40G5H40 and EP4S100G5H40 devices, respectively. The related Stratix IV GT documentation also incorrectly states that migration for PCIe interfaces using the hard IP block for these devices is allowed. PCIe interfaces using the hard IP block between these devices cannot be migrated. This migration issue is fixed in Quartus II software version 10.1 SP1, disallowing migration of the PCIe interface using the hard IP block between these devices.

PCIe Gen2 Protocol Link Establishment Issue

The PCIe rate switch controller may not be initialized correctly for the PCIe Gen2 protocol, preventing the link from being established. When the rate switch controller is not initialized correctly, the transmitted TS1 training sequence is corrupted. This link establishment issue occurs intermittently and in some cases, power cycling the device may re-establish the link. This link establishment issue affects PCIe Gen2 x1, x4, and x8 configurations with and without the hard IP block. The PCIe Gen1 only configurations are not affected.

Solution

This link establishment issue is fixed in the Quartus II software versions 10.1 SP1 and later. Altera recommends upgrading to the latest Quartus II software, regenerating the IP, and recompiling your design. For complete details of the solution, refer to the PCIe Gen2 Protocol Link Solution.

Additionally, software patches are available for the Quartus II software versions 9.1 SP2 and 10.1.

To download and install the patch, refer to the PCIe Gen2 Protocol Link Solution.

Quartus II Software Incorrect Setting for Transceiver CDR in All Modes Except PCIe Mode

The Quartus II software versions 10.0 SP1 and earlier incorrectly set the clock and data recovery (CDR) unit when the transceiver channel is configured in any mode except PCIe mode and the CDR is configured to automatic lock mode. When there are no data transitions on the transceiver data inputs for an extended period of time (in the ms range), the CDR may keep the `rx_freqlocked` signal asserted. The CDR does not return to the lock-to-reference (LTR) state and incorrect data may be recovered.

The transceiver channels configured in PCIe mode are NOT affected by this issue.

Solution

This incorrect setting issue is fixed in the Quartus II software versions 10.1 and later. Altera recommends upgrading to the latest Quartus II software and recompiling your design. For complete details of the solution, refer to the Transceiver CDR Solution.

Additionally, software patches are available for the Quartus II software versions 9.1 SP2 and 10.0 SP1.

To download and install the patch, refer to the Transceiver CDR Solution.

If you need additional support, file a service request using Altera's mySupport.

Dynamic Reconfiguration Issue Between PCIe Mode and Any Other Transceiver Mode

If your application uses dynamic reconfiguration to change the transceiver channel between PCIe mode and any other transceiver mode, the transceiver may not be initialized correctly, resulting in receiver bit errors.

This dynamic reconfiguration issue affects dynamic reconfiguration between PCIe mode and any other transceiver mode only. Dynamic reconfiguration between any transceiver modes other than PCIe mode is not affected.

Workaround

If you see bit errors, apply the reset sequence described in the Reset Sequence Solution.

If you need additional support, file a service request using Altera's mySupport.

Quartus II Mapping Issue with PCIe Interfaces Using the Hard IP Block

The Quartus II software versions 9.1, 9.1 SP1, and 9.1 SP2 incorrectly allow logical channel 0 to be placed in any physical channel for x1 and x4 PCIe Gen1 interfaces with the hard IP block when targeting Stratix IV GT ES1 and all production devices. For correct operation with the hard IP block, logical channel 0 must be placed in physical channel 0.

In addition, for EP4S40G5H40 and EP4S100G5H40 production devices, the Quartus II software versions 9.1, 9.1 SP1, 9.1 SP2, and 10.0 incorrectly map x1 and x4 PCIe (Gen1 and Gen2) interfaces with the hard IP block to transceiver block GXBL1 or GXBR1. The correct mapping must be to transceiver blocks GXBL2 or GXBR2. In addition, a no-fit error occurs for x8 PCIe (Gen1 and Gen2) interfaces in these devices when compiling in versions 9.1, 9.1 SP1, 9.1 SP2, and 10.0 of the Quartus II software, even when the pins are assigned to the correct transceiver blocks.

If you are in the register transfer level (RTL) design phase, upgrade to the Quartus II software version 10.0 SP1 for the correct mapping of the interface. If you have already designed or fabricated your boards using the incorrect mapping, for assistance to remedy the mapping issue, file a service request using mySupport.

I/O Jitter

Affected Stratix IV GT production devices (refer to Table 1 on page 1) may exhibit up to ±50 ps higher than expected jitter on all non-transceiver general purpose I/O pins. Transceiver I/O pins and I/O pins in LVDS mode (including dynamic phase alignment [DPA] and soft clock data recovery [CDR]) are not affected. The actual amount of additional jitter depends on the device switching activity.

The EP4S40G2 and EP4S100G2 production ordering codes are not affected.

Altera is fixing this issue in the next revision of production devices, which will meet all current jitter specifications.

For further support, file a service request using mySupport.

Fast Passive Parallel (FPP) Mode Configuration Failures at High DCLK Frequency

Stratix IV GT devices might fail to configure in FPP mode if the DCLK frequency is set to 125 MHz with a 60/40 or 40/60 duty cycle. When this configuration issue occurs, the device pulls the nSTATUS pin low and the configuration host may initiate a reconfiguration.

This problem affects all Stratix IV GT devices.

For successful FPP configuration at 125 MHz for EP4S40G2 and EP4S100G2 devices, set the duty cycle to 45/55, 55/45, or higher. This setting corresponds to a minimum DCLK high time (t_{CH}) and a minimum DCLK low time (t_{CL}) of 3.6 ns.

For EP4S40G5, EP4S100G3, EP4S100G4, and EP4S100G5 devices, reduce the DCLK frequency to 100 MHz or lower and set the duty cycle to 45/55, 55/45, or higher. These settings correspond to a minimum DCLK high time (t_{CH}) and a minimum DCLK low time (t_{CL}) of 4.5 ns.

FPP Mode Configuration Failures When the Minimum Hold Time (t_{DH}) is set to 0 ns or 24 ns

Stratix IV GT devices might fail to configure in FPP mode if the minimum hold time (t_{DH}) for the configuration data is set to 0 ns for uncompressed and unencrypted configuration data, or 24 ns for compressed and/or encrypted data. When this configuration issue occurs, the device pulls the nSTATUS pin low and the configuration host may initiate a reconfiguration.

This problem affects all Stratix IV GT devices.

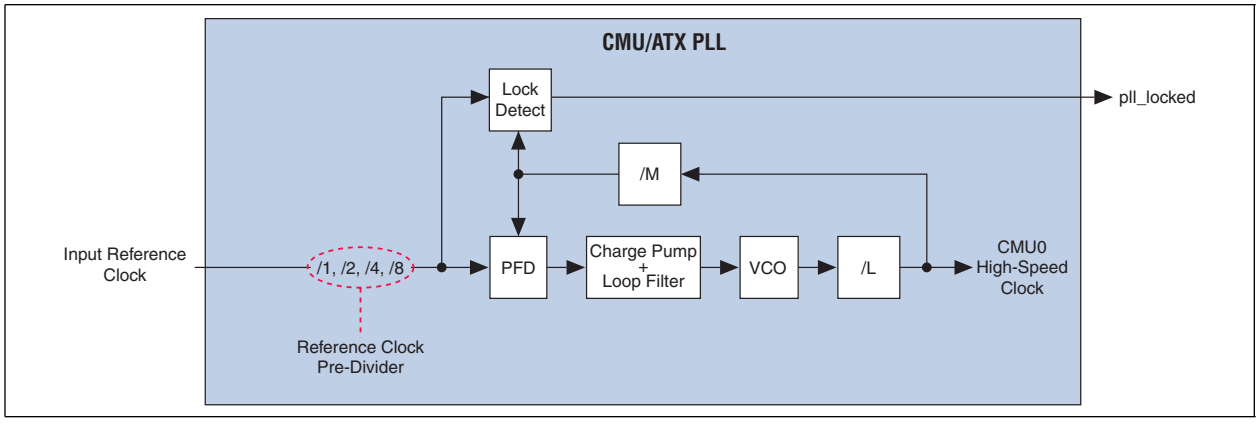
You can successfully configure the Stratix IV GT devices in FPP mode by setting the minimum hold time (t_{DH}) for the uncompressed and unencrypted configuration data to 1 ns or higher. For compressed and/or encrypted data, set the minimum hold time (t_{DH}) to 3 * 1/f_{DCLK} + 1 ns or higher (f_{DCLK} is your DCLK frequency setting). Alternatively, you can drive the configuration data out on the falling edge of the DCLK.

The MAX II Parallel Flash Loader drives out configuration data on the falling edge of the DCLK. This issue does not affect you if you use the Max II Parallel Flash Loader as the configuration controller.

Transmitter PLL Lock (pll_locked) Status Signal

The transmitter PLL lock status signal (pll_locked) does not deassert when the pll_powerdown signal is asserted in configurations that use the reference clock pre-divider of 2, 4, or 8. Figure 1 shows the reference clock pre-divider inside transmitter PLLs. This transmitter PLL lock status signal issue impacts the pll_locked status signal in both the clock multiplier unit (CMU) PLL and the auxiliary transmit (ATX) PLL.

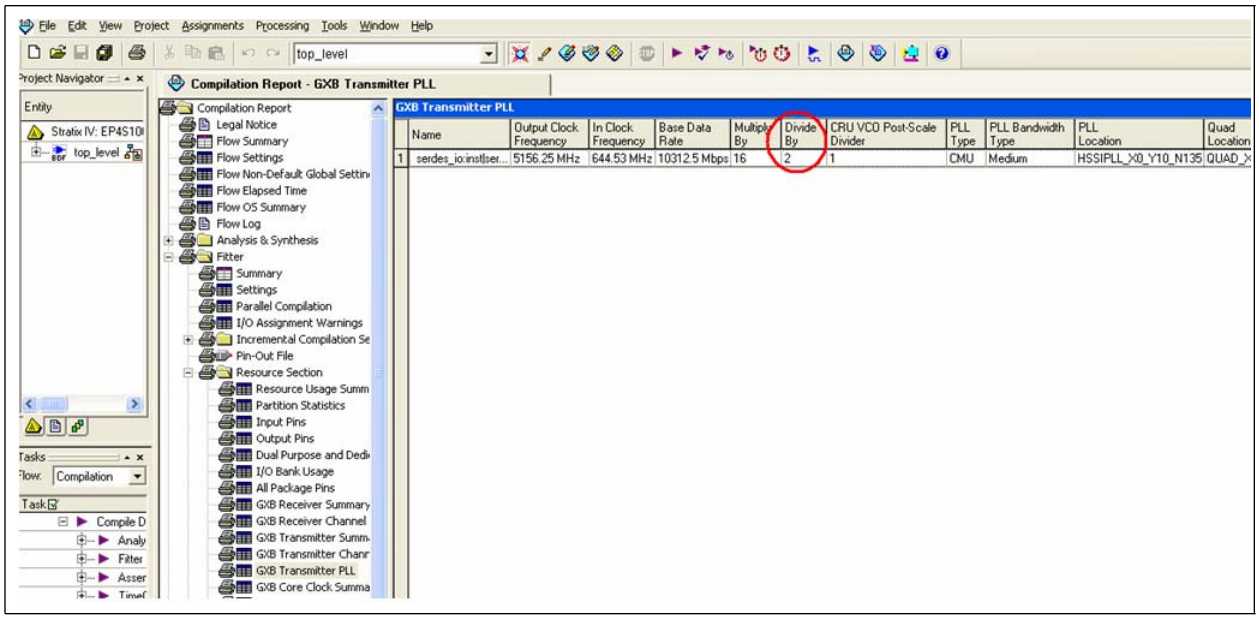
Figure 1. Reference Clock Pre-Dividers in Transmitter PLLs



Designs that implement the recommended transceiver reset sequence described in the *Reset Control and Power Down* chapter in volume 2 of the *Stratix IV Device Handbook* could potentially see a link failure after coming out of reset.

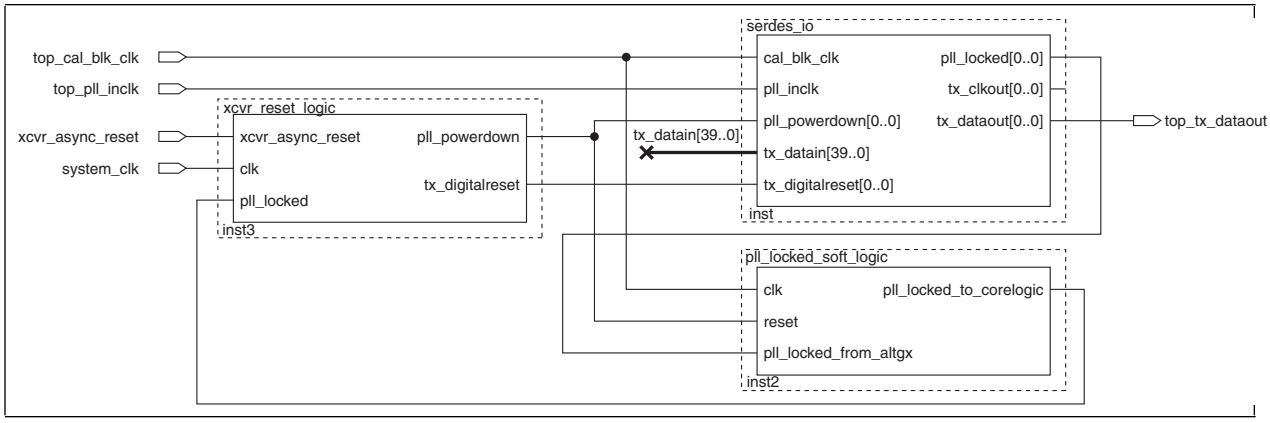
You can determine whether the Transmitter PLL in your design uses a reference clock pre-divider of 2, 4, or 8 by referring to the Quartus II software Compilation Report. Figure 2 shows an example of the GXB Transmitter PLL report, which you find in the "Resources Section" under "Fitter" in the Compilation Report. If the value in the **Divide By** column reads 2, 4, or 8, your design is impacted by the `pll_locked` status signal issue.

Figure 2. Determining Reference Clock Pre-Divider Value in the Compilation Report



If the `pll_locked` issue impacts your design, instantiate and connect the `pll_locked_soft_logic` module, as shown in Figure 3. You must use the `pll_locked_to_corelogic` output from this module in the transceiver reset logic and any user logic that relies on the transmitter PLL lock status signal.

Figure 3. Instantiating and Connecting the pll_locked_soft_logic Module



Click `pll_locked_soft_logic` to obtain the module.

Use the calibration block clock (cal_blk_clk) for the pll_locked_soft_logic module. The cal_blk_clk frequency specification ranges from 10 MHz to 125 MHz. Depending on your cal_blk_clk frequency, set the parameter p_delay_counter in the pll_locked_soft_logic so that the delay is equal to 100 us (worst-case transmitter PLL lock time).

M144K RAM Block Lock-Up

M144K blocks may lock up if there is a glitch in the clock source when rden equals 1. In the lock-up state, the RAM block does not respond to read or write operations and requires an FPGA reconfiguration to restore operation. The issue occurs within the M144K RAM in the Read Timer Trigger circuitry. A clock glitch may inadvertently freeze the Read Timer Trigger circuitry, locking the RAM block in its last operation. MLABs and M9K RAM blocks are not affected.

The workaround is to add clock-enable logic, an internal PLL, or clock-generation logic (for example, a clock divider). You can add clock-enable logic (internal or external) to disable the RAM block operation until the clock is stable. You can also gate the clock internally or externally. If FPGA resources permit, you can use an internal PLL or clock-generation logic to ensure a stable clock source at the RAM block input.

The Read Timer circuitry makes RAM block operation independent of the input clock duty cycle, thus maximizing design performance. If you cannot provide a stable clock, use the **DCD** option in the Quartus II software version 9.1 to work around this problem. When the M144K block uses the **DCD** option, the block does not exhibit the lock-up behavior, but clock high-time requirements are increased and f_{MAX} performance is degraded.

If you cannot provide a stable clock input without glitches, to enable the **DCD** option in the Quartus II software, perform the following steps:

1. On the Assignments menu, click **Settings**.
2. In the **Category** list, select **Fitter Settings**.
3. Click **More Settings**.
4. Under **Existing option settings**, set **M144K Block Read Clock Duty Cycle Dependency** to **On**.
5. Click **OK**.
6. Compile your design.

Use a **.qsf** variable instead of the previous instructions for making a global assignment.

DCD is on globally by adding the following line to the project's **.qsf** (the default is **Off**):

```
set_global_assignment -name M144K_BLOCK_READ_CLOCK_DUTY_CYCLE_DEPENDENCY
ON
```

Alternatively, you can also apply this setting to individual M144K blocks with the Assignment Editor.

Global and per instance assignments can be mixed. For example, you can set **DCD** to **On** globally, but set it to **Off** for an instance. You can also set it to **On** for an instance.

×8 and ×N Clock Line Timing Issue for Transceivers

The xN clock line timing issue in Stratix IV GT production devices affects the maximum data rate supported in the following transceiver configurations:

- Basic x8 functional mode using CMU PLL or ATX PLL (6G)
- Basic x1 and Basic x4 functional mode using ATX PLL (6G) or (10G)
- Basic (PMA Direct) xN functional mode using CMU PLL or ATX PLL (6G)
- (OIF) CEI PHY Interface functional mode using ATX PLL (6G)

The maximum supported data rate in these configurations depends on:

- Transmitter PLL type (CMU PLL, ATX PLL [6G], or ATX PLL [10G])
- Device speed grade
- Physical distance between the transmitter PLL and the transceiver channel (refer to the Placement Restrictions column in Table 2)

Table 2 lists the maximum data rate supported in the affected configurations.

Table 2. Maximum Data Rate Specification in ALTGX Functional Modes Impacted by the xN Clock Line Timing Issue (Part 1 of 2)

ALTGX Functional Mode	TX PLL Type	Bonding	Supported Data Rates		Placement Restrictions
			Speed Grade	Max Data Rate (Gbps)	
Basic x1 and Basic x4	ATX PLL (6G)	Up to x4	All (1)	6.5	It is best to use the ATX PLL (6G) adjacent to the transceiver block where the channels are located. For more information, refer to Figure 5 on page 13. The maximum distance away from the ATX PLL is two transceiver blocks.
Basic x8	CMU PLL	Up to x8	All	6.5	—
	ATX PLL (6G)	Up to x8	All (1)	6.5	It is best to use the ATX PLL (6G) between the two transceiver blocks. For more information, refer to Figure 4 on page 12. The maximum distance away from the ATX PLL is two transceiver blocks.
Basic xN (PMA Direct)	CMU PLL	Up to x17	All	6.5	Bonded channels must be contiguous. You must use the CMU PLL in the middle transceiver block. For more information, refer to Figure 6 on page 14.
		> x17	All	3.25	—
	ATX PLL (6G)	Up to x24	All (1)	6.5	You must use ATX L1 PLL (6G) for left-side bonding. You must use ATX R1 PLL (6G) for right-side bonding. For more information, refer to Figure 7 on page 15.
(OIF) CEI PHY Interface	ATX PLL (6G)	—	All (1)	6.375	You must use the 6G ATX PLL adjacent to the transceiver block where the channels are located.

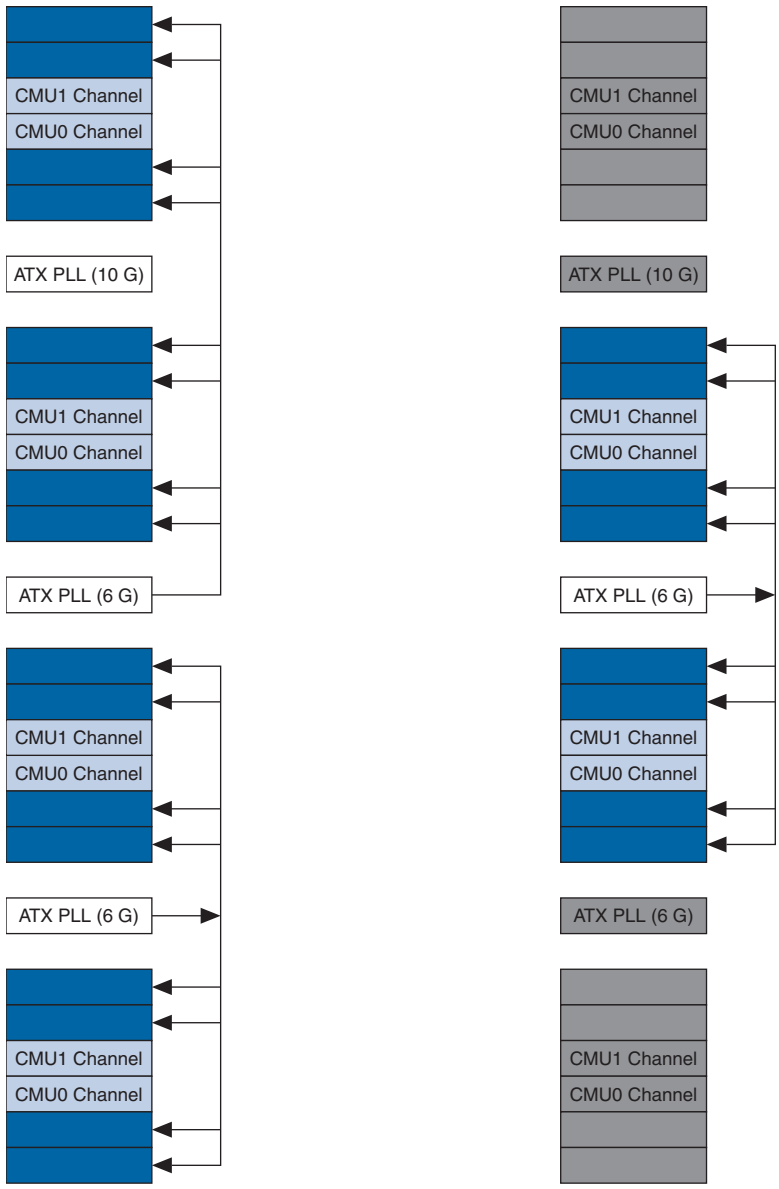
Table 2. Maximum Data Rate Specification in ALTGX Functional Modes Impacted by the xN Clock Line Timing Issue (Part 2 of 2)

ALTGX Functional Mode	TX PLL Type	Bonding	Supported Data Rates		Placement Restrictions
			Speed Grade	Max Data Rate (Gbps)	
Basic x1 and Basic x4	ATX PLL (10G)	Up to x4	All (1)	10.3	You must use the ATX PLL (10G) between the two transceiver blocks used. The ATX PLL (10G) can support the two channels just above and the two channels just below. For more information, refer to Figure 8 on page 16.

Note to Table 2:

(1) The ATX PLL (6G or 10G) is not available in I3 speed grades in Stratix IV GT devices.

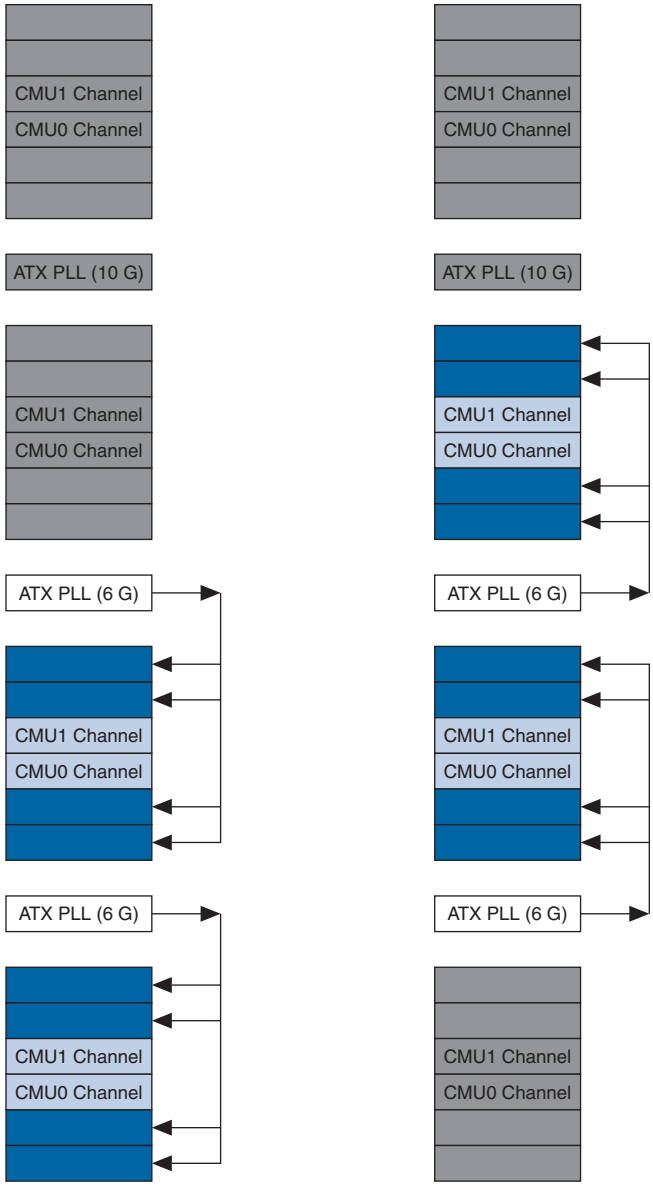
Figure 4. Placement Restrictions in Basic x8 Mode Using ATX PLLs (6G) *(1)*



Note to Figure 4:

(1) This figure shows different instantiations of Basic x8 with the 6G ATX PLL in a EP4S100G5F45 device. The best selection is to use the PLL between the transceiver blocks, but other configurations are possible. The data rate can be as high as 6.5 Gbps as long as the reach is no longer than two transceiver blocks in one direction. For example, the bottom ATX PLL could not drive the top two transceiver blocks at 6.5G, because the top transceiver block is three transceiver blocks away.

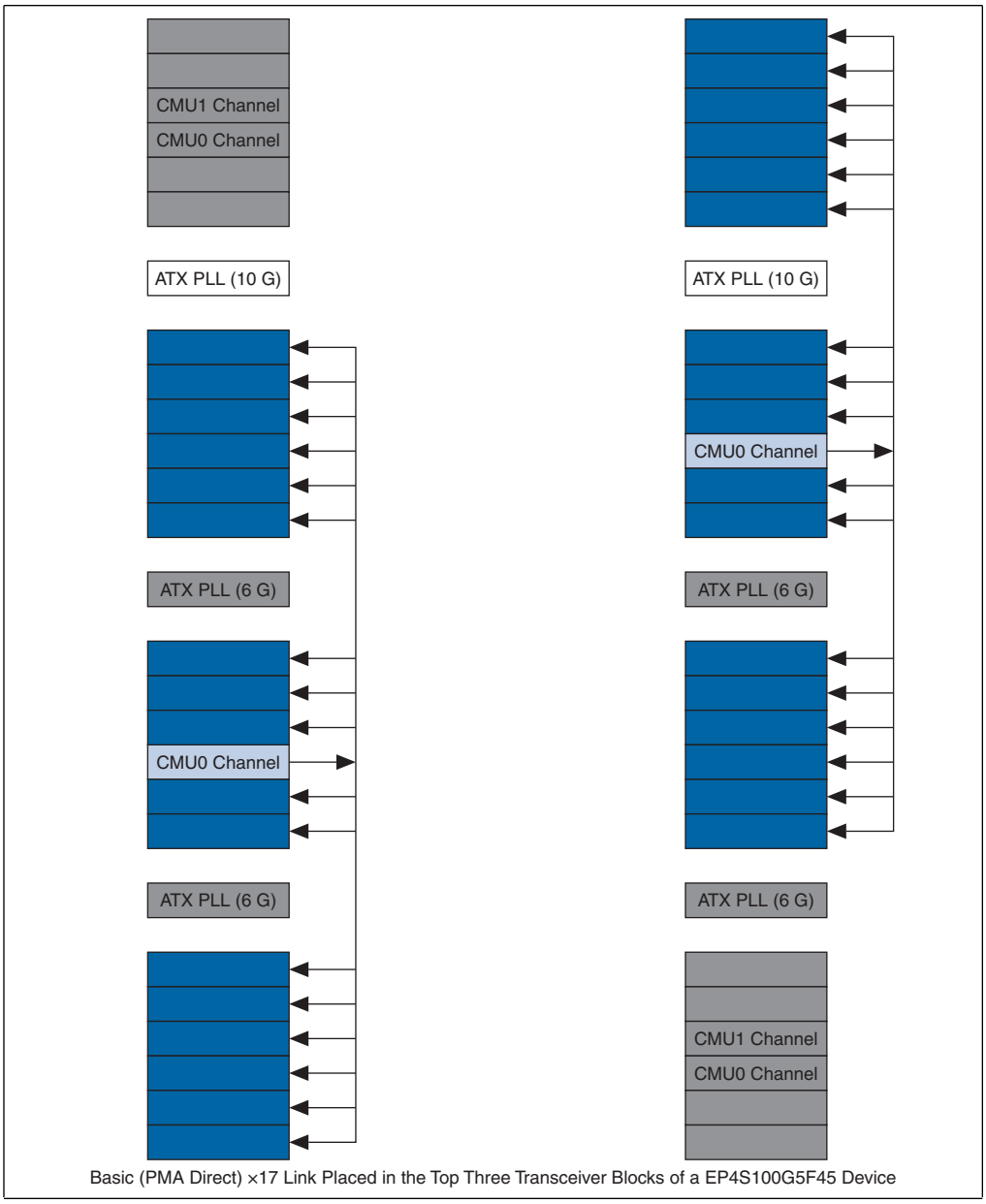
Figure 5. Placement Restrictions in Basic x1 and Basic x4 Mode Using ATX PLLs (6G) *(1)*



Note to Figure 5:

(1) These are Basic x4 instantiations with the 6G ATX PLL for best performance in a EP4S100G5F45 device.

Figure 6. Placement Restrictions in Basic (PMA Direct) xN (N=17) Mode Using CMU PLLs



Basic (PMA Direct) ×17 Link Placed in the Top Three Transceiver Blocks of a EP4S100G5F45 Device

Figure 7. Placement Restrictions in Basic (PMA Direct) xN (N=24) Using ATX PLLs (6G)

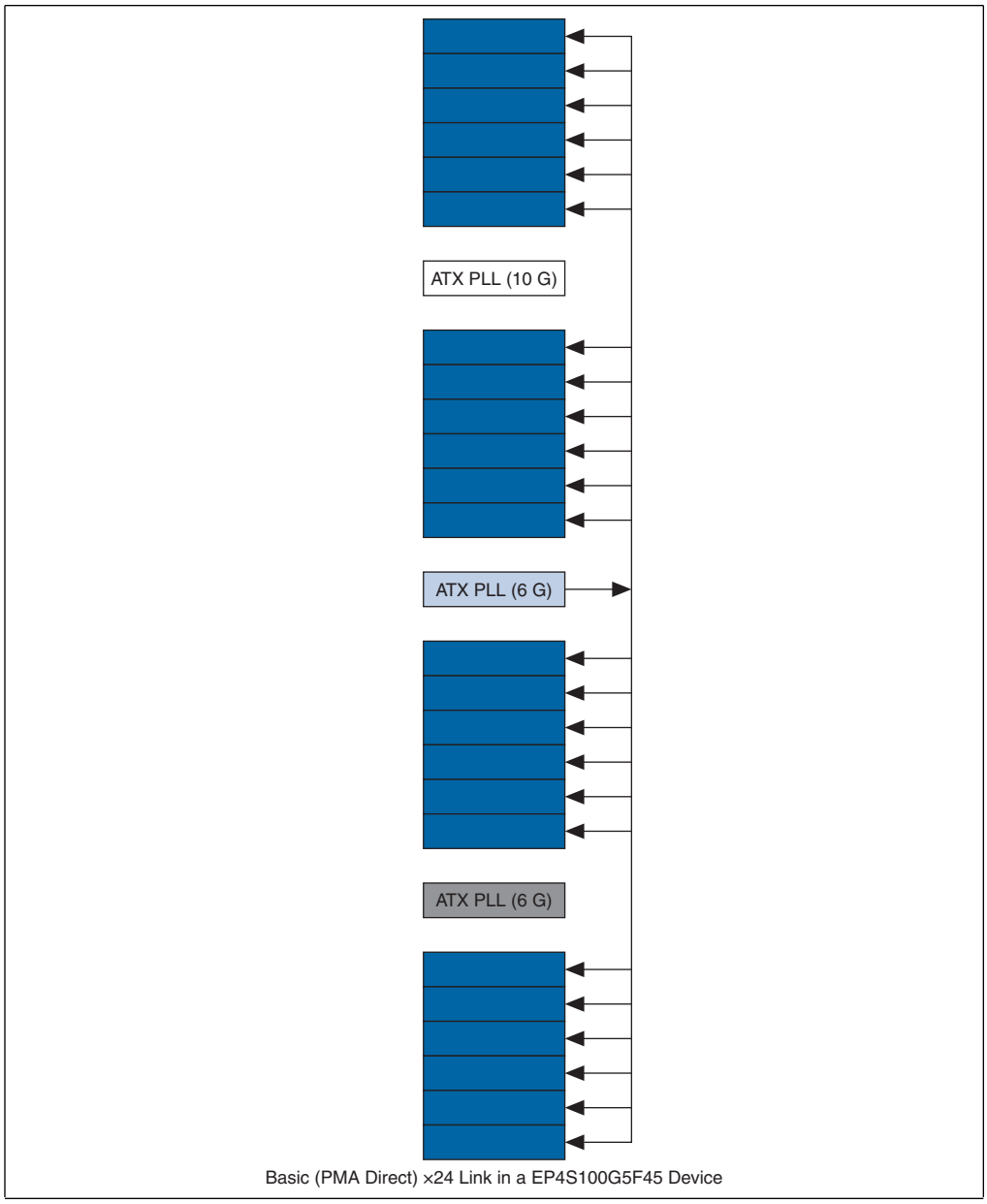
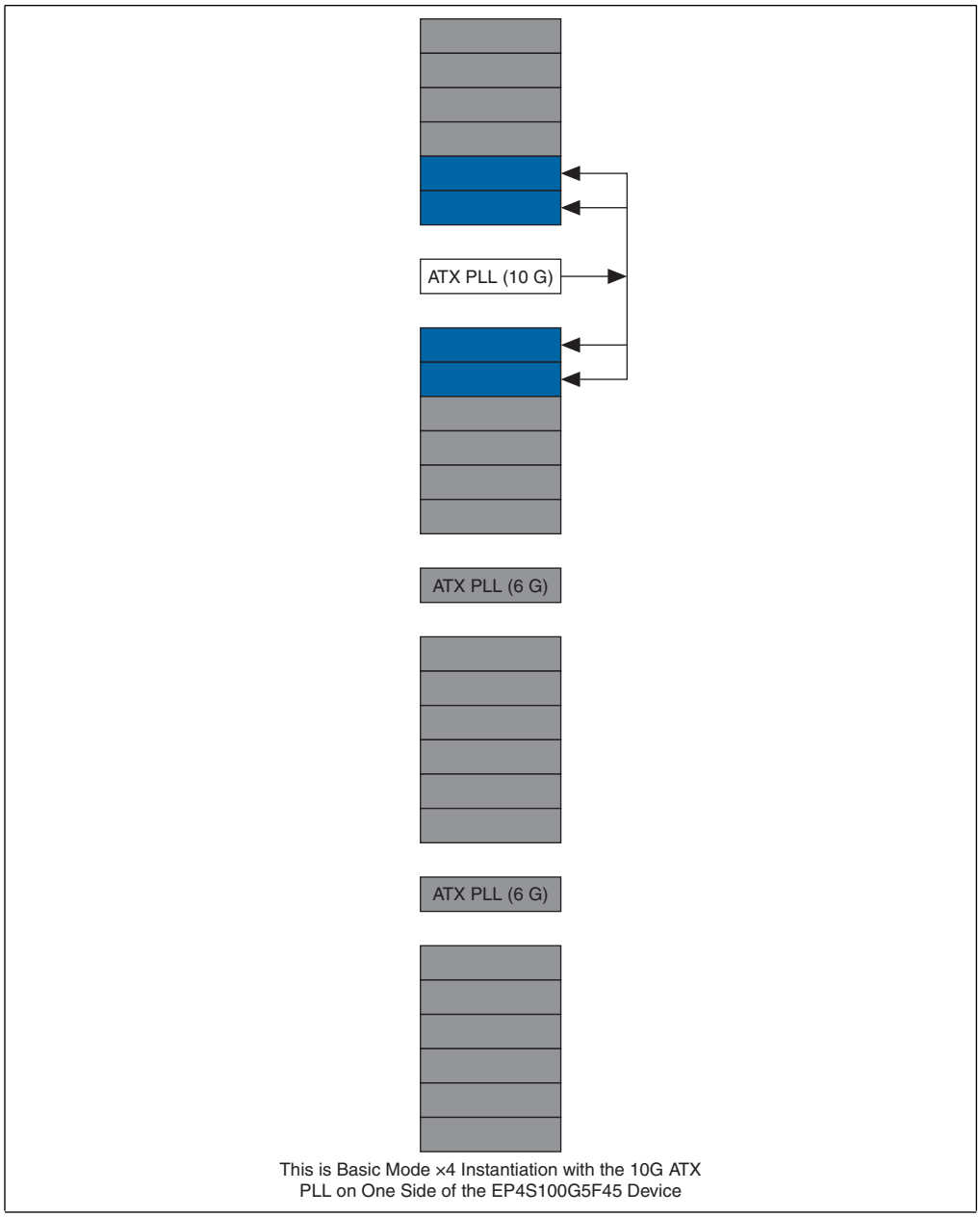


Figure 8. Placement Restrictions in Basic x1 and Basic x4 Mode Using ATX PLLs (10G)



Stratix IV GT Power-up Sequencing on Production Devices

Stratix IV GT devices might fail to power up correctly at low temperatures when the V_{CC} (0.95 V) power supply powers up after V_{CCAUX} (2.5 V) power supply. This power-up sequencing issue occurs because the device fails to exit power-on reset (POR), as indicated by the nSTATUS pin being stuck low. Configuration cannot begin when the nSTATUS pin is low.

The power-up issue occurs for all Stratix IV GT production devices. Engineering sample devices are not affected.

Production devices must use the power-up sequence board design modifications to successfully power-up and exit POR on production devices, by fully powering V_{CC} before V_{CCAUX} begins to ramp. There is no dependency on the ramp rate for V_{CC} and V_{CCAUX}. The published ramp rate specifications still apply.

☞ You can successfully use the hot socketing feature if you use the V_{CC} before V_{CCAUX} power sequence board design modification.

Contact Altera for Technical Support if you require assistance with implementing these board design changes.

High Power Supply Current During Power-Up for V_{CCPD} and $V_{CCA\_L/R}$

For more information, refer to "High Power Supply Current During Power-Up for V_{CCPD} and $V_{CCA\_L/R}$" on page 25.

Stratix IV GT ES1 Device Issues

This errata sheet provides updated information on known device issues affecting Stratix IV GT ES1 devices. Table 3 lists the naming conventions for the Stratix IV GT ES1 devices.

Table 3. Naming Conventions for Stratix IV GT ES1 Devices

G2 ES1	G5 ES1
	EP4S40G5H40C2ES1
EP4S40G2F40C2ES1	EP4S40G5H40C2NES1
EP4S40G2F40C2NES1	EP4S100G5H40C2ES1
EP4S100G2F40C2ES1	EP4S100G5H40C2NES1
EP4S100G2F40C2NES1	EP4S100G5F45C2ES1
	EP4S100G5F45C2NES1

Table 4 lists the issues and affected Stratix IV GT ES1 devices

Table 4. Family Issues for Stratix IV GT ES1 Devices (Part 1 of 3)

Issue	Affected Devices	Planned Fix
"EDCRC False Errors" The error detection CRC (SEU detection) feature may falsely assert the CRC_ERROR signal when no SEU event has occurred.	All Stratix IV GT (ES1 and Production) Devices	—
"Minimum Differential Eye Opening Requirement" The minimum differential eye opening specification has been revised for Stratix IV GT devices.	All Stratix IV GT (ES1 and Production) Devices	—
"PCI Express (PCIe) Interface with Hard IP Block Migration" PCIe interfaces using the hard IP block between specific devices cannot be migrated.	All Stratix IV GT (ES1 and Production) Devices	Quartus II software version 10.1 SP1
"PCIe Gen2 Protocol Link Establishment Issue" The PCIe rate switch controller may not be initialized correctly for the PCIe Gen2 protocol, preventing the link from being established.	All Stratix IV GT (ES1 and Production) Devices	Quartus II software version 10.1 SP1 and later. Patches are available for the Quartus II software versions 9.1 SP2 and 10.1.
"Quartus II Software Incorrect Setting for Transceiver CDR in All Modes Except PCIe Mode" The Quartus II software incorrectly sets the CDR unit when the transceiver channel is configured in any mode except PCIe mode and the CDR is configured to automatic lock mode.	All Stratix IV GT (ES1 and Production) Devices	Quartus II software version 10.1 and later. Patches are available for the Quartus II software versions 9.1 SP2 and 10.0 SP1.
"Dynamic Reconfiguration Issue Between PCIe Mode and Any Other Transceiver Mode" The transceiver may not be initialized correctly if your application uses dynamic reconfiguration to change the transceiver channel between PCIe mode and any other transceiver mode.	All Stratix IV GT (ES1 and Production) Devices	No plan to fix silicon. Apply reset workaround.
"Quartus II Mapping Issue with PCIe Interfaces Using the Hard IP Block" The Quartus II software incorrectly maps the PCIe interfaces when using the hard IP block.	Stratix IV GT ES1 and all production devices	For more information, refer to "Quartus II Mapping Issue with PCIe Interfaces Using the Hard IP Block".
"Transmitter PLL Lock (pll_locked) Status Signal" The transmitter PLL lock status signal (pll_locked) does not deassert when the pll_powerdown signal is asserted in configurations that use the reference clock pre-divider of 2, 4, or 8.	Stratix IV GT ES1 and all production devices	No plan to fix silicon. For a soft-fix solution, refer to "Transmitter PLL Lock (pll_locked) Status Signal"
"Remote System Upgrade" Remote System Upgrade fails when loading an invalid configuration image.	G2 ES1 and G5 ES1	—
"XAUI Functional Mode Failure" Channel 0 data is shifted by one cycle with respect to Channels 1, 2, and 3.	G2 ES1 and G5 ES1	Production devices

Table 4. Family Issues for Stratix IV GT ES1 Devices (Part 2 of 3)

Issue	Affected Devices	Planned Fix
"Timing Issue with Two Channels in Basic (PMA Direct) Configuration" One particular channel out of a total of 24 channels (configured in Basic [PMA Direct] mode) on either side of the device does not close timing for data rates ≥ 6.375.	G5 ES1	Production devices
"Endpoints Using the Hard IP Implementation Incorrectly Handle CfgRd0" Refer to the *Endpoints Using the Hard IP Implementation Incorrectly Handle CfgRd0* section of the *MegaCore IP Library Release Notes and Errata* document.	G2 ES1 and G5 ES1	Production devices
"M9K/M144K RAM Block Lock-Up" M9K/M144K RAM blocks may lock up due to a glitchy non-PLL clock.	G2 ES1 and G5 ES1	Production devices
"CRC Error Injection Feature" The CRC Error Injection feature may not operate correctly.	G2 ES1 and G5 ES1	Production devices
"Higher Power Supply Levels" Stratix IV GT ES1 devices require higher power supply levels.	G2 ES1 and G5 ES1	For more information, refer to "Higher Power Supply Levels" on page 23
"I/O Jitter" Stratix IV GT ES1 devices may exhibit higher than expected jitter on all non-transceiver I/O pins.	G2 ES1 and G5 ES1	Production devices
"Higher Minimum f_{INPFD} Setting" Stratix IV GT ES1 devices may exhibit higher than expected PLL jitter at low f_{INPFD} settings.	G2 ES1 and G5 ES1	Production devices
"High I/O Pin Leakage Current" Top and bottom I/O banks show higher leakage than the published Stratix IV Data Sheet version 3.0 specifications.	G2 ES1 and G5 ES1	Production devices
"Higher Standby Current for V_{CC} Supply" Higher than specified standby current on the V_{CC} supply.	G2 ES1 and G5 ES1	Production devices
"Reduced M9K/M144K Performance" Reduced M9K/M144K f_{MAX} performance for EP4SGT230 ES1 devices.	G2 ES1 and G5 ES1	Production devices
"M144K Write with Dual-Port Dual-Clock Modes" M144K RAM blocks may not operate correctly in dual-port dual-clock modes.	G2 ES1 and G5 ES1	Production devices
"Reduced Settings for Transceivers" Reduced M counter settings for ALTGX TX PLLs and RX CDRs.	G2 ES1 only	Production devices

Table 4. Family Issues for Stratix IV GT ES1 Devices (Part 3 of 3)

Issue	Affected Devices	Planned Fix
"High Power Supply Current During Power-Up for V_{CCPD} and $V_{CCA\_L/R}$" Higher power-up current requirements are needed for V_{CCPD} and $V_{CCA\_L/R}$ power supplies.	Stratix IV GT ES1 and all production devices	None
"Automatic Clock Switchover" Automatic clock switchover feature may not operate correctly.	G2 ES1 and G5 ES1	Production devices
"CRC Error Detection Feature" MLAB RAM blocks may not operate correctly with the CRC Error Detection feature enabled.	G2 ES1 and G5 ES1	Production devices
"x8 and xN Clock Line Timing Issue for Transceivers" Transceiver transmits incorrect serial bits due to timing skew on the x8 and xN clock lines.	G2 ES1 and G5 ES1	Production devices
"DPA Misalignment" DPA circuitry in Stratix IV GT ES1 devices might get stuck at the initial configured phase or move to the optimum phase after a longer than expected period of time.	G2 ES1 and G5 ES1	For more information, refer to "DPA Misalignment" on page 28.

EDCRC False Errors

For more information, refer to "EDCRC False Errors" on page 4.

Minimum Differential Eye Opening Requirement

For more information, refer to "Minimum Differential Eye Opening Requirement" on page 4.

PCI Express (PCIe) Interface with Hard IP Block Migration

For more information, refer to "PCI Express (PCIe) Interface with Hard IP Block Migration" on page 4.

PCIe Gen2 Protocol Link Establishment Issue

For more information, refer to "PCIe Gen2 Protocol Link Establishment Issue" on page 4.

Quartus II Software Incorrect Setting for Transceiver CDR in All Modes Except PCIe Mode

For more information, refer to "Quartus II Software Incorrect Setting for Transceiver CDR in All Modes Except PCIe Mode" on page 5.

Dynamic Reconfiguration Issue Between PCIe Mode and Any Other Transceiver Mode

For more information, refer to "Dynamic Reconfiguration Issue Between PCIe Mode and Any Other Transceiver Mode" on page 5.

Quartus II Mapping Issue with PCIe Interfaces Using the Hard IP Block

For more information, refer to "Quartus II Mapping Issue with PCIe Interfaces Using the Hard IP Block" on page 6.

Transmitter PLL Lock (pll_locked) Status Signal

For more information, refer to "Transmitter PLL Lock (pll_locked) Status Signal" on page 7.

Remote System Upgrade

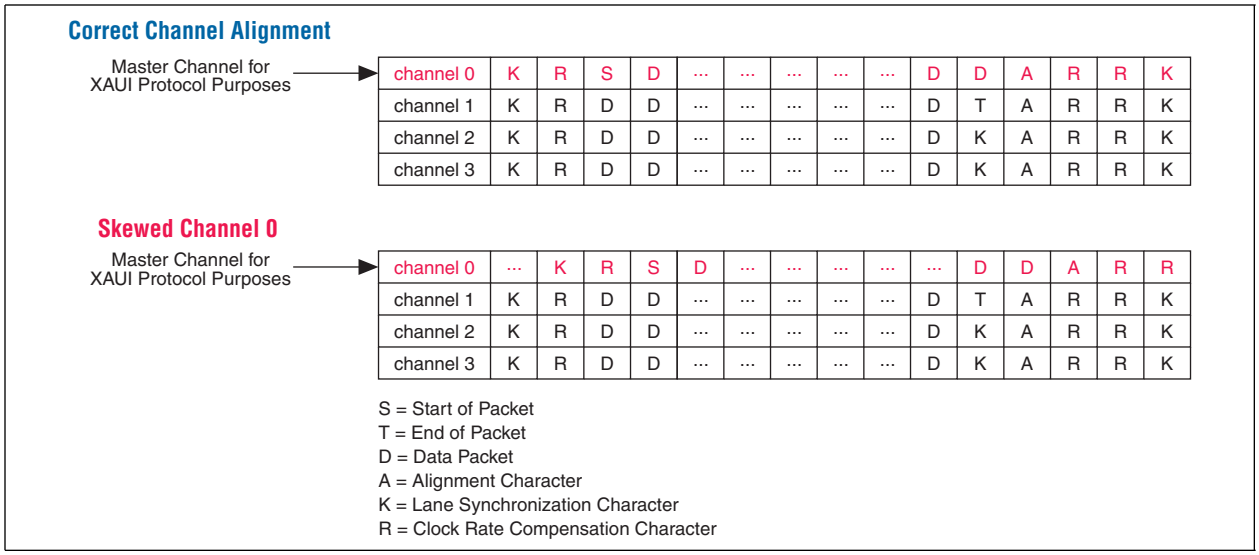
For more information, refer to "Remote System Upgrade" on page 3.

XAUI Functional Mode Failure

In XAUI functional mode, the data out of the physical transceiver channel 0's Rate Match FIFO may be shifted by one byte with respect to the data of the other three channels. This shifting causes incorrect idle ordered set conversion, resulting in incorrect received parallel data. The corrupted received parallel data caused by improper idle ordered set conversion or rate matcher corruption happens only during initialization or receiver channel reset (assertion of `rx_analogreset` or `rx_digitalreset`).

Figure 9 shows the channel skew.

Figure 9. Rate Match FIFO Skew



Altera provides a soft IP solution and associated documentation, available for download at: www.altera.com/patches/xaui-softip/xaui-softip-fix-reva.zip

Integrate this soft IP into the XAUI receiver data path. Altera will fix this issue on production devices.

Timing Issue with Two Channels in Basic (PMA Direct) Configuration

The peripheral clock from the transmitter PMA in channel 3 of GXBR0 and GXBL0 feed a peripheral clock through a multiplexer from a periphery clock region that is not adjacent to channel 3, causing additional routing delays. This delay causes one particular channel out of a total of 24 channels (configured in Basic [PMA Direct] mode) on either side of the device to not close timing for data rates ≥ 6.375.

The workaround is to route the `tx_clkout` signal for channel 3 of GXBR0 and GXBL0 to a general-purpose PLL (GPLL) that is closest to the affected channel to re-generate the clock for the transmit side logic.

For more information about implementing this workaround with a GPLL, refer to *AN 580: Achieving Timing Closure in Basic (PMA Direct) Functional Mode*.

Altera will fix this issue in production devices.

Endpoints Using the Hard IP Implementation Incorrectly Handle CfgRd0

For more information about this issue, refer to the *Endpoints Using the Hard IP Implementation Incorrectly Handle CfgRd0* section of the *MegaCore IP Library Release Notes and Errata* document.

M9K/M144K RAM Block Lock-Up

The M9K and M144K RAM blocks can lock up if the clock source glitches when `rden=1`, which can occur if the clock source is not from a PLL. In this state, a RAM block no longer responds to read or write operations and requires an FPGA reconfiguration to restore operation. This ram block lock-up issue occurs in the Read Timer Trigger circuitry, where a glitchy non-PLL clock may inadvertently freeze the Read Timer Trigger circuitry, locking the RAM block in its last operation. All RAM block modes are affected. Memory logic array blocks (MLABs) are not affected.

The workarounds are to add clock-enable logic, an internal PLL, or clock generation logic (for example, a clock divider). You can add clock-enable logic (internal or external) to disable RAM block operations until the clock is stable. You can also gate the clock internally or externally. If FPGA resources permit, you can use an internal PLL or clock generation logic to ensure a stable clock source at the RAM block input.

This issue will be fixed in production devices.

CRC Error Injection Feature

The CRC Error Injection feature on Stratix IV GT ES1 devices may not operate correctly when running the EDERROR_INJECT JTAG instruction. The CRC_ERROR output status pin might remain low, incorrectly indicating no CRC errors.

This CRC Error Injection feature issue only occurs with the error injection block and will be resolved in production devices. The CRC Error Detection feature operates correctly as expected, and is not affected by this issue.

If the CRC Error Injection feature is required with ES1 devices, contact Altera Technical Support.

Higher Power Supply Levels

Stratix IV GT ES1 devices require higher power supply levels (refer to Table 5).

Table 5. Power Supply Levels for Stratix IV GT ES1 Devices

Power Supply Pin	Power Supply Level (V)	Description
VCC	0.95	Core voltage and periphery circuitry power supply
VCCD_PLL	0.95	PLL digital power supply
VCCHIP_L	0.95	Transceiver hardware interoperability platform digital power (left side)
VCCHIP_R	0.95	Transceiver hardware interoperability platform digital power (right side)
VCCA_L	3.9	Transceiver high voltage power (left side)
VCCA_R	3.9	Transceiver high voltage power (right side)

Stratix IV GT ES1 devices require V_{CC}, V_{CCD_PLL}, and V_{CCHIP} power supplies set to **0.95 V ± 0.03 V** in all cases. This power supply level will remain the same in production.

Stratix IV GT ES1 devices require **3.9 V ± 2%** on V_{CCA_L} and V_{CCA_R}. This power supply level will return to **3.3 V** in production silicon.

Use the Stratix IV PowerPlay Early Power Estimator (EPE) version 9.0.1 to estimate current and power/thermal requirements for Stratix IV ES1 devices with the required higher power supply levels. The Stratix IV PowerPlay EPE version 9.0 will reflect current and power estimates for production devices at data sheet specifications only.

Production devices will not operate at these higher V_{CCA} power supply levels. If necessary, design your power supplies to support dropping power supply levels back to the data sheet specification for production devices.

☞ Stratix IV GT ES1 devices do have a reduced reliability to one year of operation from the elevated V_{CCA} supply. Stratix IV GT ES1 devices are to be used for prototyping only.

I/O Jitter

Stratix IV GT ES1 devices may exhibit ~+100 ps higher than expected jitter on all non-transceiver I/O pins. The actual amount of additional jitter is application and toggle-rate dependent. High-speed transceiver I/O pins are unaffected and perform to data sheet specifications.

Altera will resolve the issue in production devices, which will meet all current jitter specifications.

If you are using ES1 devices, you must account for this additional timing uncertainty in all non-transceiver I/O timing closure budgets.

Higher Minimum f_{INPFD} Setting

Stratix IV GT ES1 devices may exhibit higher than expected PLL jitter at low f_{INPFD} settings. Raising the minimum f_{INPFD} to 25 MHz removes the additional PLL jitter in ES1 devices.

Altera will resolve the issue in production devices, which will meet the current f_{INPFD} minimum of 5 MHz.

If you are using ES1 devices, review your f_{INPFD} settings by searching under "Nominal PFD Frequency" in each PLL section of your **.fit.rpt** compilation report file. If necessary, recompile your design in the Quartus II software with modified PLL settings to achieve the higher minimum f_{INPFD}.

For more information about the ALTPLL megafunction, refer to the *Quartus II Development Software Handbook* or the *Phase-Locked Loops (ALTPLL) Megafunction User Guide*.

High I/O Pin Leakage Current

Top and bottom I/O pin leakage current is higher for Stratix IV GT ES1 devices than production devices. Side I/O banks are not affected. For Stratix IV GT ES1 device I/O pin leakage on top and bottom I/O banks, refer to Table 6.

Table 6. I/O Pin Leakage Current for Top and Bottom I/O Banks

Temp.	I/O Bank Voltage					Units
	3.0 V	2.5 V	1.8 V	1.5 V	1.2 V	
25°C	35	25	15	11	9	µA
85°C	140	100	60	45	35	µA

These I/O pin leakage current values apply to Stratix IV GT ES1 silicon only and not to production silicon.

Higher Standby Current for V_{CC} Supply

You can expect to see higher standby ICC values on the 0.95-V power supply (V_{CC}) for Stratix IV GT ES1 devices than indicated in the Quartus II software version 9.0 and the Stratix IV PowerPlay EPE version 9.0. The high standby ICC current for the 0.95-V V_{CC} supply will be fixed in production devices.

Use the Stratix IV PowerPlay EPE version 9.0.1 to estimate current and power/thermal requirements for the Stratix IV GT ES1 device. The Stratix IV PowerPlay EPE version 9.0 will not be updated with these higher standby current values.

Reduced M9K/M144K Performance

M9K/M144K f_{MAX} and t_{CO} performance for Stratix IV GT ES1 devices may be lower than indicated in the Quartus II software version 8.1. Compile your design in the Quartus II software version 9.0 to estimate the impact on your design.

M144K Write with Dual-Port Dual-Clock Modes

M144K RAM blocks in dual-port dual-clock modes may fail to operate correctly, affecting applications such as DCFIFO memories, where data is transferred between two separate clock domains.

If you are using Stratix IV GT ES1 devices with the Quartus II software version 9.0, you must recompile your design and manually avoid all use of M144K RAM blocks in dual-port dual-clock modes. The Quartus II software version 9.0 SP1 automatically disables the use of dual-port dual-clock modes in all M144K RAM blocks. In both cases, your design's usage of M144K RAM blocks and M9K RAM blocks may increase as a result.

This issue will be resolved in production devices.

Reduced Settings for Transceivers

There are reduced settings for the `M` counter of the ALTGX transmitter (TX) PLLs and receiver (RX) CDRs in the transceiver blocks for the EP4S40G2 and EP4S100G2 devices. Settings with **M=16** and **M=20** in all ALTGX PLLs are removed from Basic modes and all protocol configurations.

Update your design in the ALTGX MegaWizard™ Plug-In Manager in the Quartus II software version 9.0 and recompile the design. In some cases, you may have to change your ALTGX input reference frequency, which can be done using the available GPLL resources or external clock inputs.

High Power Supply Current During Power-Up for V_{CCPD} and $V_{CCA\_L/R}$

Stratix IV GX ES devices require higher power-up current levels for V_{CCPD} and $V_{CCA\_L/R}$ power supplies than previously specified. The PowerPlay Early Power Estimator (EPE) version 9.0.1 correctly shows the V_{CCPD} and $V_{CCA\_L/R}$ power-on current for ES devices. The Quartus II software and PowerPlay EPE version 9.1 and later versions correctly show the V_{CCPD} power-on current for production devices. The Quartus II software and PowerPlay EPE version 9.1 SP1 and later versions correctly show the $V_{CCA\_L/R}$ power-on current for production devices.

Stratix IV GX ES and production device functionality is not affected by this issue, even if your V_{CCPD} and/or $V_{CCA\_L/R}$ power supplies are designed with output current levels below what the Quartus II software and/or EPE specify. Stratix IV GX ES and production devices will power-up and operate correctly as expected, provided the supplies power up monotonically and the minimum voltage requirement is met. V_{CCPD} must meet the minimum power supply voltage requirement for the device to exit POR. After the device exits POR, the V_{CCPD} current requirements return to what is reported by Altera's power estimation tools. Overall thermal power and operating current levels are not affected by this issue.

If there are other devices on the board that share the V_{CCPD} and/or $V_{CCA\_L/R}$ power supplies, you can use the Quartus II software and/or the EPE to estimate power supply current requirements. This analysis may be needed if the other devices on the board have stringent power supply integrity requirements.

There is no planned fix for the higher power-up current requirements.

Automatic Clock Switchover

The Automatic Clock Switchover feature may fail to operate correctly on Stratix IV GT ES1 devices when the two clocks are running different frequencies. If both clocks are running at the same frequency, there is no impact to your design. The following modes are affected:

- Automatic
- Automatic with Manual Override

You may observe two possible issues:

- Switchover from `inclk0` to `inclk1`, even though `inclk0` is active (and vice-versa)
- `clkbad[0,1]` status signals may glitch, even if the input clocks are active

☞ Manual clock switchover mode operates correctly as expected and is not affected.

There is no planned fix for this issue.

CRC Error Detection Feature

MLAB RAM blocks may fail to operate correctly in Stratix IV GT ES1 devices with the CRC Error Detection feature enabled. Write operations in MLAB RAM blocks are affected with all CRC Error Detection divisor settings.

☞ The CRC Error Detection feature operates correctly as expected. FPGA configuration bits are not affected by this issue.

Disabling the CRC Error Detection feature in your design compilation with the Quartus II software prevents this issue from occurring in Stratix IV GT ES1 devices.

This issue will be fixed in production devices.

x8 and xN Clock Line Timing Issue for Transceivers

Transceiver channels in Stratix GT ES1 devices may transmit incorrect serial bits due to skew accumulated from x8 and xN clock lines. This clock line timing issue leads to loss-of-link synchronization.

The following configurations are affected:

- Basic functional mode with 10G ATX PLL
- Basic x8 (PCS+PMA Bonded) functional mode with CMU PLL
- PMA direct mode xN with CMU PLL
- PMA direct mode xN with 6G ATX PLL
- (OIF) CEI PHY interface functional mode with 6G ATX PLL
- Basic functional mode x1/x4/x8 with 6G ATX PLL

Altera will fix this issue in production devices.

Table 7 lists the updated data rate ranges and behavior for the affected configurations (system constraints permitting) if you are using Stratix IV GT ES1 devices.

Table 7. Updated Data Rate Ranges and Behavior for Affected Configurations with Stratix IV GT ES1 Devices

Configuration	Updated Data Rate Ranges and Behavior
Basic functional mode with 10G ATX PLL	Not supported. Affects only the G5 ES1 device and will be fixed in production devices. The G2 ES1 device does not have the 10G ATX PLL.
Basic x8 (PCS+PMA Bonded) functional mode with CMU PLL	2.488 to 6.5 Gbps
PMA direct mode xN with CMU PLL	The number of contiguous bonded channels are reduced to ≤ 17 and the center transceiver block CMU PLL is required: ■ 2.488 to 6.5 Gbps All other configurations: ■ 2.488 to 3.25 Gbps
PMA direct mode xN with 6G ATX PLL	With contiguous bonded channels ≤ 12 (two transceiver blocks) and 6G ATX PLL between the only two transceiver blocks used or next to the only one transceiver block used: ■ 2.488 to 2.7, 3.0 to 3.25 and 4.8 to 5.4 Gbps All other configurations: ■ 2.488 to 2.7, 3.0 to 3.25 Gbps
(OIF) CEI PHY interface functional mode with 6G ATX PLL	With 6G ATX PLL between the only two transceiver blocks used or next to the only one transceiver block used: ■ 3.125 to 3.25 and 4.8 to 5.4 Gbps All other configurations: ■ 3.125 to 3.25 Gbps
Basic functional mode x1/x4/x8 with 6G ATX PLL	With 6G ATX PLL between the only two transceiver blocks used or next to the only one transceiver block used: ■ 2.488 to 2.7, 3.0 to 3.25 and 4.8 to 5.4 Gbps All other configurations: ■ 2.488 to 2.7, 3.0 to 3.25 Gbps

The best data rate ranges and behaviors shown in Table 7 require the following specific placement constraints, depending on the type of transmit PLL used by the transceiver:

- CMU PLL—the CMU PLL must be placed in the center transceiver block for a PMA direct mode xN link and on the lower transceiver block for a Basic x8 (PCS+PMA Bonded) link
- 6G ATX PLL—the transceiver channel must be placed in the adjacent transceiver block in Basic functional mode x1/x4 and between the two transceiver blocks for PMA direct mode xN

DPA Misalignment

The Stratix IV GT DPA circuitry for Stratix IV GT ES1 devices occasionally become stuck at the initial configured phase or take significantly longer than expected to select the optimum phase. A non-ideal phase may result in data bit errors, even after the DPA lock signal has gone high. Resetting the DPA circuit may not alleviate the problem; in fact, resetting the DPA circuit might trigger the problem. LVDS receivers configured in DPA mode are affected. LVDS receivers configured in soft CDR mode with 0 parts-per-million (ppm) difference (synchronous interface) are also affected.

For applications with flexibility in the choice of training patterns, Altera recommends choosing bit sequences with more data transitions and a non-cyclical pattern similar to a PRBS or K28.5 code sequence.

For applications using a fixed, cyclical, or data transition sparse training pattern (for example, if you are using the SPI 4.2 protocol, which specifies a training pattern of 10 0s and 10 1s), turn on the **DPA PLL Calibration** option (available in the Quartus II software version 9.0 and later) in the ALTLVDS MegaWizard Plug-In Manager.

There are two caveats when enabling the **DPA PLL Calibration** option:

- PLL merging (merging RX and RX or merging RX and TX PLL) is not automatically supported by the ALTLVDS megafunction; use the **external PLL** option to handle PLL merging separately.
- Timing for all PLL outputs is pulled in by 1/4 of the voltage controlled oscillator (VCO) phase during the PLL calibration process. This timing change must be taken into account for external I/O pin timing interfaces and for clock domain transfers (without a FIFO) when the clocks are not all from this same PLL.

For more information about the **DPA PLL Calibration** option, refer to the *LVDS SERDES Transmitter/Receiver (ALTLVDS_TX and ALTLVDS_RX) Megafunction User Guide* planned release corresponding to the Quartus II software version 9.0. Until the User Guide is updated, in the interim, file a service request using mySupport.

Document Revision History

Table 8 lists the revision history for this errata sheet.

Table 8. Document Revision History (Part 1 of 2)

Date	Version	Changes
February 2012	3.1	Changed Stratix V reference to Stratix IV in Table 1.
December 2011	3.0	Added the "PLL phasedone Signal Stuck at Low" section.
September 2011	2.9	■ Added the "Remote System Upgrade" section. ■ Minor text edits.
June 2011	2.8	Added the "EDCRC False Errors" section.
March 2011	2.7	■ Added the "Minimum Differential Eye Opening Requirement" and "PCI Express (PCIe) Interface with Hard IP Block Migration" sections. ■ Updated the "I/O Jitter" section in Table 1.
December 2010	2.6	Added the "PCI Express (PCIe) Gen2 Protocol Link Establishment Issue" section.
October 2010	2.5	■ Added the "Quartus II Software Incorrect Setting for Transceiver CDR in All Modes Except PCIe Mode" and "Dynamic Reconfiguration Issue Between PCIe Mode and Any Other Transceiver Mode" sections.
September 2010	2.4	■ Added the "Quartus II Mapping Issue with PCIe Interfaces Using the Hard IP Block" section. ■ Updated the "High Power Supply Current During Power-Up for VCCPD and VCCA_L/R" section. ■ Added three headings with links to improve bookmark navigation.
May 2010	2.3	■ Added the "I/O Jitter" section.
April 2010	2.2	■ Added "Fast Passive Parallel (FPP) Mode Configuration Failures at High DCLK Frequency" ■ Added "FPP Mode Configuration Failures When the Minimum Hold Time (t_{DH}) is set to 0 ns or 24 ns" ■ Updated "DPA Misalignment" and removed this issue from Production devices section ■ Updated "High Power Supply Current During Power-Up for VCCPD and VCCA_L/R"
January 2010	2.1	■ Added "Transmitter PLL Lock (pll_locked) Status Signal" ■ Updated "Stratix IV GT Power-up Sequencing on Production Devices" because the planned fix was modified.

November 2009	2.0	■ Added the following sections:
		  ■ "Stratix IV GT Production Device Issues"
		  ■ "M144K RAM Block Lock-Up"
		  ■ "×8 and ×N Clock Line Timing Issue for Transceivers"
		  ■ "Stratix IV GT Power-up Sequencing on Production Devices"
		  ■ "Stratix IV GT ES1 Device Issues"
		■ Updated "Higher Standby Current for VCC Supply" with updated voltage level

Table 8. Document Revision History (Part 2 of 2)

Date	Version	Changes
June 2009	1.1	■ Added "M9K/M144K RAM Block Lock-Up" ■ Removed references to ES2 in Table 4 ■ In the "Higher Power Supply Levels" section, revised the two paragraphs under Table 5. ■ Renamed the "MLAB Issue with CRC Error Detection Feature" section to "CRC Error Detection Feature". Revised the second sentence of this section.
April 2009	1.0	Initial release.